AHB to APB Bridge

About the AMBA Buses

The Advanced Microcontroller Bus Architecture(AMBA) specification defines an on-chip communications standard for designing high-performance microcontrollers. Three distinct buses are defined within the AMBA specification:

- **Advanced High-performance Bus (AHB)**
- **Advanced System Bus (ASB)**
- **Advanced Peripherial Bus (APB)**

Advanced High-performance Bus (AHB)

The AMBA AHB is for high-performance, high clock frequency system modules. The AHB acts as the high-performance system backbone bus. AHB supports the efficient connection of processors,on-chip memories and off-chip external memory interfaces with low-power peripherial macrocell functions. AHB is also specified to ensure ease of use in an efficient design flow using systhesis and automated test techniques.

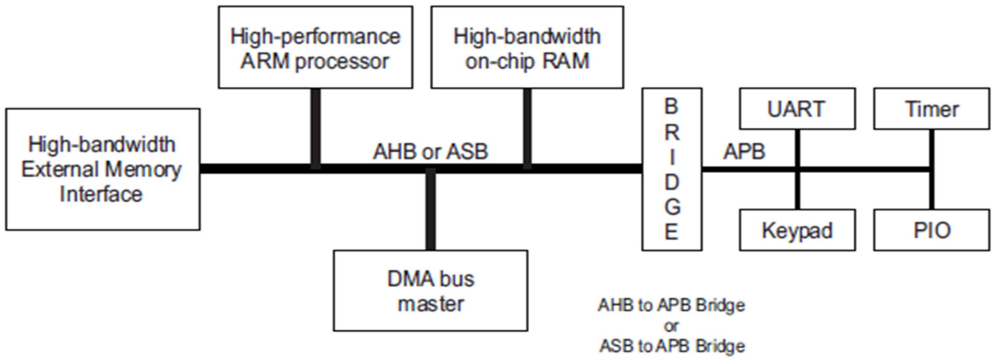
Advanced System Bus (ASB)

The AMBA ASB is for high-performance system modules. AMBA ASB is an alternative system bus suitable for use where the high-performance features of AHB are not required. ASB also supports the efficient connection of processors, on-chip memories and off-chip external memory interface with low-power peripherial macrocell functions.

Advanced Peripherial Bus (APB)

The AMBA APB is for low-power peripherials. AMBA APB is optimized for minimal power consumption and reduced interface complexity to support peripherial functions. APB can be used in conjunction with either version of the system bus.

The overall architecture looks like as:



Key functions of the AHB-to-APB bridge using an FSM:

AHB Slave Interface:

The bridge acts as a slave on the AHB bus, receiving address, control, and data signals from AHB masters.

APB Master Interface:

It acts as a master on the APB bus, initiating and managing APB transactions.

Address and Data Buffering:

The bridge buffers address and data signals received from the AHB, ensuring they are properly timed and formatted for the APB.

Peripherial Selection:

The bridge decodes the AHB address and selects the appropriate APB peripheral.

Timing Control:

The bridge generates timing signals (e.g., PENABLE, PCLK) to control the APB transactions.

Response Handling:

It handles APB responses (e.g., PREADY) and returns the appropriate response signals to the AHB.

Wait Sate Management:

The bridge can insert wait states if necessary to accommodate the APB's slower timing compared to the AHB.

Basic Terminology:

Bus cycle

A bus cycle is a basic unit of one bus clock period and for the purpose of AMBA AHB or APB protocol descriptions is defined from rising-edge to rising-edge transitions.

Bus transfer

An AMBA ASB or AHB bus transfer is a read or write operation of a data object, which may take one or more bus cycles. The bus transfer is terminated by a completion response from the addressed slave. An AMBA APB bus transfer is a read or write operation of a data object, which always requires two bus cycles.

Burst operation

A burst operation is defined as one or more data transactions, initiated by a bus master, which have a consistent width of transaction to an incremental region of address space. The increment step per

transaction is determined by the width of transfer (byte, halfword, word). No burst operation is supported on the APB.

Burst

A “Burst” refers to a sequence of data transfer between a master and a slave in a burst mode.

State Machine Logic

Resetn(at low)