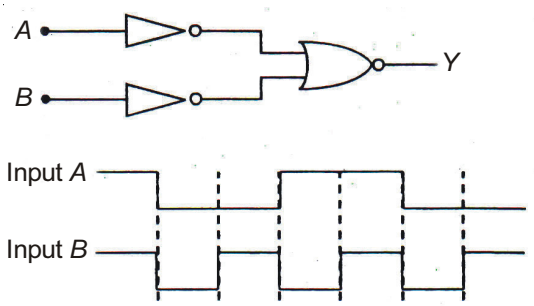
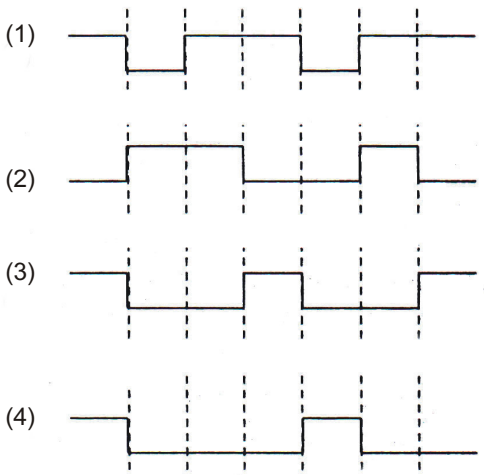
Semiconductor Electronics : Materials Devices and Simple Circuits

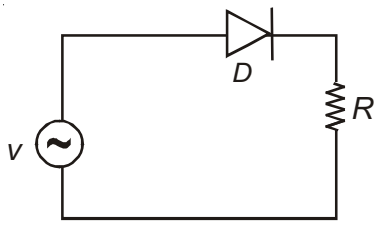
1. The logic circuit shown below has the input waveforms '*A*' and '*B*' as shown. Pick out the correct output waveform. **[AIEEE-2009]**



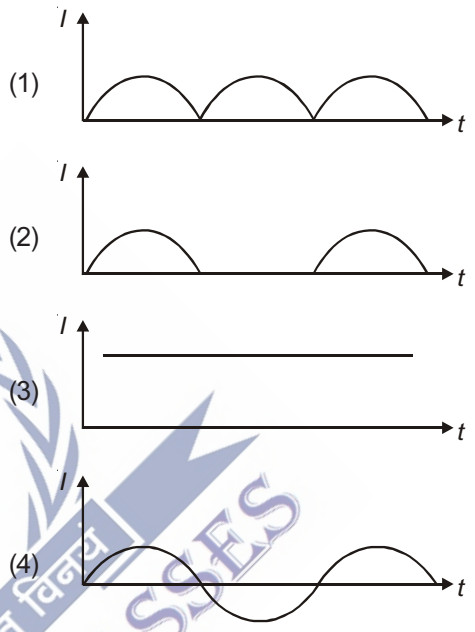
Output is :



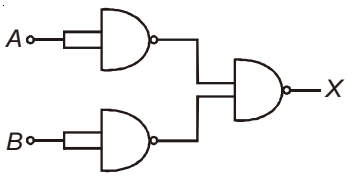
2. A *p-n* junction (*D*) shown in the figure can act as a rectifier. An alternating current source (*V*) is connected in the circuit. **[AIEEE-2009]**



The current (*I*) in the resistor (*R*) can be shown by:



3. The combination of gates shown below yields **[AIEEE-2010]**



(1) NAND gate (2) OR gate

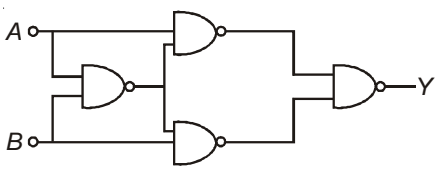
(3) NOT gate (4) XOR gate

4. The output of an OR gate is connected to both the inputs of a NAND gate. The combination will serve as a **[AIEEE-2011]**

(1) AND gate (2) OR gate

(3) NOT gate (4) NOR gate

5. Truth table for system of four NAND gates as shown in figure is **[AIEEE-2012]**



(1)

A	B	Y
0	0	0
0	1	0
1	0	1
1	1	1

(2)

A	B	Y
0	0	1
0	1	1
1	0	0
1	1	0

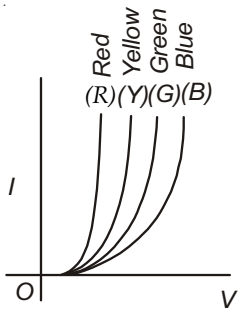
(3)

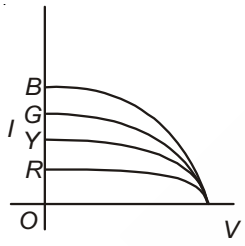
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

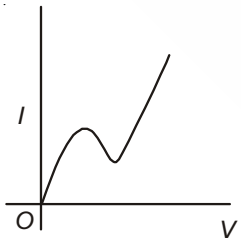
(4)

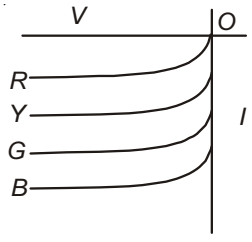
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

6. The *I* - *V* characteristic of an *LED* is **[JEE (Main)-2013]**

(1) 

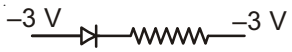
(2) 

(3) 

(4) 

7. The forward biased diode connection is **[JEE (Main)-2014]**

(1) 

(2) 

(3) 

(4) 

8. The temperature dependence of resistances of Cu and undoped Si in the temperature range 300-400 K, is best described by **[JEE (Main)-2016]**

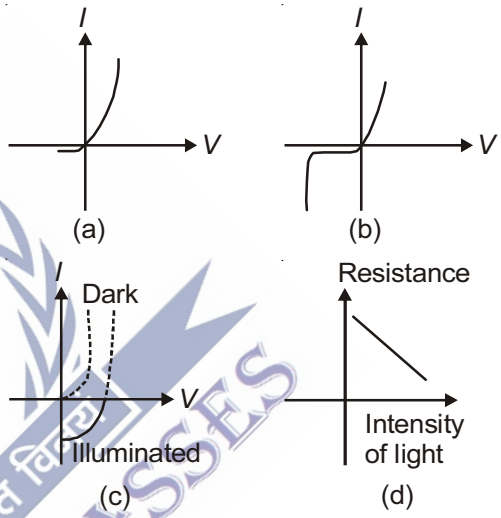
(1) Linear increase for Cu, exponential increase for Si

(2) Linear increase for Cu, exponential decrease for Si

(3) Linear decrease for Cu, linear decrease for Si

(4) Linear increase for Cu, linear increase for Si

9. Identify the semiconductor devices whose characteristics are given below, in the order (a), (b), (c), (d) : **[JEE (Main)-2016]**



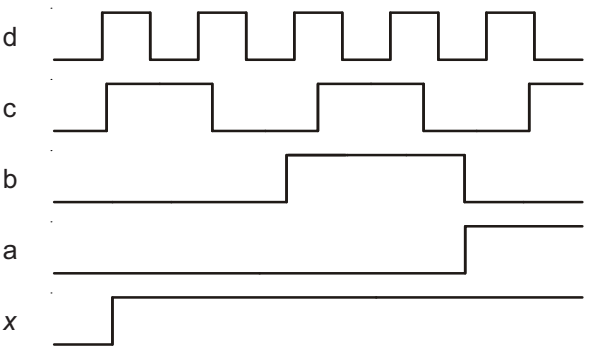
(1) Zener diode, Simple diode, Light dependent resistance, Solar cell

(2) Solar cell, Light dependent resistance, Zener diode, Simple diode

(3) Zener diode, Solar cell, Simple diode, Light dependent resistance

(4) Simple diode, Zener diode, Solar cell, Light dependent resistance

10. If a, b, c, d are inputs to a gate and *x* is its output, then, as per the following time graph, the gate is: **[JEE (Main)-2016]**



(1) AND (2) OR

(3) NAND (4) NOT

11. For a common emitter configuration, if α and β have their usual meanings, the incorrect relationship between α and β is :

[JEE (Main)-2016]

(1) $\alpha = \frac{\beta}{1-\beta}$ (2) $\alpha = \frac{\beta}{1+\beta}$

(3) $\alpha = \frac{\beta^2}{1+\beta^2}$ (4) $\frac{1}{\alpha} = \frac{1}{\beta} + 1$

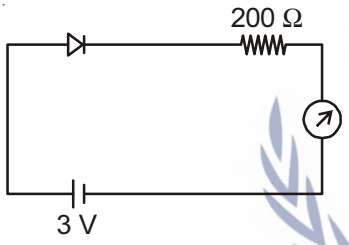
12. In a common emitter amplifier circuit using an n-p-n transistor, the phase difference between the input and the output voltages will be

[JEE (Main)-2017]

(1) 45° (2) 90°

(3) 135° (4) 180°

13. The reading of the ammeter for a silicon diode in the given circuit is **[JEE (Main)-2018]**



(1) 0 (2) 15 mA

(3) 11.5 mA (4) 13.5 mA

14. Mobility of electrons in a semiconductor is defined as the ratio of their drift velocity to the applied electric field. If, for an *n*-type semiconductor, the density of electrons is 10^{19} m^{-3} and their mobility is 1.6 $m^2/(V.s)$ then the resistivity of the semiconductor (since it is an *n*-type semiconductor contribution of holes is ignored) is close

[JEE (Main)-2019]

(1) 2 Ωm (2) 0.2 Ωm

(3) 0.4 Ωm (4) 4 Ωm

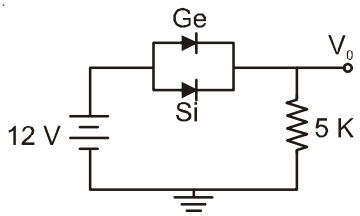
15. Drift speed of electrons, when 1.5 A of current flows in a copper wire of cross section 5 mm^2, is v. If the electron density in copper is $9 \times 10^{28}/m^3$ the value of v in mm/s is close to (Take charge of electron to be = 1.6×10^{-19} C)

[JEE (Main)-2019]

(1) 0.02 (2) 0.2

(3) 3 (4) 2

16. Ge and Si diodes start conducting at 0.3 V and 0.7 V respectively. In the following figure if Ge diode connection are reversed, the value of V_0 changes by (assume that the Ge diode has large breakdown voltage) **[JEE (Main)-2019]**

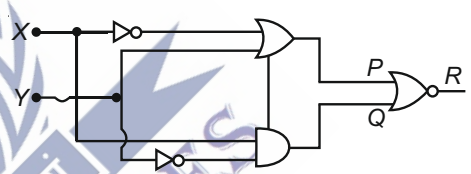


(1) 0.2 V (2) 0.4 V

(3) 0.6 V (4) 0.8 V

17. To get output '1' at *R*, for the given logic gate circuit the input values must be

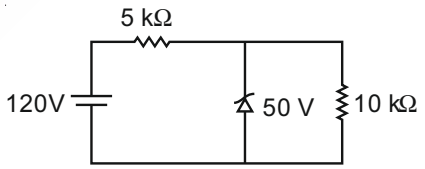
[JEE (Main)-2019]



(1) X = 1, Y = 1 (2) X = 0, Y = 0

(3) X = 1, Y = 0 (4) X = 0, Y = 1

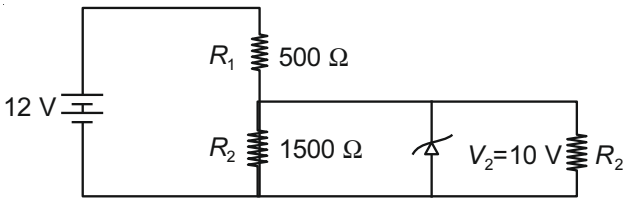
18. For the circuit shown below, the current through the Zener diode is **[JEE (Main)-2019]**



(1) Zero (2) 9 mA

(3) 14 mA (4) 5 mA

19. In the given circuit the current through Zener Diode is close to **[JEE (Main)-2019]**

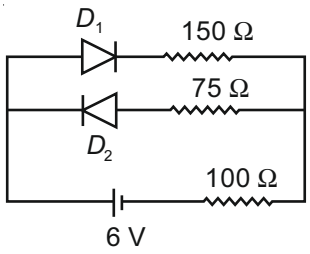


(1) 6.7 mA (2) 0.0 mA

(3) 4.0 mA (4) 6.0 mA

20. The circuit shown below contains two ideal diodes, each with a forward resistance of 50 Ω. If the battery voltage is 6 V, the current through the 100 Ω resistance (in amperes) is

[JEE (Main)-2019]

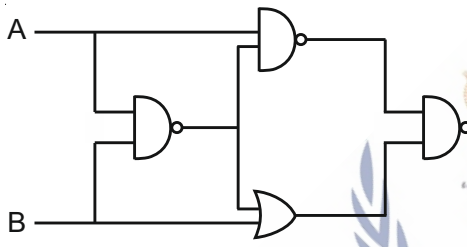


(1) 0.036 (2) 0.020

(3) 0.030 (4) 0.027

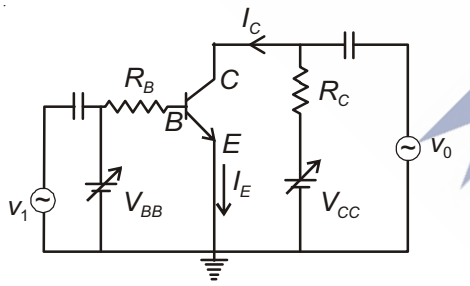
21. The output of the given logic circuit is

[JEE (Main)-2019]



(1) $A\bar{B} + \bar{A}B$ (2) $A\bar{B}$

(3) $AB + \overline{AB}$ (4) $\bar{A}B$

22. 

In the figure, given that V_{BB} supply can vary from 0 to 5.0 V, V_{CC} = 5 V, β_{dc} = 200, R_B = 100 $k\Omega$, R_C = 1 $k\Omega$ and V_{BE} = 1.0 V. The minimum base current and the input voltage at which the transistor will go to saturation, will be respectively

[JEE (Main)-2019]

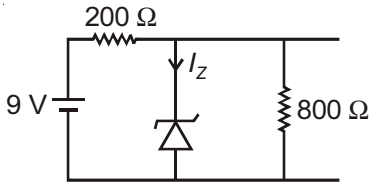
(1) 25 μA and 3.5 V

(2) 20 μA and 2.8 V

(3) 25 μA and 2.8 V

(4) 20 μA and 3.5 V

23. The reverse breakdown voltage of a Zener diode is 5.6 V in the given circuit. **[JEE (Main)-2019]**

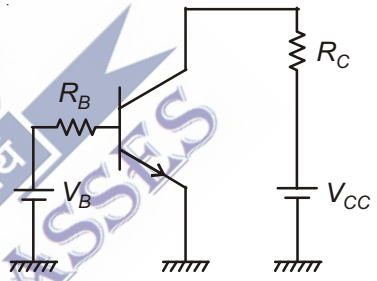


The current I_Z through the Zener is

(1) 15 mA (2) 7 mA

(3) 10 mA (4) 17 mA

24. A common emitter amplifier circuit, built using an npn transistor, is shown in the figure. Its dc current gain is 250, R_C = 1 kΩ and V_{CC} = 10 V. What is the minimum base current for V_{CE} to reach saturation? **[JEE (Main)-2019]**



(1) 10 μA (2) 100 μA

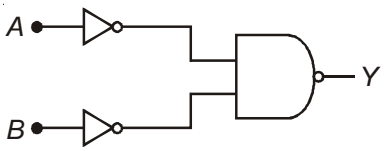
(3) 7 μA (4) 40 μA

25. An NPN transistor is used in common emitter configuration as an amplifier with 1 kΩ load resistance. Signal voltage of 10 mV is applied across the base-emitter. This produces a 3 mA change in the collector current and 15 μA change in the base current of the amplifier. The input resistance and voltage gain are **[JEE (Main)-2019]**

(1) 0.33 kΩ, 1.5 (2) 0.33 kΩ, 300

(3) 0.67 kΩ, 200 (4) 0.67 kΩ, 300

26. The logic gate equivalent to the given logic circuit is **[JEE (Main)-2019]**



(1) OR (2) NAND

(3) AND (4) NOR

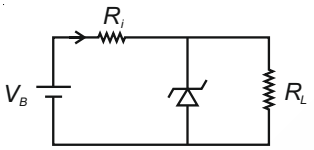
27. An npn transistor operates as a common emitter amplifier, with a power gain of 60 dB. The input circuit resistance is 100 Ω and the output load resistance is 10 kΩ. The common emitter current gain β is : **[JEE (Main)-2019]**

(1) 10^4 (2) 6×10^2

(3) 10^2 (4) 60

28. The figure represents a voltage regulator circuit using a Zener diode. The breakdown voltage of the Zener diode is 6 V and the load resistance is, R_L = 4 kΩ. The series resistance of the circuit is R_i = 1 kΩ. If the battery voltage V_B varies from 8 V to 16 V, what are the minimum and maximum values of the current through Zener diode?

[JEE (Main)-2019]

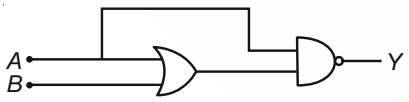


(1) 0.5 mA; 6 mA (2) 0.5 mA; 8.5 mA

(3) 1.5 mA; 8.5 mA (4) 1 mA; 8.5 mA

29. The truth table for the circuit given in the fig. is:

[JEE (Main)-2019]



(1)

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

(2)

A	B	Y
0	0	0
0	1	0
1	0	1
1	1	1

(3)

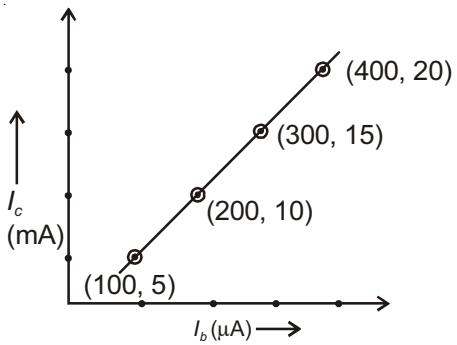
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	1

(4)

A	B	Y
0	0	1
0	1	1
1	0	0
1	1	0

30. The transfer characteristic curve of a transistor, having input and output resistance 100 Ω and 100 kΩ respectively, is shown in the figure. The Voltage and Power gain, are respectively :

[JEE (Main)-2019]



(1) 5×10^4, 2.5×10^6

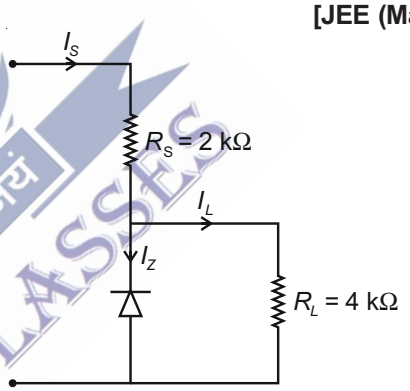
(2) 2.5×10^4, 2.5×10^6

(3) 5×10^4, 5×10^6

(4) 5×10^4, 5×10^5

31. Figure shows a *DC* voltage regulator circuit, with a Zener diode of breakdown voltage = 6 V. If the unregulated input voltage varies between 10 V to 16 V, then what is the maximum Zener current?

[JEE (Main)-2019]

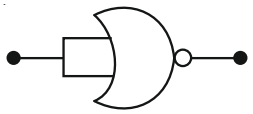


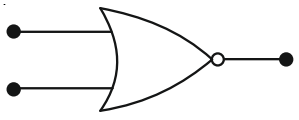
(1) 7.5 mA (2) 1.5 mA

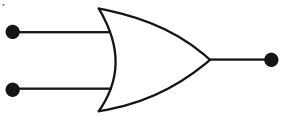
(3) 2.5 mA (4) 3.5 mA

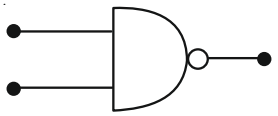
32. Which of the following gives a reversible operation?

[JEE (Main)-2020]

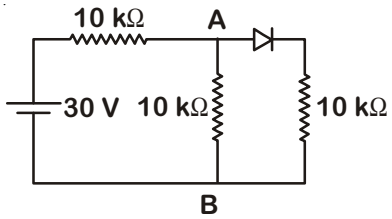
(1) 

(2) 

(3) 

(4) 

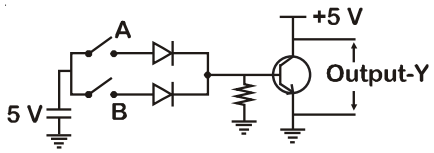
33. In the figure, potential difference between A and B is **[JEE (Main)-2020]**



(1) Zero (2) 5 V

(3) 10 V (4) 15 V

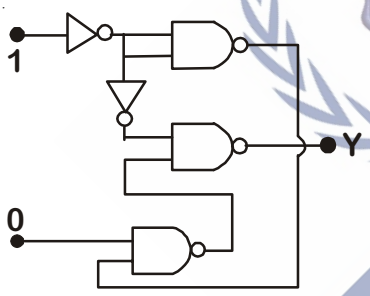
34. Boolean relation at the output stage-Y for the following circuit is **[JEE (Main)-2020]**



(1) $\bar{A} \cdot \bar{B}$ (2) $A \cdot B$

(3) $A + B$ (4) $\bar{A} + \bar{B}$

35. In the given circuit, value of Y is **[JEE (Main)-2020]**



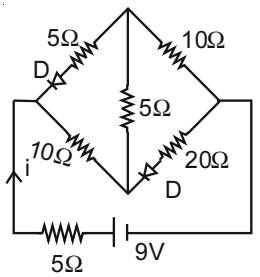
(1) Toggles between 0 and 1

(2) 0

(3) 1

(4) Will not execute

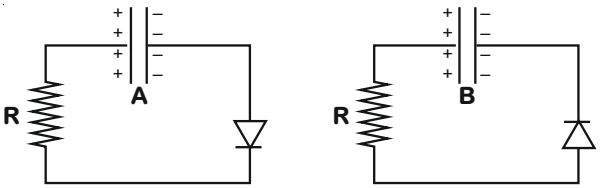
36. The current i in the network is **[JEE (Main)-2020]**



(1) 0.3 A (2) 0.6 A

(3) 0 A (4) 0.2 A

37. Two identical capacitors A and B, charged to the same potential 5 V are connected in two different circuits as shown below at time $t = 0$. If the charge on capacitors A and B at time $t = CR$ is Q_A and Q_B respectively, then (Here e is the base of natural logarithm) **[JEE (Main)-2020]**



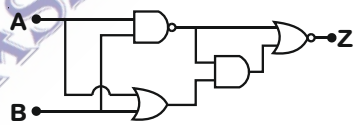
(1) $Q_A = \frac{CV}{2}, Q_B = \frac{VC}{e}$

(2) $Q_A = VC, Q_B = CV$

(3) $Q_A = \frac{CV}{e}, Q_B = \frac{VC}{2}$

(4) $Q_A = VC, Q_B = \frac{VC}{e}$

38. In the following digital circuit, what will be the output at 'Z', when the input (A, B) are (1, 0), (0, 0), (1, 1,), (0, 1) **[JEE (Main)-2020]**



(1) 1, 1, 0, 1 (2) 0, 0, 1, 0

(3) 1, 0, 1, 1 (4) 0, 1, 0, 0

39. When a diode is forward biased, it has a voltage drop of 0.5 V. The safe limit of current through the diode is 10 mA. If a battery of emf 1.5 V is used in the circuit, the value of minimum resistance to be connected in series with the diode so that the current does not exceed the safe limit is **[JEE (Main)-2020]**

(1) 50 Ω (2) 200 Ω

(3) 300 Ω (4) 100 Ω

40. If a semiconductor photodiode can detect a photon with a maximum wavelength of 400 nm, then its band gap energy is **[JEE (Main)-2020]**

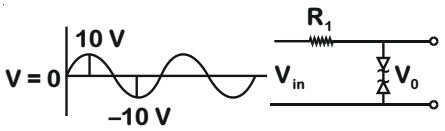
Planck's constant $h = 6.63 \times 10^{-34}$ J.s.

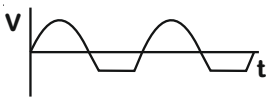
Speed of light $c = 3 \times 10^8$ m/s

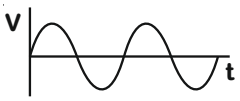
(1) 1.1 eV (2) 2.0 eV

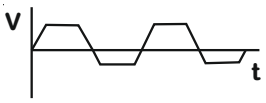
(3) 3.1 eV (4) 1.5 eV

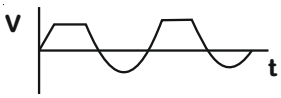
41. Take the breakdown voltage of the zener diode used in the given circuit as 6 V. For the input voltage shown in figure below, the time variation of the output voltage is (Graphs drawn are schematic and not to scale) **[JEE (Main)-2020]**



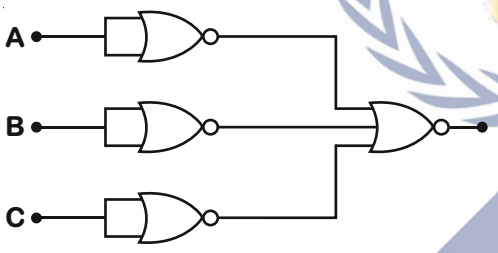
(1) 

(2) 

(3) 

(4) 

42. Identify the operation performed by the circuit given below. **[JEE (Main)-2020]**



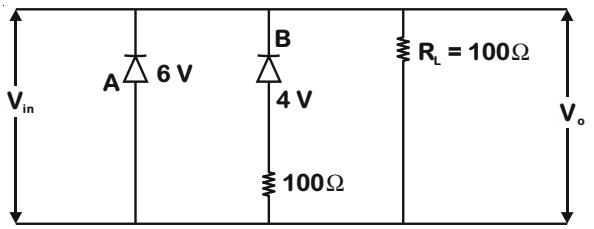
(1) AND (2) NOT

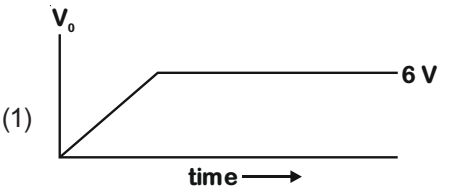
(3) NAND (4) OR

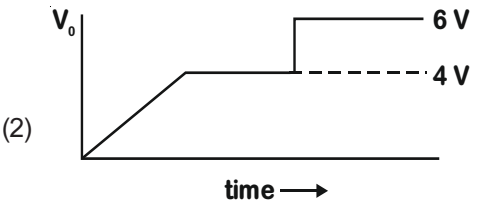
43. Two Zener diodes (*A* and *B*) having breakdown voltages of 6 V and 4 V respectively, are connected as shown in the circuit below. The output voltage V_0 variation with input voltage linearly increasing with time, is given by

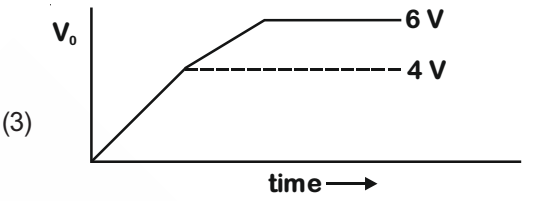
(V_{input} = 0 V at t = 0)

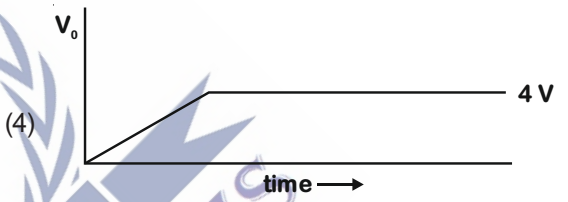
(figures are qualitative) **[JEE (Main)-2020]**



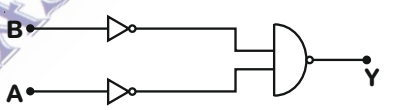
(1) 

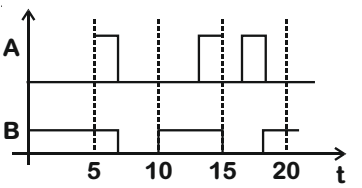
(2) 

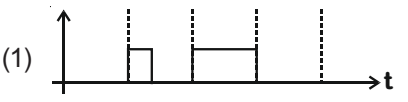
(3) 

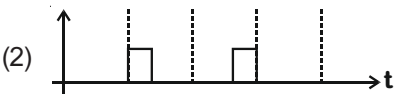
(4) 

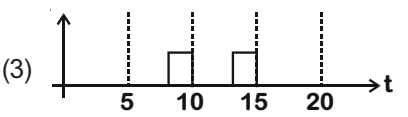
44. Identify the correct output signal *Y* in the given combination of gates (as shown) for the given inputs *A* and *B*. **[JEE (Main)-2020]**

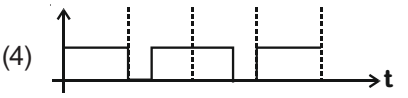




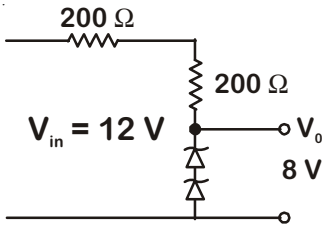
(1) 

(2) 

(3) 

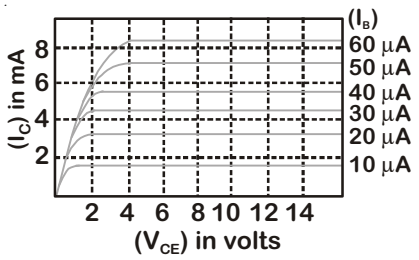
(4) 

45. The circuit shown below is working as a 8 V dc regulated voltage source. When 12 V is used as input, the power dissipated (in mW) in each diode is; (considering both zener diodes are identical) _____. **[JEE (Main)-2020]**

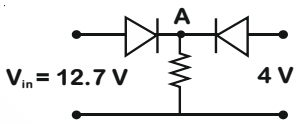


46. The output characteristics of a transistor is shown in the figure. When V_{CE} is 10 V and I_C = 4.0 mA, then value of β_{ac} is _____.

[JEE (Main)-2020]



47. Both the diodes used in the circuit shown are assumed to be ideal and have negligible resistance when these are forward biased. Built in potential in each diode is 0.7 V. For the input voltages shown in the figure, the voltage (in Volts) at point *A* is _____ **[JEE (Main)-2020]**



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