Implementation of 1-bit Full adder using CMOS mirror logic

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17 February 2022

***Abstract*—In this paper I am going to design 1-bit full adder using CMOS mirror logic. Using Mirror logic, the power consumptions of circuits can be reduced to the effective level by supplying it with low power supply. These circuits are frequency independent circuits. Here, a 28 transistors full adder is constructed the circuit is simulated using LT SPICE tool in 180 nm technology.**

***Keywords*—CMOS, Full adder, mirror logic, power consumption.**

I. INTRODUCTION

Full Adder is the adder which adds three inputs and produces two outputs. The first two inputs are A and B and the third input is an input carry as C_{in} The output carry is designated as C_{out} and the normal output is designated as SUM The expressions for sum and C_{out} are

$$Sum = A \oplus B \oplus Cin$$

$$Cout = AB + Cin\ (A+B)$$

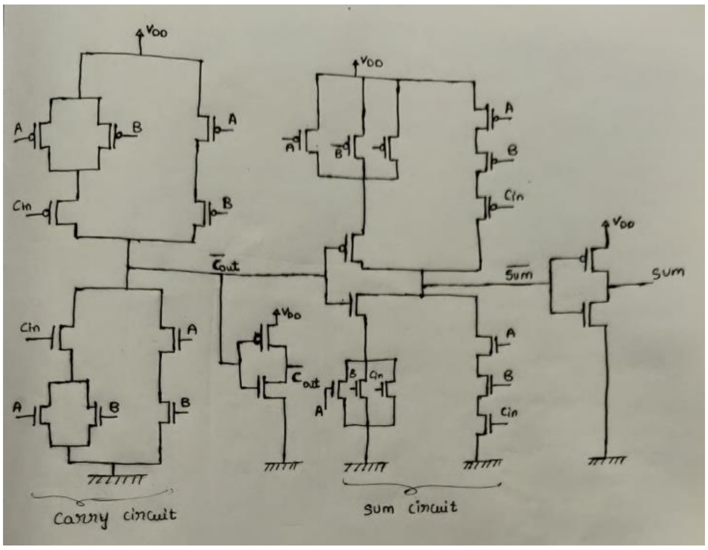
By using the above equations, we can design full adder using static cmos logic but it takes nearly 40 transistors to build it. By using the simple current mirror logic, we can reduce the total number of transistors and power consumption. Indeed, compared to static CMOS logic, it exhibits a very low switching noise, a very high speed and a better power efficiency at high operating frequencies other than a significantly lower sensitivity to process variability. These features are exploited in current high resolution mixed signal Integrated Circuits (ICs), high speed arithmetic cores, multiplexing/demultiplexing ICs for optical fiber communication systems and RF circuits [2].

To implement mirror logic the pull up and pull-down network of carry circuit and sum circuit should be same, with this we can reduce the number of transistors used to build the circuit to 28 and the total power consumption in the circuit. As the full adder equations obeys duality and inversion, we can convert above equations to the following to implement mirror logic easily.

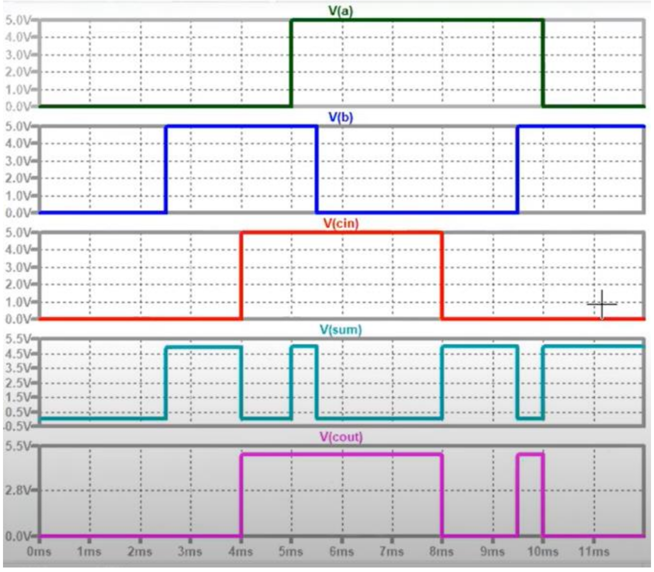
$$Cout = AB + Cin\ (A+B) \Leftrightarrow (A+B)\ (Cin+AB)$$

$$Sum = ABCin + Cout(A+B+Cin) \Leftrightarrow (A+B+Cin)\ (Cout+ABCin)$$

II. REFERENCE CIRCUIT DESIGN



III. REFERENCE CIRCUIT WAVEFORMS



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