POKHARA UNIVERSITY

Level: Bachelor	Semester: Spring	Year : 2018
Programme: BE Computer		Full Marks: 100
Course: Embedded System		Pass Marks: 45
		Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a) Define embedded system. Discuss the various skills required for an embedded system designer. 7

   b) Design a synchronous sequential machine that produces output 1 when input sequence is 1101 using T-flip flop. 8

2. a) Design a custom single-purpose processor that generates Fibonacci series up to n places. Start with a function computing the desired result, translate it into a state diagram, and sketch a probable datapath. 8

   b) Discuss basic architecture of general purpose processor with necessary diagram. 7

3. a) What is memory cache mapping? Explain cache mapping techniques. 8

   b) How can you compose memory to increase number and width of words? Design 2KX16 ROMs using 1KX8 ROMs.(1K=1024 words). 7

4. a) Define arbtitration. Explain in brief about daisy chain and network oriented arbitration. 8

   b) Define scheduling? Explain various types of task scheduling techniques in RTOS. 7

5. a) Briefly explain the terms: 7

   i) Cross-assemblers

   ii) Cross-compilers

   OR

   Sketch a simple MOSFET Model and hence deduce its analytic equation to determine speed, propagation Delay and Fan out.

   b) Explain task and state of tasks in a system with necessary diagram. 8

6. a) Write an assembly language program for 8051 microcontroller for the following condition. The controller is connected to a single LED and three push buttons PB1, PB2 and PB3 respectively. If PB1 is pressed, the LED blinks 1 time. If PB2 is pressed, the LED blinks 2 times and If PB3 is pressed LED blinks 3 times. Show with necessary connection diagram. 8

b). Write a VHDL program for 4-to-1 MUX. 7

7. Write short notes on: **(Any two)** 2×5

a) DMA

b) Superscalar and VLIW Architectures.

c) Modelling techniques in VHDL