

Chapter 7: Control System (Contd...)

Software coding of PID controller

- PID controller can be implemented using software.
- First of all, initialization is done which is followed by reading reference value and sensor value.
- Error is then calculated which is used to compute the output of PID controller.
- the output is then fed to actuator which in turn controls the process or plant based on proportional, integral and derivative constant.

* Pseudo code for the PID controller

- set values for Pgain, Igain, Dgain
- initialize prior_error = 0 and integral = 0
- Repeat following steps
 - * sensorValue = getValueFromSensor();
 - * refValue = getReferenceValue();
 - * error = refValue - sensorValue;
 - * Integral = integral + error * ~~iterationTime~~
+ error * iterationTime;
 - * derivative = (error - prior_error) / iterationTime;
 - * output = Pgain * error + Igain * integral
+ Dgain * derivative;
 - * setActuator(output);
 - * prior_error = error;
 - * wait(iterationTime);

No. _____
Date _____

PID Tuning

- is adjustment of its control parameters to the optimum values for desired control response.
- to determine value of P, I, and D based on quantitative analysis
- * Quantitative analysis is not necessary when safety and cost of the plant is not a concern.
- Ad hoc tuning process is one of the tuning method.

* steps for Ad hoc tuning process

- ① start with small value of P_{gain} , I_{gain} and D_{gain} as '0'.
- ② Increase value of D_{gain} until oscillation is seen and then D_{gain} is decreased by a factor of 2 to 4.
- ③ Increase the value of P_{gain} until oscillation or excessive overshoot is observed, and then P_{gain} is reduced by a factor of 2 to 4.
- ④ Increase the value of I_{gain} ; reduce it slightly when oscillation or excessive overshoot is seen.
- ⑤ Above steps are repeated until satisfactory performance is achieved.

No. _____
Date _____

Practical Issue Related to computer-Based control

- ① quantization and overflow error.
- ② Aliasing
- ③ computation delay.

1) Quantization and Overflow Error

- when number system of a machine is not fit to the computer memory.

* case I :

- when arithmetic results requires more precisions than original values; so, overflow error.
eg: in operation $0.50 \times 0.25 = 0.125$
the final result requires more precisions.

* case II :

- When analog signals are quantized by ADC (Analog to digital converter) it can create quantization error.
- In quantization process, limited set of discrete values are defined and unmatched signal level rounds or truncates to defined discrete value; so, rounding or truncation causes the quantization error.

overflow error

- occurs when system attempts to operate on or results a number out of range defined
eg: lots consider signed binary number

No. _____
Date _____

- five bits are used to represent magnitude and sixth or MSB is used for sign.
- * consider addition of 010010 (+18) and 010101 (+21) are added to 100111 (-25) rather than (+99).

(b) Aliasing

- is the consequence of improper sampling process.
- It appears when signal is discretely sampled at a rate that is insufficient to capture the changes in the signal.
- this is actually the distortion of reconstructed signal

Ex:

- Sampling period is 0.4 sec; so the sampling frequency is 2.5 Hz

Now, sample following signal

$$y_1(t) = 1.0 \times \sin(6\pi t), \text{ freq} = 3 \text{ Hz}$$

$$y_2(t) = 1.0 \times \sin(\pi t), \text{ freq} = 0.5 \text{ Hz}$$

- * $y_2(t)$ is indistinguishable, when sampled at 2.5 Hz, from signal $y_1(t)$.
- * can only correctly sample signal below Nyquist Frequency, which is half of the value of sampling rate.

No. _____
Date _____

(c) computation delay

- In general, computation delay is common in digital signal; but too much delay results in performance degradation.

* analysis should be accurate to ensure the effect. If computation delay is negligible

* synchronous design makes the hardware delay to characterize easily

* for software delay, careful organization of code is demanding and delay is predictable.

Aliasing

f_m

original signal

$f_s > 2f_m$

oversampling

$f_s = 2f_m$

perfect sampling

$f_s < 2f_m$

undersampling

No. _____
Date _____

Benefits of computer-Based control implementation

- (a) Repeatability
- (b) stability
- (c) programmability
- (d) flexibility.

a) Repeatability

- Analog signal systems are more prone to aging, temperature and manufacturing tolerance effects which cause results to vary with time;

However, digital systems can produce identical identical results for longer time

b) stability

- since digital systems are less prone to different sorts of degradation, and optimizations can be implemented efficiently; system can become stable

c) programmability

- Advanced features can be easily implemented in digital system but that would be very complex in analog implementation.
- some features include:
 - (1) control mode and gain switching
 - (2) online performance evaluation.
 - (3) data storage,
 - (4) performance evaluation parameter estimation
 - (5) Adaptive behavior.

No. _____
Date _____

d) flexibility

- easy re-configuration based on requirement allowing periodic upgrade and enhancement of the system
- modification of sequencing and control procedures for different products are permitted.

chapter-8 / IC Technology

* structural representation of a system generally deals with various components and their interconnections to implement system function.

* IC technology maps the structural representation to physical implementation

* physical implementation

- can be done using methods

- (a) full - custom technology
- (b) semi - custom technology
- (c) Programmable technology

common
methods

* CMOS transistor is one of the core of every components,

CMOS Transistor

- consist three terminals : source, drain and gate.

- source and drain are created by implanting ion on the surface of silicon - creates PN junction.

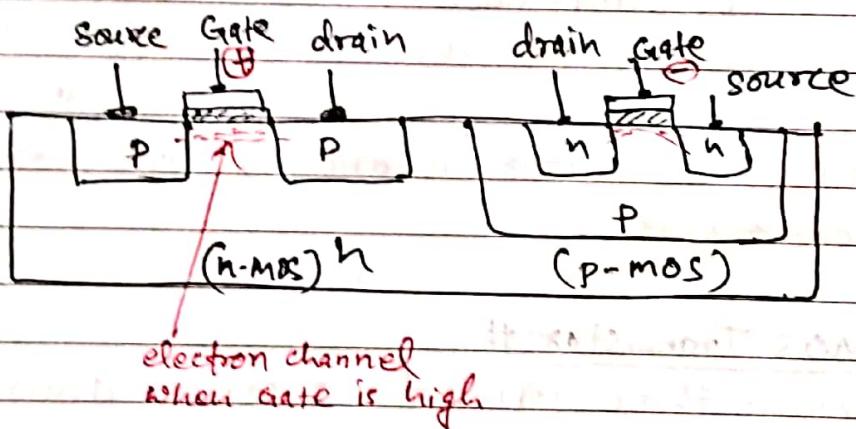
- Gate is formed using poly-silicon, and it lies between source and drain

- poly-silicon is placed on the surface of silicon-oxide layer over silicon; silicon-oxide layer insulates the conduction between poly-silicon layer and silicon (substrate).

- Gate voltage controls the current flow from source to drain.

* In case of nMOS, high voltage at gate will attract electrons from silicon substrate towards it; so, forms conducting channel between source and drain.

* for lower gate voltage conducting channel is thin enough unable to conduct the current from source to drain.



CMOS physical implementation.

Layers in Physical implementation

- transistor basically has three layers

(a) diffusion layer

(b) silicon-oxide layer

(c) polysilicon layer.

- in circuits; there will be number of transistors connected together to represent particular functionality.

- the connections are represented by metal layer
- There can be number of metal layers based on complexity of circuit implemented.
- each metal layer is insulated from other layers with oxide layer.

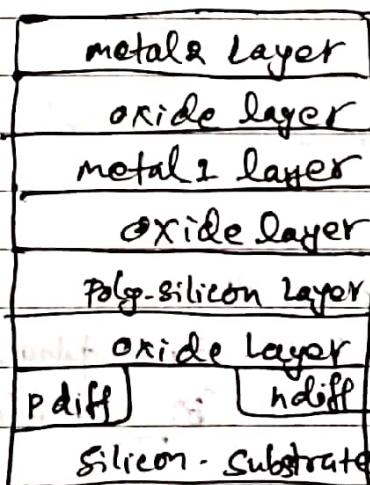
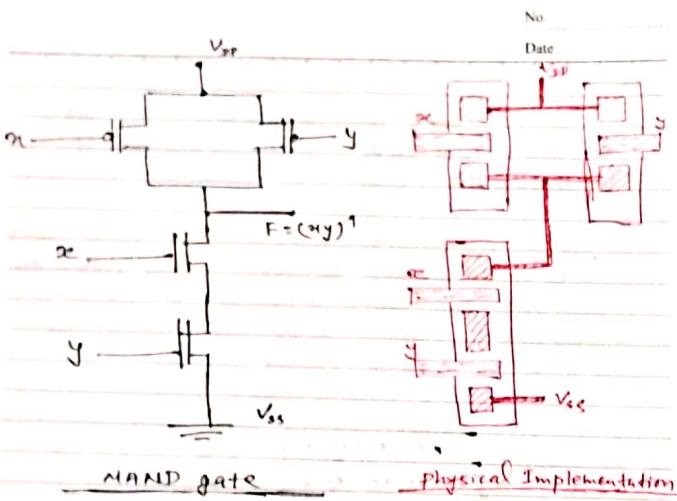


Fig. Basic layers in physical Implementation



IC Manufacturing Process

- can be divided into two phase

(A) Design phase (B) manufacturing phase.

- | | |
|--|--|
| ① → Structural design
② → Layout design | ③ → Mask creation
④ → Wafer creation & cleaning
⑤ → Layering on silicon
⑥ → Ion implantation
⑦ → Metallization
⑧ → Wafer testing
⑨ → Cut out & packaging |
|--|--|

#(A) design Phase

- ① - structural description along with system layout is developed.
- Initially, the behavioral description of the system is implemented in hardware description language (HDL) \rightarrow how system or circuit behaves to the input;
- \times so, highest level of abstraction compared to data-flow level or structural model.
- \times HDL synthesizer tool decides the actual circuit implementation.
- high-level HDL describes the circuit at the register-transistor level (RTL).
- the first step in synthesis process is compilation which converts high-level HDL language into a netlist at gate level.
- the second step is speed and space optimization, which performed on gate level netlist.
- \times netlist is description of connectivity of a circuit.

- ① - the physical layout of the system is generated with the help of place and route software.
- it specifies the placement of every transistor and every wire connecting those transistors.
- \times Electronic Design Automation (EDA) tools are available for circuit synthesis, implementation and simulation.

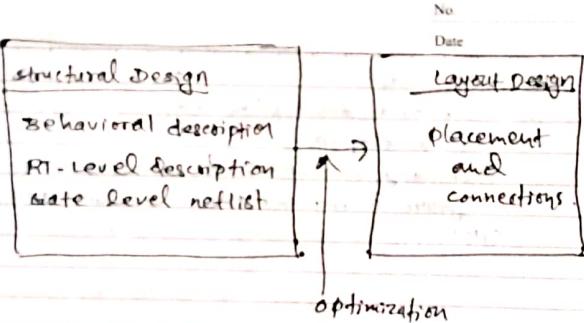


Fig. Design phase in IC manufacturing

(B) Manufacturing phase

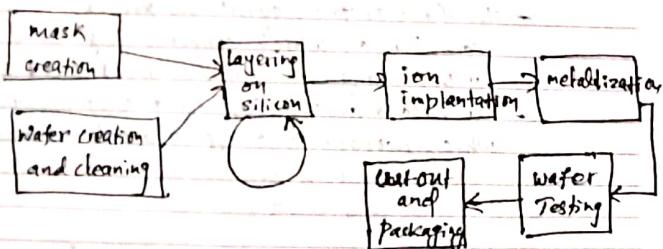


Fig. Manufacturing phase in IC manufacturing.

(1) Mask creation

- the layout of the system is translated into masks.
- the number of masks depends on the number of layers defined by the system complexity.



No. _____
Date _____
layers
- mask for different ~~layers~~ (oxide layer, metal layer etc) are generated.

② Silicon wafer creation and Si cleaning

- high purity silicon is melted in a crucible
- * crucible - is ceramic or metal container in which metal or other substances may be melted to very high temperature
- donor impurity can be added to dope the crystal.
- A seed crystal is dipped into molten silicon and pulled out upwards rotating it.
- cylindrical ingot is extracted by controlling temperature gradient, rate of pulling, and speed of rotation.
- finally the wafer is sliced with wafer saw and polished to form wafers.

* wafer must be cleaned before any layer is deposited on the wafer.

* chemical cleaning (out of various cleaning methods) can be used.

* in chemical cleaning, piranha solution is used.

No. _____
Date _____

- * Piranha solution is hot mixture of hydrogen peroxide and sulfuric acid.
- * Another method of cleaning is use of sonic waves in cleaning solution known as megasonic cleaning process.
- * After cleaning with solution, wafer is rinsed with deionized water.
- * Wafer is dried either using either nitrogen gun or by baking.
- * Spin dry method can also be used.

② Layering on silicon ||

- various layers on silicon surface.
- layer for masks can be created using different layering technique,
- * photolithography
 - uses optical radiation to create pattern.
 - common method in layering process.
 - in this process, layer required is built on to silicon surface overlapped by photoresist.
 - * Positive photoresist becomes soluble when UV rays are exposed on it.
 - Using proper alignment, the UV rays are exposed through the masks which cast a shadow on the photoresist wherever the layer is required.



No. _____
Date _____

- then soluble photoresist is washed using appropriate solvent.
- exposed portion of layer is etched away using chemicals.
- remaining photoresist is removed to expose the regions of the layer that we required in our layer.

④ Ion Implantation

- ions are accelerated at a very high energy and impinged on the target.
- ion energy ranges from several KeV to MeV.
- main purpose of ion implantation is doping in which impurities are added into wafer.
- the process is finalized with annealing process that repairs the lattice damage inflicted by high energy ions.

⑤ Metallization

- thin-film layer is produced which interconnects various circuit elements on the chip.
- it also produces metallized area around the edge of the chip - bonding pads.
- metal film can be deposited by physical vapor deposition (PVD) and chemical vapor deposition (CVD)



No. _____
Date _____

① Wafer testing

- number of ICs are produced which in a ~~is~~ single silicon wafer.
- the ICs are subjected to test for errors or faulty one.
- Tester or wafer probes are equipments used to test the correctness of ICs by inspecting the O/P response for the streams of I/P.

② Chip cutout / packaging

- Individual IC from wafer is cut out using diamond scribe.
- verified IC are mounted in IC package.
- Packaging prevents physical damage and corrosion, supports electrical contact.

No. _____
Date _____

photolithography

- is the process which transfers a pattern from a mask to a light-sensitive chemical photoresist on substrate.

photo — light

litho — stone

graphy — writing

* it uses optical ~~pattern~~ radiation, to create patterns of complex circuit on a wafer.

steps

- ① deposit barrier
- ② photoresist Coating
- ③ soft Bake / Pre Bake
- ④ Mask Alignment and exposure
- ⑤ Develop Photoresist
- ⑥ Hard Bake or Post Bake
- ⑦ Etch window in Barrier Layer
- ⑧ Remove Photoresist

1#) Deposit Barrier Layer

- materials which are required to be laid on substrate.

eg: * silicon dioxide, silicon nitrite, polysilicon, metals.

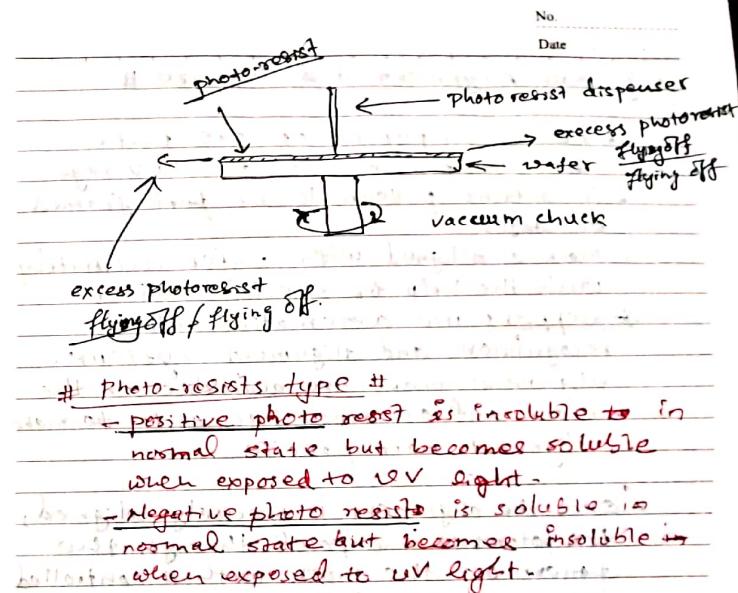
- different methods are available for barrier formation

eg: * thermal oxidation, chemical vapor deposition, sputtering & vacuum evaporation

- silicon dioxide as a barrier layer is used to isolate one layer from another.
- It is used in electrical isolation & multilevel metallization.
- silicon dioxide can be grown using dry oxidation which uses O₂ gas in chamber or wet oxidation in which the wafer is submerged in ~~water~~ water.
- when heat is applied to the oxidation process, it increases the rate of SiO₂ growth.

2#) Photoresist Coating

- is substance which changes its characteristics when exposed to UV light.
- Before the coating, hexamethyl disilazane (HMDS) is used on the surface to improve adhesion.
- then, liquid photoresist is coated over barrier layer using spin coating method.
- In this method, the wafer is held on vacuum chuck which is spun at about 3000-6000 rpm for about 15-30 seconds.
- Appropriate spinner rotational speed and viscosity of resist are essential factors to define photoresist's thickness which is in few micrometers.



3#) Soft Bake or PreBake

- is simply heating process (for resists) which removes the solvent from the photoresist.
- Baking time and temperature depends on the type of photoresist used and baking method.

* different baking method include hot plate, oven baking and microwave baking.

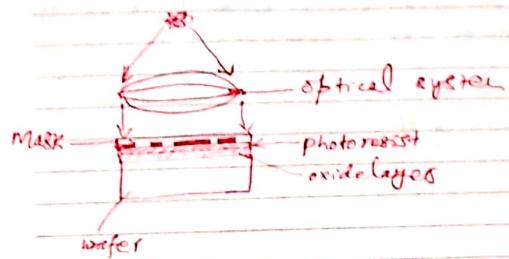
#4) Mask Alignment and Exposure

- mask is simply an opaque plate with estate holes to pass UV rays,
- it contains pattern to be ~~perf~~ formed on wafer.
- Mask is aligned with wafer accurately with the help of special devices:
- * steppers use automatic pattern recognition and alignment systems. alignment masks are available on the mask and on wafer; so, as to to make alignment more precise.
- once the alignment is precisely aligned, the photoresist is exposed through the pattern on the mask with a controlled amount of UV light.
- Exposure will cause exposed positive photoresist to become more soluble whereas if negative photoresist is used then exposed part of it becomes insoluble.

* Three primary exposure methods

- a) contact
- b) proximity
- c) projection

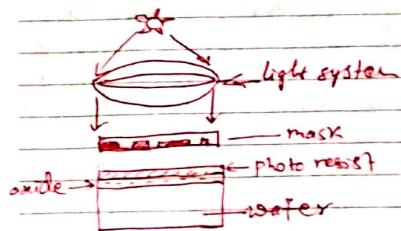
(a) contact Pointing



- resist coated silicon wafer and mask are brought into physical contact when exposed to UV light.

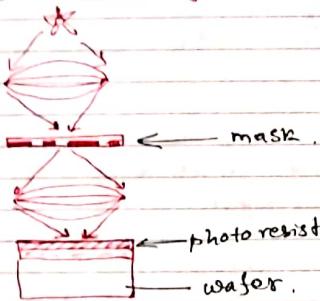
- this method results in very high resolution but the debris, trapped between the resist and the mask, can damage the mask and cause defects in the pattern.

(b) Proximity Pointing



- No _____
Date _____
- In this method, small gap is maintained between waffer and mask during UV exposure.
 - The gap minimizes the risk of mask damage at the expense of resolution.

② Projection Pointing



- An image of the pattern on the mask is projected onto the resist-coated wafer.
- High gap eliminates the risk of mask damage and high resolution is possible.
- * For high resolution, only a small portion of the mask is imaged and stepped over the surface of the wafer.

- No _____
Date _____
- 5#) Develop photoresist #
- * Barrier layer is exposed when the soluble photoresist is chemically washed away using a developer solution.
 - * In immersion develop method, the photoresist-coated wafer is immersed in a developer solution.
 - * Then, it is rinsed with deionized water and dried using spin dry method.

6#) Hard Bake or Post Bake

- Is used to stabilize and harden developed photoresist.
- It not only improves adhesion of the photoresist but also removes the traces of solvent or developer solution.
- Improper post bake can cause resist removal more difficult.
- Baking time and temperature can vary based on the type of photoresist and baking method.

7#) Etch window in Barrier Layer

- As hardened photoresist does not shield all parts of barrier layer, etching method is implanted to remove the barrier layer which was left uncovered.

→

* two methods of etching

(a) wet etch

- also known as
chemical etching

(b) dry etch

- also known as
plasma etching

* In wet etching,

- wafer is submerged in HF acid and
unprotected barrier layer is removed.

$\text{HF acid} \rightarrow \text{hydrofluoric Acid}$

* In dry etching

- plasma used collides with surface
and removes the layer of target
material.

#8) Remove photoresist

- Finally, the remaining photoresist is
stripped from the surface exposing the
required barrier layer.

- Photoresist can be removed by using
solvent strippers, which cause the resist
swell and lose adhesion from the
substrate.

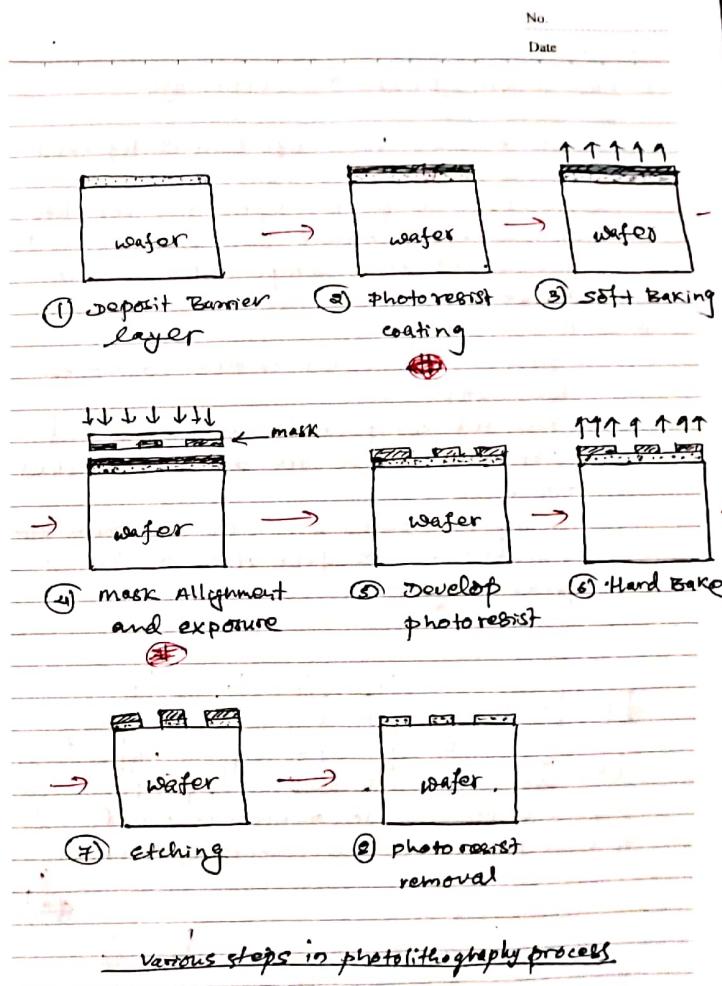
- Another method of photoresist removal
is by burning the resist in an oxygen
plasma system and this process is
called "Resist Ashing".

No _____

Date _____

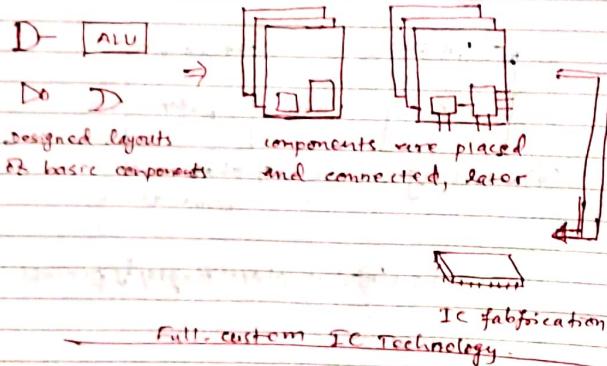
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Date _____



Full-custom (VLSI) IC Technology

- It includes very large scale Integrated circuitry (VLSI) design.
- In VLSI, designer designs the complete transistor-level circuit for every processor, memory and other components used in design.
- * In this technology
 - first the designer creates layouts for basic components.
 - then the components are placed and connected, which are latter translated into mask.
 - finally mask area given to the manufacturer for fabrication of IC of final design.



No.

Date

No.

Date

* placement, routing and sizing are few important physical design task that should be done carefully for an efficient layout design.

* placement - task of placing and orienting the transistors on the IC.

* Routing - task of connecting wires between transistors.

* Sizing - width of each wire along with size of transistor is taken into considerations.

* placement and routing should be done so as to avoid overlapping of transistors and wires.

* placement also defines the length of wire required to connect transistors.

* larger size of wires and transistors provide better performance, but increase power consumption and demands more silicon area in IC.

* compact layout can lead to an efficient design

- closer placement of transistor reduces the length of wire needed to connect and silicon size in the IC.

* Today, automatic physical design tools are used for optimized layout for better performance.

Advantages

④ Excellent efficiency

- with respect to power consumption, performance and size, Full-custom IC technology can be highly efficient.

- Layout design is done by the designer & the components can be placed closer to each other.
- * yields optimum performance, size and power

⑤ No wasted area and unused transistors

- required transistors for the circuits are placed on the IC
- no unused transistors on the IC preventing wasted area.

Disadvantage

- #### ⑥ High NRE cost and long time-to-market
- complete layout design (even with CAD tool) can be time consuming and prone to error
 - additionally, creating mask for every layer of IC adds more time in design process
 - IC manufactured may contain errors, requiring several re-spins
 - this all causes high NRE cost and long time-to-market

semi-custom (ASIC) IC Technology

- designer does not require to create full-custom layout rather connects the pre-positioned building blocks.
- the use of chip with pre-existing gates will lessen the design work and mask creation.
- so, NRE cost is reduced while the time-to-market is relatively fast as compared to full-custom IC Technology
- there will be reduction in performance in terms of power, size and speed.

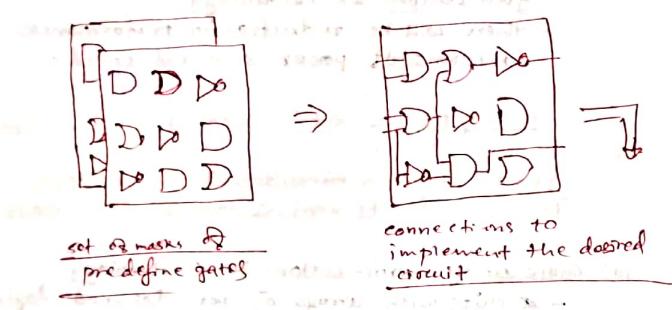
two types of semi-custom IC technology

- (a) Gate Array semi-custom IC Technology
- (b) Standard cell semi-custom IC Technology

(a) Gate Array semi-custom IC Technology

- chips with arrays of pre-designed logic gates are utilized to implement the designed circuit.
- here the masks for transistor and gate levels are already designed, so the designer has the task of connecting present pre-designed gates.
- In this technology, a set of masks of predefined gates are provided to the designer, then designer provides the connections among the gates.

- This technology results in fast and relatively inexpensive design cycles.
- use of gate array placed in advance may result in many unused gates.
- fixed placement of gates can result in long routing wires between gates as connections is not known while gates are placed in advance without knowing circuit design required.

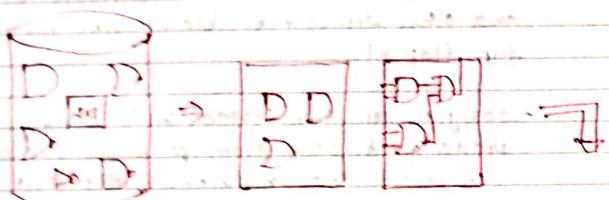


which step is the next stage of IC fabrication.
implies that the layout process is done
earlier and optimization is done with each
step. which leads to better performance
and efficiency. so the next step is to
make the interconnects using thin film
technology. which will connect
different regions with gates and buses.

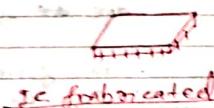
- No. _____
Date _____
- (b) standard cell semi-custom IC technology
- In this technology, functional blocks are utilized in the design to achieve high gate density and good electrical performance.
 - * functional blocks are also known as cells with known electrical properties.
 - cells may include as NAND, NOR etc and other functional blocks like multiplexor flip-flop etc.
 - designers are facilitated with library of predesigned cells from which the designer can select the required cells that are needed in the desired circuit.
 - masks of cells are created after the cells are placed and connected. Also the masks of connections among cells are generated.
 - the generated cell masks are used for IC fabrication.
 - * the designer selects the cell, its position and routing mechanism.
 - * so, it requires more NRE cost and longer time-to-market as compared to gate array technology but still requires less than that of full custom.
 - * However, efficiency is better compared to gate array but less efficient than full-custom.

No. _____
Date _____

Hence, standard cell design lies between gate array and full custom design in terms of NRE costs, time to market and performance.



Library with placement and connection predefined among cells, those masks are generated



IC fabricated

No. _____ Date _____

Programmable Logic Device (PLD) Technology

- In programmable logic device IC technology, there exist programmable circuits which are programmed by the designer to implement the required design.
- Programming means either creating or breaking connection between nodes that connects gates, either by blowing a fuse with high current or setting a bit in a programmable switch.
- In this technology, pre-fabricated chip with no logic function programmed is made available to the designer who programs the required portion of the chip to implement the desired functionality.

* it offers the facility of changing design functions even after it has been programmed.

* PLD can be programmed, erased and reprogrammed number of times, allowing easier prototyping and design modification.

* There is a wide variety of PLD types

- a) Simple PLD
- b) Complex PLD
- c) GAL (Generic Array Logic)
- d) FPGA (Field-programmable Gate array)

II Simple PLD

- (1) programmable logic array (PLA)
- (2) Programmable Array logic (PAL)

PLA

* PLA consists of two planes of logic arrays:

- (a) programmable array of AND gates.
- (b) programmable array of OR gates.

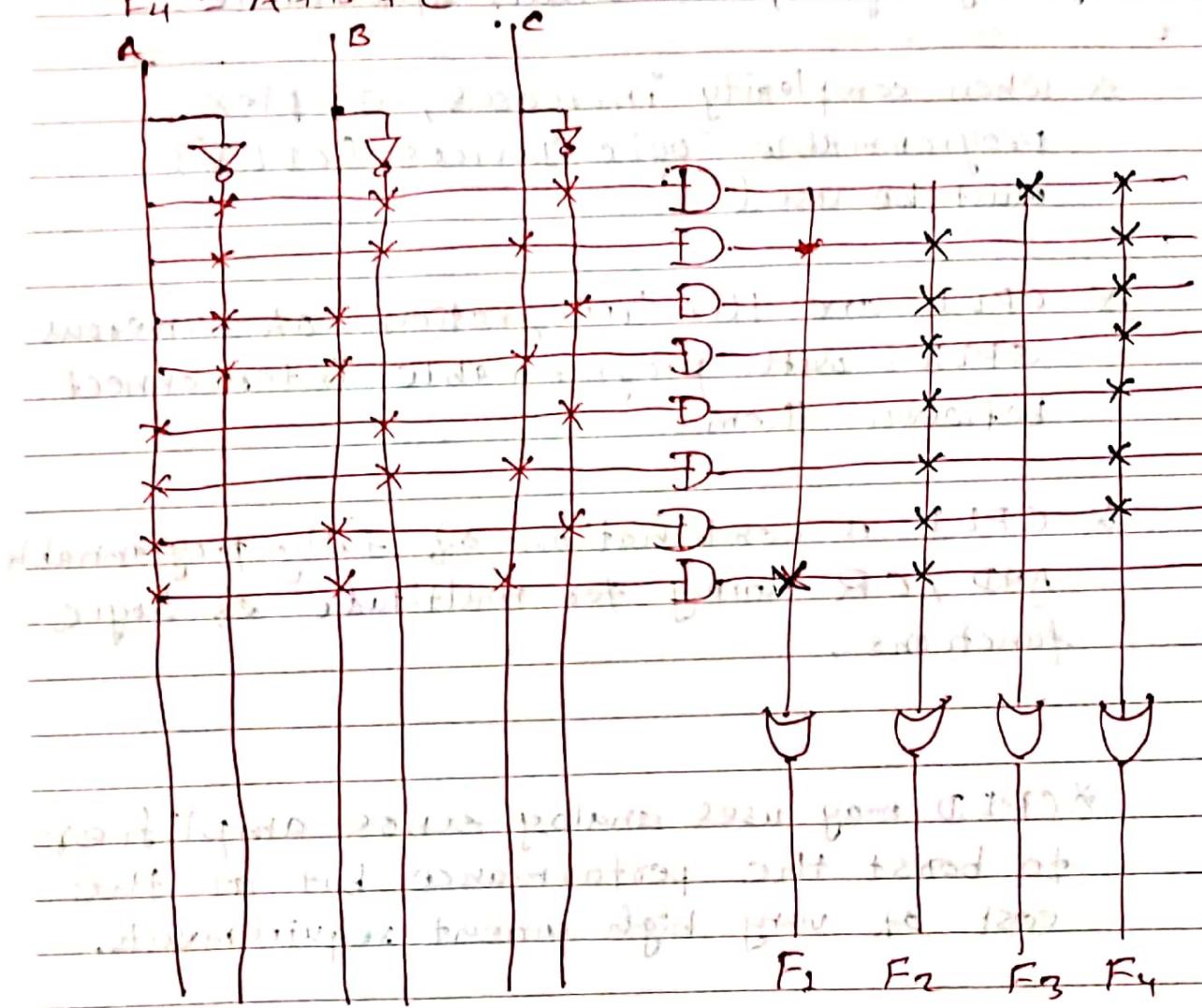
* Every AND gate in AND plane is associated with inputs and complement of inputs to generate any product term.

* OR gate plane generates the sum of AND gate output

Example of PLA

A	B	C	F_1	F_2	F_3	F_4
0	0	0	0	0	1	1
0	0	1	0	1	0	1
0	1	0	0	1	0	1
0	1	1	0	1	0	1
1	0	0	0	1	0	1
1	0	1	0	1	0	1
1	1	0	0	1	0	1
1	1	1	1	1	0	0

$$F_1 = ABC + \bar{B}C, F_2 = A\bar{B} + \bar{B}C, F_3 = \bar{A}\bar{B}'C, \\ F_4 = \bar{A}B + \bar{B}'C$$



PA1

- uses just one programmable array
- (a) fixed OR matrix and programmable AND matrix.
- reduces the programmable components reducing size and delay.

PLA and PAL are low-complexity with fairly high speed circuit applicable.

- * When complexity increases, complex programmable logic Devices (CPLD) must be used.
- * CPLD are the integration of numerous SPLDs with programmable interconnect between them.
- * CPLD is combination of fully programmable AND / OR array for multitude of logic functions.
- * CPLD may use analog sense amplifier to boost the performance but at the cost of very high current requirements.

VHDL - (chapter no.)

- very high speed Integrated circuit Hardware Description language (VHDL)
- describes the behavior of an electronic system.
- It further enables designer to implement physical system.

* The main purpose of VHDL

- to model and synthesize digital circuit.
- simulation and testing of design for optimal operation.

* VHDL code is used to create actual functional system.

* So, VHDL is used either to implement the circuit in a programmable device or can be forwarded for IC fabrication.

VHDL invariants

- case insensitive
- insensitive to white space
- comments with two consecutive dashes "--".
- parenthesis usage is option in many cases.
- All the statements in VHDL are terminated with semi-colon.

No.

Date

VHDL code structure

- VHDL code comprises of at least three fundamental sections:
 - (a) Library Declaration,
 - (b) Entity
 - (c) Architecture

(a) Library declaration

- Library is collection of pre-defined set of codes that can be re-used or shared by various designs.

(b) Entity

- specifies the I/O connections of the system.

(c) Architecture

- contains the code that describes how the circuit should function.

Library Declaration

* The general form is
library library-name;
use library-name.package-name;
package-parts;

Eg: library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

No.

Date

Entity

- The VHDL entity declaration describes the interface or the external representation of the circuit.
- Lists all input and output pins with specification such as data type and data direction mode.

Eg: Entity entity-name is

port (port-name : signal-mode signal-type
port-name : signal-mode signal-type)

* entity-name and port-name are identifier.

* signal-mode defines the direction of signal ie in, out, inout or buffer.

* signal-type can be BIT, STD_LOGIC, INTEGER etc.

Ex:

```
# Entity AND_Gate is
port ( in_A : in STD_LOGIC;
       in_B : in STD_LOGIC;
       out_Z : out STD_LOGIC
      );
```

End AND_Gate;

```
# Entity mux is
```

```
port ( A,B,C,D : in std_logic_vector(2 downto 0);
       sel : in std_logic_vector(1 downto 0),
       Z : out STD_LOGIC
      );
```

End mux;

Architecture

- describes how the circuit should function.
- describes the internal implementation of the associated entity.

The general form of architecture is

```
Architecture architecture_name OF entity_name  
  is  
    [Declaration]  
    Begin  
      [Code]  
    End architecture_name;
```

Data types, Data Objects and Operators

- VHDL contains a series of predefined data types.
- Such data type definitions can be found in various packages or libraries.

* Package standard STD includes BIT, Boolean, Integer's and real.

* Package std_logic_1164 IEEE includes std_logic and std-logic.

Date

Date

User defined data type

- VHDL allows users to define their own data type

- ① user defined integer type
- ② user defined enumerated Type

③

Type temperature is range -125 to 125;

Type marks is range 0 to 100;

* General form

Type type_name is range low_value to high_value;

④ Type color is (Red, Green, Blue, White);

* General form

Type type_name is (value1, value2, ..., valuen);

Data object

- object is an item in VHDL which has both name and a specific type.

* Common data objects are : signals, variables and constants.

Constants

- used to assign default values in the code.
- it can be declared in package, entity or architecture.

* **PA**

- * constant declaration in package make it global.
- * Constant declaration in entity makes the constant available for all architecture.
- * when defined within architecture the scope is limited to that architecture only.

Declaration

```
constant name : Type := value;
eg: constant high : std_logic := '1';
      constant count : integer := 10;
```

Signal

- is used to pass value in and out of the circuit and within internal units.
- It simply represents interconnection of circuit.

* all ports of entity are signals by default.

* the change in signal may not be updated immediately, since value is likely to get updated after the completion of its corresponding process, function or procedure.

* similar to constant, it can be declared in package, entity or architecture.

Declaration:

```
signal name : type [range] [:= initial value];
eg signal start : std_logic := '0';
Signal count : integer range 0 to 100;
```

Note: the part inside the square bracket may or may not be present depending upon datatype used and requirement.

①

Variables

- represents the local information.
- its value can not be passed out directly.
- changed value is updated immediately.

it new value can be promptly used in next line of code.

it It can be declared and used inside process, function or procedure.

Declaration

```
variable name : type [range]  
[ := initial_value];
```

e.g: variable count : integer := 0

variable a : std_logic_vector(7 downto 0);

Operators

(a) Assignment operator

$a \leftarrow b$ — value of b assigned to a

$a := '0'$ — a is initialized to zero

$a \Rightarrow b$ — value of a is assigned to b

(b) Logical operators

NOT, AND, OR, XNOR, NOR

(c) Relational operators

"=" → equal to;

" \neq " → not equal to;

"<" → less than;

" \leq " → less than equal to;

" \geq " → greater than equal to;

(d) Arithmetic operators

"+" → addition

"-" → subtraction

"*" → multiplication

" $/$ " → division

" $**$ " → exponentiation

MOD → modulus

REM → remainder

ABS → absolute value.

c) Shift operators

SLL → shift left logic

SRL → shift right logic

SLA → shift left arithmetic

SRA → shift right arithmetic

ROL → Rotate Left

ROR → Rotate right,

Note: in shifting zero are fed to other end and bits in other end are lost.

In arithmetic shifting, sign bit never changes.

concatenation operator

- the operator is &

- used to combine values of similar data type.

Eg: signal A, B : std_logic_vector (8 downto 0);
 signal C : std_logic_vector (5 downto 0);
 signal D : std_logic_vector (7 downto 0);

C <= A & "00";

D <= B & A;

Behavioral style Architecture

- it models how the circuit outputs will behave to the circuit inputs.
- it may not reflect how the circuit is implemented when it is synthesized.

* process statement is the core part of behavioral style architecture.

* internal working is implemented using sequential statements within process statements.

structural style Architecture

- is modular approach to coding.
- it supports hierarchical design which helps to understand complex digital system design.
- modular designs enhance understandability by combining low-level functionality into modules.
- these modules can be reused in different designs resulting in save of design time.
- It might not be efficient for ~~simple~~ simple digital system while easy and efficient design style for complex digital system design.