

POKHARA UNIVERSITY

Level: Bachelor

Programme: BE

Course: Computer Architecture

Semester: Fall

Year : 2023

Full Marks: 100

Pass Marks: 45

Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a) How computer architecture differs from computer organization? 7
✓ Explain future trends in computer system.
- b) What are the uses of shift micro-operations in computer arithmetic? 8
✓ Explain the register transfer micro operations between two 4-bit register via bus connection provided that certain condition is true.
2. a) Illustrate the concept of register organization and explain the registers involved. 8
- b) What is Booth's algorithm? Use the algorithm for binary multiplication of $(-1)_{10}$ and $(13)_{10}$. 7
- a) Explain with example to implement hardwired control unit with its logic. 7
- b) How single address, two address and variable format differ from each other? Explain in detail. 8
- a) What are the pros and cons of direct mapping? Explain direct mapping techniques with necessary diagram. 8
- b) What is content addressable memory? Explain about address matching logic in CAM? 7
- a) What is a pipelining? Differentiate between RISC and CISC pipelining. 7
- b) What is register renaming? How does register window in RISC processor handle subroutine call and return inside CPU itself? Illustrate with example. 8
- a) How parallelism occurs in uniprocessor system? What is the inter-connections structure possible in multiprocessor system? 8
- b) What are the hardware and software performance issues that arise in multicore organization? 7

7. Write short notes on: (Any two)
- Floating point representation
 - Instruction pipelining
 - Horizontal and vertical microinstruction set

2x5

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Page 2 of 2

POKHARA UNIVERSITY

Level: Bachelor
Programme: BE
Course: Computer Architecture

Semester : Spring

Year : 2023
Full Marks: 100
Pass Marks: 45
Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a) Differentiate between Computer Organization and Computer Architecture. Explain the functional view of the computer with reference to each component. 8
- b) Define RTL. Explain about Bus and Register transfers in RTL. 7
2. a) Explain different types of registers used in Computer System with examples. What is the use of registers in Computer System? 7
- b) Perform $-15 * 6$ using Booth's algorithm. 8
3. a) Explain the restoring division algorithm with flowchart. 8
- b) Explain the working principle of Micro-programmed implementation of control unit. Why is it slower than Hardwired Control Unit? 7
4. a) What is associative memory? How read /write operation takes place in associative memory? 7
- b) As we know cache memory size is smaller than main memory, how is it possible to map main memory data into cache memory? Explain in detail. 8
5. a) How Interrupt driven I/O differ from programmed I/O? Explain with necessary diagram. 7
- b) How instruction pipelining supports in parallelism? Explain. 8
6. a) Cache coherence problem arise in multiprocessor system and must be resolved. Justify this statement. 8
- b) What are the performance issues that arise in multicore computers? 7

Write short notes on: (Any two)

- a) Control unit.
- b) RISC VS CISC
- c) Flynn's Classification

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POKHARA UNIVERSITY

Level: Bachelor
Programme: BE
Course: Computer Architecture

Semester: Fall

Year : 2022
Full Marks: 100
Pass Marks: 45
Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a) Discuss the term Computer Architecture. Explain IAS computer architecture with detailed diagram. 8
 - b) Define addressing mode. Explain different addressing modes with appropriate figures and example of each. 7
 2. a) Define RTL. How data can be transferred between registers. Explain. 8
 - b) Define Instruction cycle. What are the different states in an instruction cycle? Also explain fetch cycle, decode cycle, execute cycle and indirect cycle. 8
 3. a) Draw the flowchart for Booth's Algorithm. Use the algorithm for binary multiplication of (-12) and (-9). 8
 - b) Explain single and two address field sequencing techniques in micro programmed control unit. 7
 4. a) Differentiate between Hardwired and Micro-programmed control unit. Explain the logic of Hardwired unit. 7
 - b) What is memory hierarchy? Explain with reason why do we need multilevel memory hierarchy? 7
 5. a) Explain various communication techniques for I/O devices. 8
 - b) Differentiate between various mapping techniques when main memory data is to be mapped into cache memory. 7
 6. a) What is power efficient processor? Explain dual core processor with respect to quad core processor. 8
 - b) Describe in brief about Flynn's Taxonomy. Also explain how parallelism can be experienced in uniprocessor systems. 7
 7. Write short notes on: (Any two) 2×5
- a) RISC vs. CISC
 - b) Vector processors and Array processors
 - c) BCD Adder

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POKHARA UNIVERSITY

Level: Bachelor

Semester: Spring

Year : 2021

Programme: BE

Full Marks: 100

Course: Computer Architecture

Pass Marks: 45

Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

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|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---|
| 1. a) | What are the major differences between Computer Architecture and Computer Organization? Explain about different categories of micro operations. | 6 |
| b) | What is addressing mode? Write Codes to evaluate $X = (A-B^*F)^*C+D/E$ using three, two, one and zero address instruction formats. | 9 |
| 2. a) | Define data path. What are the design principles for modern CPU system? | 7 |
| b) | Explain Booth's algorithm with example of your own. | 8 |
| 3. a) | Draw the circuit for BCD adder. Explain floating point representation. | 7 |
| b) | Distinguish hardwired control unit and micro programmed control unit with suitable example of each. | 8 |
| 4. a) | Explain about Associative mapping technique. Why replacement algorithm is required in associative mapping technique? | 7 |
| b) | Describe the drawbacks of Programmed I/O and interrupt driven I/O and explain how DMA overcomes these drawbacks. | 8 |
| 5. a) | What is hit ratio in cache memory? Mention the advantages and disadvantages of various cache mapping techniques. | 8 |
| b) | Differentiate between RISC and CISC pipelining. | 7 |
| 6. a) | Differentiate between multi computer and multiprocessor system. List out various multiprocessor interconnection structure. How does the cache coherence problem arise in multiprocessor system? Explain with example. | 8 |
| b) | Show that the speedup factor for pipelined processor is equal to the number of stages in a pipeline. | 7 |

POKHARA UNIVERSITY

Level: Bachelor

Semester: Fall

Year : 2021

Programme: BE

Full Marks: 100

Course: Computer Architecture

Pass Marks: 45

Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a) Define Computer Architecture and Computer Organization. What is HDL and what are its advantages? 6
b) What is addressing mode? Explain about different types of addressing modes. 9
2. a) What is CPU organization? Explain register organization in details. 8
b) What is ALU? Design a 2-bit ALU that can perform AND, OR & ADD operations. 7
3. a) What is Booths algorithm in computer Architecture? Explain 8
b) What is associative memory? How read write operation is performed in associative memory? 7
4. a) Draw the block diagram of micro programmed control unit and explain it. 6
b) What the drawbacks are of interrupt driven and programmed I/O? 9
How DMA overcomes it? Explain.
5. a) Explain DMA transfer in a Computer system with necessary diagram. 6
b) Compare RISC and CISC Architecture. Describe Flynn's classification. 9
6. a) Show that the speedup factor for pipelined processor is equal to the number of stages in a pipeline. 7
b) What is cache mapping? Explain cache replacement algorithm with a suitable example. 8

POKHARA UNIVERSITY

Level: Bachelor
Programme:BE
Course:Computer Architecture

Semester: Fall

Year : 2020
Full Marks: 100
Pass Marks: 45
Time : 3 hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a) Differentiate Computer Organization and architecture. Explain the various addressing modes. 8
- b) Define RTL. Explain about BUS and Memory trans ferrin RTL. 7
2. a) Explain different types of registers used in computer system. What is use of register in computer system? 7
- b) Perform multiplication -13*7 using Booth's Algorithm. 8
3. a) What are the various number representation method in computer system? 7
- b) Explain block diagram of micro programmed control organization and write down its advantages. 8
4. a) Explain associative and set-associative mapping in cache memory? 8
- b) Define an interrupt with its classes in detail. Also explain about interrupt driven I/O. 7
5. a) What is pipelining hazards? Explain structural and data hazard and its solution 7
- b) What is cache coherence problem? Explain software and hardware solution of cache coherence problem. 8
6. a) Write about parallelism in computer system. Explain about symmetric multiprocessor in detail. 7
- b) Explain about the various Hardware Performance issues in Multicore Computers. 8

POKHARA UNIVERSITY

Level: Bachelor

Semester: Spring

Year : 2019

Programme: BE

Full Marks: 100

Course: Computer Architecture

Pass Marks: 45

Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a) Explain the different evolutionary milestones in development of computer system. 7
b) What are the different types of register used in computer system, explain with examples. 8
2. a) Write the algorithm and perform multiplication of 9*-3 using booth algorithm. 8
b) Differentiate between micro programmed control and hardwired control unit? What are the techniques used to sequence microinstructions. 7
3. a) What is instruction cycle? Explain various sub cycle of instruction cycle with micro-instructions involved in each sub cycle. 8
b) Define virtual memory. Explain address mapping using pages in virtual memory. 7
4. a) Explain how redundancy is obtained in RAID, with reference to any two RAID levels. What is the application of RAID? 8
b) Explain with an example, how effective address is calculated in Direct, Register indirect, Relative and Index addressing modes. (Assume necessary data if you need) 7
5. a) What is mean by pipelining? Explain in brief about RISC pipelining? 7
b) What is cache coherence problem? Explain methods of solving cache coherence problem. 8
6. a) What are the various interconnected structure used for multiprocessor system? Explain them. 7
b) Briefly explain the different performance issues in Hardware. 8
7. Write short notes on: (Any two) 2x5
 - a) Register Transfer language (HDL)
 - b) Future trends in computer
 - c) Instruction pipelining

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a) Explain the functional view of the computer system with reference to each component.
b) How data can be transferred between registers? Explain in detail.
2. a) Describe the arithmetic and logic circuit with its appropriate block diagram.
b) Multiply $(14)_{10}$ and $(3)_{10}$ using unsigned binary multiplication method with data flow diagram.
3. a) Perform $(-5) * (-3)$ using the Booth multiplication algorithm.
b) Compare single and two address field addressing techniques used in micro-programmed implementation of control unit.
4. a) Does hardwired implementation of Control Unit makes control unit fast or slow explain? Mention disadvantages of Hardwired implementation.
b) What is associative memory? How match logic works for associative memory?
5. a) Define DMA. Explain DMA controller with different DMA transfer modes.
b) Explain the advantages of pipelining in the multiprocessor system. Describe the instruction pipeline with examples.
6. a) Why cache coherency occur in multiprocessor system? What are the various ways to troubleshoot the problem?
b) Explain Flynn's classification of computer system.
7. Write short notes on: (Any two)
 - a) Optical disk
 - b) RISC Vs CISC
 - c) Multi Core Organization

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

- | | | |
|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---|
| 1. a) | What are the characteristics of computer system? Draw and explain the basic computer organization in detail. | 8 |
| b) | What is RTL? Explain it when data transfer takes place between one and four bit register. | 7 |
| 2. a) | How a floating point number is represented in computer system? Verify the operation $(9) \times (-2)$ using signed magnitude data | 8 |
| b) | What is sequencer? Draw and explain the micro programmed control unit in detail. | 7 |
| 3. a) | What is instruction cycle? Write the necessary micro-operations for fetch, decode, indirect and interrupt cycles. | 8 |
| b) | What is mapping? What are the different cache memory mapping technique? | 7 |
| 4. a) | What is DMA? Explain why DMA is used instead of interrupt driven and programmed I/O? | 7 |
| b) | What is instruction pipeline? Explain 3-segment instruction pipelining used in RISC computer. | 8 |
| 5. a) | How a computer system can be classified according to Flynn's? Design an arithmetic pipeline to speed up the computer to solve the expression $A_i * C_i + D_i$ for $i=0, 1, 2, 3, 4$. | 8 |
| b) | What are the function of ISR? Explain how interrupt are processed in computer system. | 7 |
| 6. a) | How floating point number can be added or subtracted using pipelining techniques? | 8 |
| b) | What are different interconnection structure when there are multiple | 7 |

Year : 2018
Full Marks: 100
Base Marks: 42
Date : 3/12/2018

QUESTION PAPER - II

CPUs?

7. Write short notes on: (Any two)

- a) Alternative Chip Organization
- b) Types of registers
- c) Control memory organization and mapping logic

POKHARA UNIVERSITY

Level: Bachelor	Semester: Fall	Year : 2018
Programme: BE		Full Marks: 100
Course: Computer Architecture		Pass Marks: 45

Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a) Explain different stages of computer evolution with reference of generation of computer. 7
- b) Explain instruction cycle state diagram with interrupt. 8
2. a) How overflow be detected in computer? Verify the operation (7) / (-3) using signed 2's complement method. 8
- b) Compare and Contrast between micro-program and hardwired control unit. Explain the micro program sequencer with example. 7
3. a) What is interrupt cycle? Explain how instruction be processed with interrupt in computer along with necessary diagram. 8
- b) What is m-way interleaving? Explain different types of memory interleaving. 7
4. a) Consider a system with main memory (MM) consisting of 8K blocks, a cache memory consisting of 256 blocks and a block size of 16 words- what will be the word field, block filed and Tag field length? How many bits are there in main memory address? If the system uses direct mapping and associative mapping techniques. 8
- b) What are the drawbacks of programmed I/O and interrupt driven I/O? Explain how DMA overcomes those drawbacks. 7
5. a) Assume that pipeline has K=8 segment and execute n=125 tasks in sequence. Let the time taken to process a sub-operation in each segment is 30 sec. Calculate the speed up ratio in the pipeline. 8
- b) What type of hardware and software performance issues are seen in multi-core computers? Explain. 7

6. a) Explain different interconnection structures in multiprocessors. 8
b) What is cache coherence problem? Explain MESI protocol for solving cache coherence problem. 1
7. Write short notes on: (Any two) 2x5
- a) RISC vs. CISC
 - b) Hardware Description language (HDL)
 - c) Logic Microoperation

**Level: Bachelor
Programme: BE
Course: Comput**

Semester: Spring

Year : 2011
Full Marks: 100
Pass Marks: 45
Time : 3 hrs

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

- | | | |
|----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|
| 1. | a) What is stored program concept, explain with reference to IAS computer.
b) What is register in computer system? Explain different types of registers used in computer system. | 7
1+7 |
| 2. | a) Perform multiplication of -5×2 .
b) Explain working principle of micro-programmed implementation of control unit. Why it is slower than hardwired implementation of control unit. | 7
6+2 |
| 3. | a) Explain single address field and two address field sequencing techniques used in micro-programmed implementation of control unit.
b) What is associative memory? Explain hardware organization of associative memory. | 7
2+6 |
| 4. | a) How redundancy is achieved in RAID, explain with any two RAID levels.
b) Explain the Input output module in computer system along with its block diagram, also write its importance. | 8
5+2 |
| 5. | a) Mention the need of use of large register file in RISC. Explain overlapping register windows in RISC with example?
b) What is pipelining hazards? Explain structural and data hazard with solutions. | 7
8 |
| 6. | a) Explain Flynn's classification, along with its general block diagrams.
b) What is cache coherence? Explain any two methods of solving cache coherence problem. | 7
2+6 |
| 7. | Write short notes on: (Any two)
a) Memory hierarchy
b) Register Transfer Language (RTL)
c) Dual core and Quad core processors | 2x5 |

POKHARA UNIVERSITY

Level: Bachelor
 Programme: BE
 Course: Computer Architecture

Semester: Fall

Year : 2017
 Full Marks: 100
 Pass Marks: 45
 Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a) The terms "computer architecture" and "computer organization" are same or different, explain with examples. 7
- b) Define RTL. Describe different types of Shift micro-operations. 8
2. a) What is instruction cycle, explain instruction cycle state diagram with interrupt. 7
- b) Multiply using Booth's Algorithm: $(-11)_{10} * (15)_{10}$ 8
3. a) Describe ac algorithm used for the division of signed numbers. Find the result of $(-9)_{10}$ divided by $(2)_{10}$ using same algorithm. 8
- b) Explain hardwired implementation of control unit. List out advantages of using hardwired control unit. 7
4. a) What is micro instruction sequencing? Explain single address field and variable format sequencing techniques used in micro-programmed implementation of control unit. 7
- b) How can use of cache memory improve performance in any computer system? Explain set-associative and direct mapping in cache. 8
5. a) Define locality of reference. Differentiate between Static and Dynamic RAM. 7
- b) Define DMA. Explain DMA transfer modes. 8
6. a) Compare RISC and CISC systems. 7
- b) What is cache coherence problem? Write the methods used in solving the problem. 8
7. Write short notes on: (Any two)
 - a) Multi-core organization
 - b) Parallelism in Uniprocessor System
 - c) Register windows

POKHARA UNIVERSITY

Level: Bachelor
Programme: BE
Course: Computer Architecture

Semester: Fall

Year : 2016
Full Marks: 100
Pass Marks: 45
Time : 3 hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a) Define Computer Organization and what are the instruction used in IAS computer explain each in detail. 8
b) Explain instruction cycle state diagram with interrupt. 7
2. a) Compute $(7)_{10} \times (-3)_{10}$, where numbers are represented by 2's complement representation 8
b) Explain how hardwired control unit is implemented, with appropriate block diagrams. 7
3. a) Define cache. Explain set associative mapping with necessary diagrams. 7
b) Define cache miss. Describe cache read operation with flowchart. 8
4. a) Define External Interfaces. Explain how DMA improves the limitations of Interrupt Driven I/O. 8
b) How Instruction pipelining can increase system performance? A non pipeline system takes 50ns to process a task. The same task can be processed in a six segment pipeline with clock cycle of 10ns. Determine the speed up ratio of the pipeline for 100 tasks. What is the maximum speedup that can be achieved? 7
5. a) Mention the need of use of large register file in RISC. Explain overlapping register windows in RISC with example? 7
b) Explain different interconnection structures in multiprocessor systems. 8
6. a) What is cache coherence problem? Explain MESI protocol approach for the solution of this problem. 7
b) Explain different types of hardware and software performance in multicore computers. 7

POKHARA UNIVERSITY

Level: Bachelor

Semester: Fall

Year : 2016

Programme: BE

Full Marks: 100

Course: Computer Architecture

Pass Marks: 45

Time : 3 hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a) Define Computer Organization and what are the instruction used in IAS computer explain each in detail. 8
b) Explain instruction cycle state diagram with interrupt. 7
2. a) Compute $(7)_{10} \times (-3)_{10}$, where numbers are represented by 2's complement representation 8
b) Explain how hardwired control unit is implemented, with appropriate block diagrams. 7
3. a) Define cache. Explain set associative mapping with necessary diagrams. 7
b) Define cache miss. Describe cache read operation with flowchart. 8
4. a) Define External Interfaces. Explain how DMA improves the limitations of Interrupt Driven I/O. 8
b) How Instruction pipelining can increase system performance? A non pipeline system takes 50ns to process a task. The same task can be processed in a six segment pipeline with clock cycle of 10ns. Determine the speed up ratio of the pipeline for 100 tasks. What is the maximum speedup that can be achieved? 7
5. a) Mention the need of use of large register file in RISC. Explain overlapping register windows in RISC with example? 7
b) Explain different interconnection structures in multiprocessor systems. 8
6. a) What is cache coherence problem? Explain MESI protocol approach for the solution of this problem. 7
b) Explain different types of hardware and software performance issues in multicore computers. 8

7. Write short notes on: (Any two)
- a) Register Transfer language (RTL)
 - b) Dual and Quad Core Processor
 - c) Addressing Modes

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COMPUTER ARCHITECTURE

Level: Bachelor	Semester: Spring	Year : 2016
Programme: BE		Full Marks: 100
Course: Computer Architecture		Pass Marks: 45
		Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a) Write codes for the operation $Y = (A + B * C) / (E - F)$ using 3 -, 2 -, 1 - and 0 - address instruction format. 8
- b) Write RTL for fetch, indirect and interrupt cycles. 7
2. a) Describe the basic ALU with its functional block diagram and operational truth table. 7
- b) Draw Booth multiplication algorithm and perform multiplication between 5 and -6. 8
3. a) Design 2 bit array multiplier using combinational logic. 7
- b) Explain the operation of microprogram sequencer used in microprogramming CU with its block diagram. 8
4. a) Draw memory hierarchy with their relative characteristics and differentiate between SRAM and DRAM. 8
- b) Describe the principle of associative cache mapping with its merits and demerits. 7
5. a) Explain DMA with flowchart and interconnection of DMA controller with processor, memory and I/O devices. 7
- b) Explain the major characteristics of CISC with its shortcomings. 8
6. a) Describe different interconnection structures in multiprocessor system. 8
- b) Describe hardware performance issues in multicore computer. 7
7. Write short notes on: (Any two) 2x5
 - a) Hardwired CU
 - b) Array Processor
 - c) Control Hazard in Instruction Pipeline

POKHARA UNIVERSITY

Level: Bachelor
Programme: BE
Course: Computer Architecture

Semester: Spring

Year : 2015
Full Marks: 100
Pass Marks: 45
Time : 3 hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a) Differentiate between Computer Architecture and Computer Organization with example. 8
- b) What are the different registers used for storage and data transfer in CPU? 7
2. a) Perform 7/3 division using unsigned binary division. 8
- b) Explain arithmetic pipelining with examples. 7
3. a) Explain how single address, two address and variable format differ from each other? 8
- b) Define mapping function. Briefly explain the Set-associative mapping technique. 7
4. a) What are the limitations of programmed I/O, how these are improved in interrupt driven I/O, and how the limitations of interrupt driven I/O are improved by DMA. 7
- b) Instruction pipelining increases system performance without increasing processor number, explain how? 4
- c) What are Pipelining hazards and how can these be removed? 4
5. a) Assume that pipeline has K=6 segment and execute n=120 tasks in sequence. Let the time taken to process a sub-operation in each segment is 30 sec. Calculate the speed up ratio in the pipeline. 7
- b) Define parallelism? Draw different interconnection structure of multiprocessor system and describe it with necessary diagram. 7
6. a) Explain different types of hardware performance issues in multicore computers. 7
- b) What is cache coherency and how can they be removed? 7
7. Write short notes on: (Any two)
 - a) BCD Adder
 - b) Dual Core and Quad Core Processors
 - c) VHDL

POKHARA UNIVERSITY

Level: Bachelor
Programme: BE
Course: Computer Architecture

Semester: Fall

Year : 2015
Full Marks: 100
Pass Marks: 45
Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

Computer transfer in 8

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1. a) Differentiate between Computer Architecture and Computer Organization. Explain the term SSI and VLSI. 8
- b) Define RTL. Describe different types of Shift micro-operations. 7
2. a) Define Instruction Set? Explain the basic component used in register organization. 7
- b) Divide (8) by (3) using 2's complement division. 8
3. a) How floating point arithmetic operations are performed using binary numbers? Give an example. 7
- b) Differentiate between Hardwired and Micro-programmed control unit. Explain the logic of Hardwired unit. 8
4. a) Differentiate between direct, associative and set associative mapping technique. 8
- b) Define cache miss. Describe cache read operation with flowchart. 7
5. a) Compare Programmed I/O and Interrupt Driven I/O. How does DMA overcome the problems of both these techniques? 8
- b) Which instruction set computers are used in today's world? Differentiate between RISC and CISC. 7
6. a) How parallelism occurs in uniprocessor system? What are the connections possible for multiprocessor system? 8
- b) Assume that pipeline has K=6 segment and execute n=120 tasks in sequence .Let the time taken to process a sub-operation in each segment is 30 sec. Calculate the speed up ratio in the pipeline. 7
7. Write short notes on: (Any two) 2×5
 - a) Dual Core and Quad Core Processors.
 - b) BCD Adder.
 - c) Register Windowing and Register Renaming.

POKHARA UNIVERSITY

Level: Bachelor
Programme: BE
Course: Computer Architecture (New Course)

Semester: Fall

Year : 2014
Full Marks: 100
Pass Marks: 45
Time : 3 hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a) Differentiate between computer organization and architecture with example. 8
- b) Define RTL .Explain all micro operations with RTL code 7
2. a) Draw internal CPU structure and explain each part. 7
- b) What is normalization in floating point operation? How do you normalize the floating point after floating point operation? 8
3. a) Explain Booth algorithm and use it to multiply $(-5)_{10} * (-7)_{10}$ 8
- b) Differentiate between hardwired and micro programmed control unit. Which one is preferable and why? Illustrate. 7
4. a) What are the various microinstruction sequencing techniques used in control unit? 8
- b) Explain operation of magnetic disk with necessary diagram. 7
5. a) Define Cache memory. What is cache coherence? Explain associative mapping technique. 8
- b) Differentiate between programmed I/O and interrupt driven I/O. 7
6. a) What is pipelining? Explain major hurdles of pipelining. 7
- b) Why cache coherency occurs in multiprocessor system and how can this problem be removed. Explain 8
7. Write short notes on: (Any two) 2x5
 - a) Dual core and Quad core Processor
 - b) Cache coherence
 - c) RAID

POKHARA UNIVERSITY

Level: Bachelor
Programme: BE
Course: Computer Architecture

Semester: Spring

Year : 2014
Full Marks: 100
Pass Marks: 45
Time : 3hrs.

Candidates are required to give their answers in their own words as far as practicable.

The figures in the margin indicate full marks.

Attempt all the questions.

1. a) Differentiate between Computer Architecture and Computer Organization. Explain the term SSI, LSI and VLSI. 8
- b) Define the term micro-operation. Write down the sequence of microinstructions for fetch and interrupt cycle. 7
2. a) What is the necessity of Booth's algorithm? Draw the flowchart for floating point division. 8
- b) What is microprogramming? Explain the function of micro programmed control unit with figure. 7
3. a) Draw draft architecture of CPU and show the microinstruction and control signal for the following instruction:
 - i. Load Accumulator
 - ii. Store Accumulator
 - iii. And to Accumulator
 - iv. Jump if AC=0.8
- b) Why are external devices not connected directly with bus structure of computer system? Draw an internal structure of I/O module. 7
4. a) What is writing policy in cache? Explain about direct mapping of cache memory with its pros and cons. 7
- b) Discuss Interrupt Driven I/O with necessary block diagram. 8
5. a) Explain various types of interconnection Structures in multiprocessor system. 8
- b) Define RISC processor and differentiate it with CISC processor. 7
6. a) What are different approaches for dealing with condition branches? Describe how branch prediction and delayed branch deal with condition branch. 8

- 7
- b) In certain scientific computations it is necessary to perform the arithmetic operation $(A_i + B_i)/(C_i + D_i)$ with a stream of numbers. Specify a pipeline configuration to carry out this task. List the contents of all registers in the pipeline for $i=1$ through 6. 2x5
7. Write short notes on: (Any two)
- Multicore organization
 - VHDL
 - Flynn's classification of computer