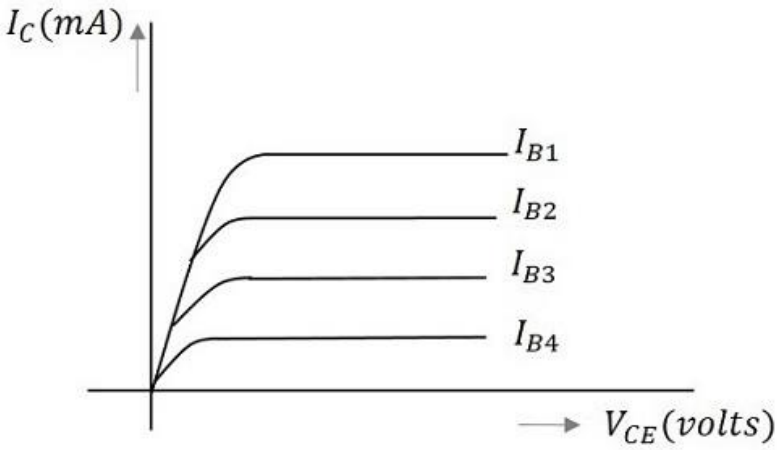
Output Characteristics

When the output characteristics of a transistor are considered, the curve looks as below for different input values.



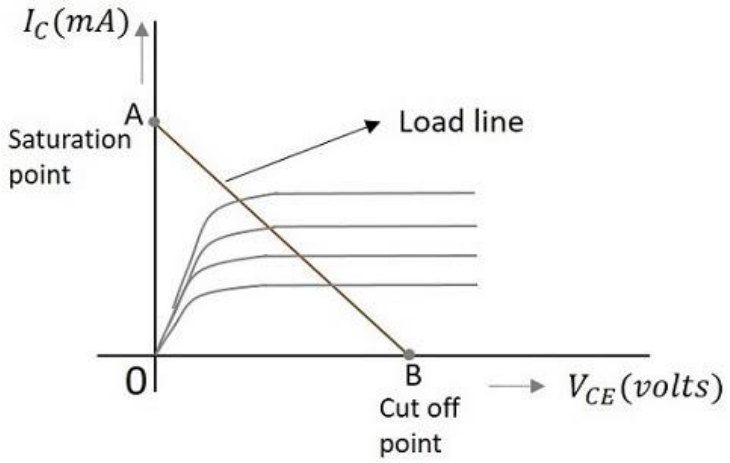
In the above figure, the output characteristics are drawn between collector current $\mathbf{I_c}$ and collector voltage $\mathbf{V_{CE}}$ for different values of base current $\mathbf{I_B}$. These are considered here for different input values to obtain different output curves.

Load Line

When a value for the maximum possible collector current is considered, that point will be present on the Y-axis, which is nothing but the **Saturation point**. As well, when a value for the maximum possible collector emitter voltage is considered, that point will be present on the X-axis, which is the **Cutoff point**.

When a line is drawn joining these two points, such a line can be called as **Load line**. This is called so as it symbolizes the output at the load. This line, when drawn over the output characteristic curve, makes contact at a point called as **Operating point** or **quiescent point** or simply **Q-point**.

The concept of load line can be understood from the following graph.

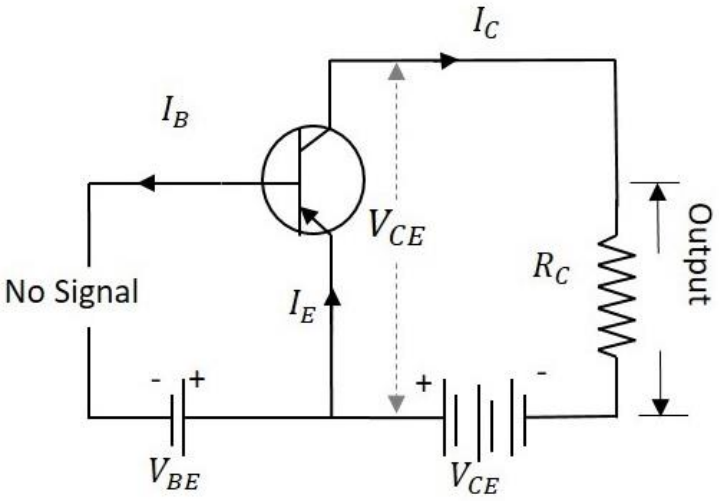


The load line is drawn by joining the saturation and cut off points. The region that lies between these two is the **linear region**. A transistor acts as a good amplifier in this linear region.

If this load line is drawn only when DC biasing is given to the transistor, but **no input** signal is applied, then such a load line is called as **DC load line**. Whereas the load line drawn under the conditions when an **input signal** along with the DC voltages are applied, such a line is called as an **AC load line**.

DC Load Line

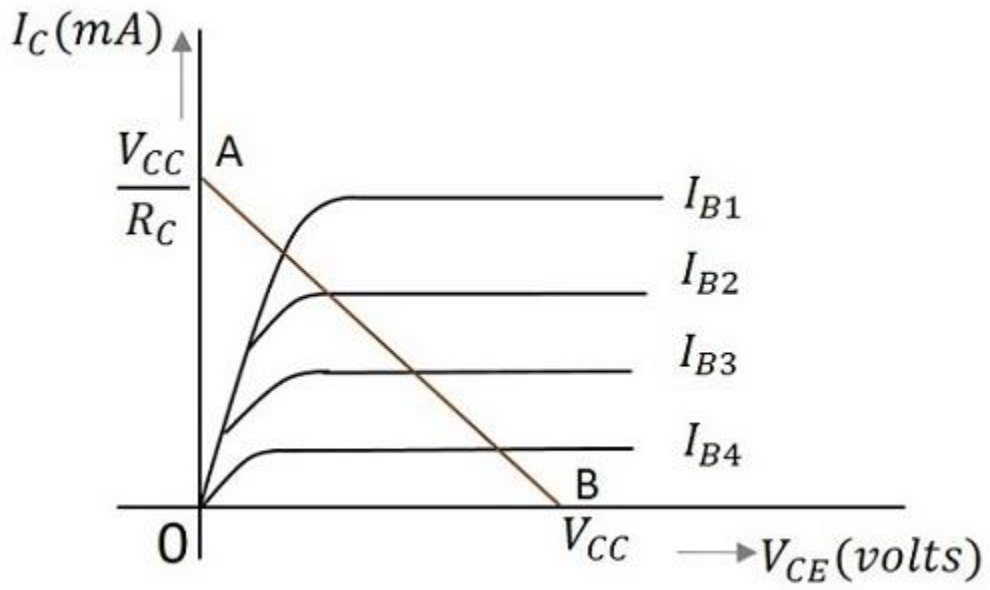
When the transistor is given the bias and no signal is applied at its input, the load line drawn under such conditions, can be understood as **DC** condition. Here there will be no amplification as the **signal is absent**. The circuit will be as shown below.



The value of collector emitter voltage at any given time will be

$$V_{CE} = V_{CC} - I_C R_C$$

As V_{cc} and R_c are fixed values, the above one is a first degree equation and hence will be a straight line on the output characteristics. This line is called as **D.C. Load line**. The figure below shows the DC load line.



To obtain the load line, the two end points of the straight line are to be determined. Let those two points be A and B.

To obtain A

When collector emitter voltage V_{CE} = 0, the collector current is maximum and is equal to V_{cc}/R_c. This gives the maximum value of V_{CE}. This is shown as

$$V_{CE} = V_{CC} - I_C R_C$$

$$0 = V_{CC} - I_C R_C$$

$$I_C = V_{CC}/R_C$$

This gives the point A (OA = V_{cc}/R_c) on collector current axis, shown in the above figure.

To obtain B

When the collector current $I_c = 0$, then collector emitter voltage is maximum and will be equal to the V_{cc}. This gives the maximum value of I_c. This is shown as

$$V_{CE} = V_{CC} - I_C R_C$$

$$= V_{CC}$$

(AS $I_c = 0$)

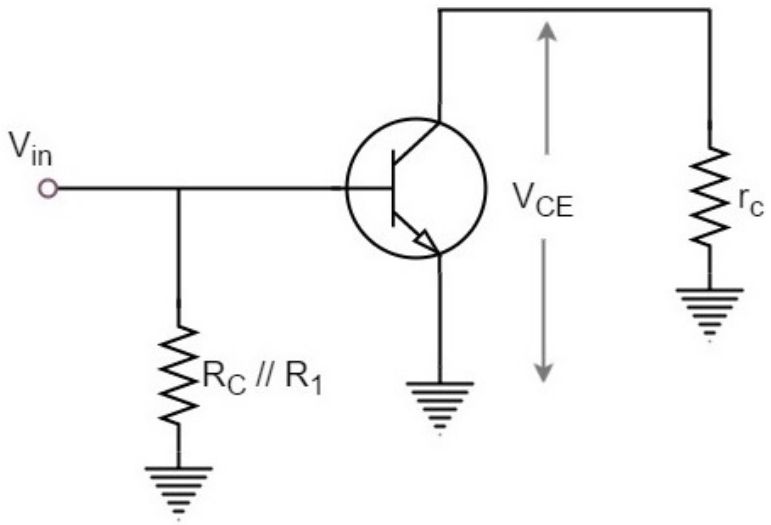
This gives the point B, which means (OB = V_{cc}) on the collector emitter voltage axis shown in the above figure.

Hence we got both the saturation and cutoff point determined and learnt that the load line is a straight line. So, a DC load line can be drawn.

AC Load Line

The DC load line discussed previously, analyzes the variation of collector currents and voltages, when no AC voltage is applied. Whereas the AC load line gives the peak-to-peak voltage, or the maximum possible output swing for a given amplifier.

We shall consider an AC equivalent circuit of a CE amplifier for our understanding.



From the above figure,

$$V_{CE} = (R_C//R_1) \times I_C$$

$$r_C = R_C//R_1$$

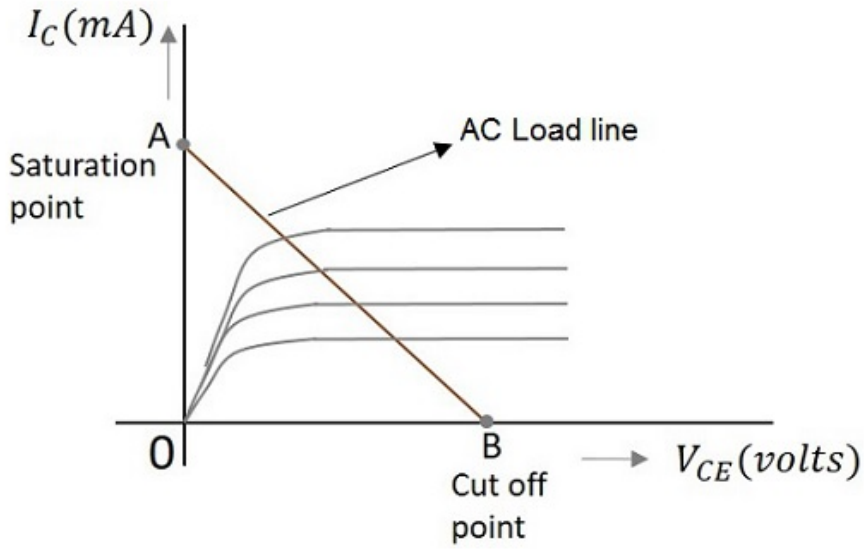
For a transistor to operate as an amplifier, it should stay in active region. The quiescent point is so chosen in such a way that the maximum input signal excursion is symmetrical on both negative and positive half cycles.

Hence,

$$V_{max} = V_{CEQ} \quad \text{and} \quad V_{min} = -V_{CEQ}$$

Where V_{CEQ} is the emitter-collector voltage at quiescent point

The following graph represents the AC load line which is drawn between saturation and cut off points.



From the graph above, the current IC at the saturation point is

$$I_{C(sat)} = I_{CQ} + (V_{CEQ}/r_C)$$

The voltage V_{CE} at the cutoff point is

$$V_{CE(off)} = V_{CEQ} + I_{CQ}r_C$$

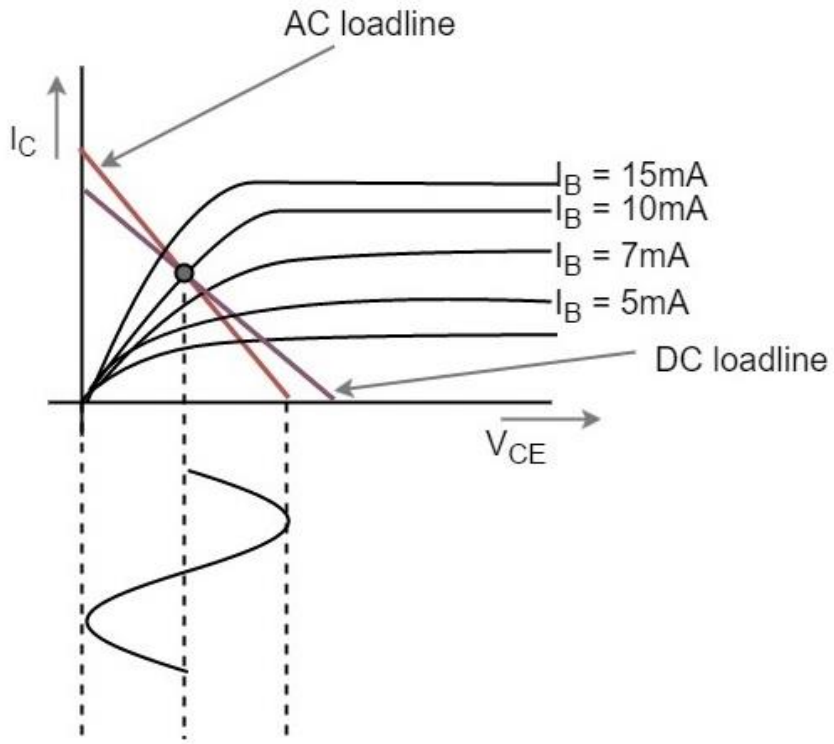
Hence the maximum current for that corresponding $V_{CEQ} = V_{CEQ} / (R_C // R_1)$ is

$$I_{CQ} = I_{CQ} * (R_C//R_1)$$

Hence by adding quiescent currents the end points of AC load line are

$$I_{C(sat)} = I_{CQ} + V_{CEQ}/(R_C//R_1)$$

$$V_{CE(off)} = V_{CEQ} + I_{CQ} * (R_C//R_1)$$


AC loadline
I_C
I_B = 15mA
I_B = 10mA
I_B = 7mA
I_B = 5mA
DC loadline
V_{CE}

Stability factor (S):

It is the rate of change of collector current (I_C) with respect to the reverse saturation current of collector junction (I_{CO}), i.e.

$$S = \frac{\partial I_C}{\partial I_{CO}} \quad \text{---(1)}$$

We know that collector current is given by:

$I_C = \beta I_B + (1 + \beta) I_{CO}$ ---(2)

Differentiating equation (2) w.r.t I_C and treating β as constant, we can write:

$$1 = \beta \times \frac{\partial I_B}{\partial I_C} + (1 + \beta) \frac{\partial I_{CO}}{\partial I_C}$$

$$\frac{\partial I_{CO}}{\partial I_C} = \frac{1 - \beta \frac{\partial I_B}{\partial I_C}}{1 + \beta}$$

$$\frac{\partial I_C}{\partial I_{CO}} = \frac{1 + \beta}{1 - \beta \frac{\partial I_B}{\partial I_C}} \quad \text{---(3)}$$

From (1) & (3), we get:

Stability factor (S) will be:

$$S = \frac{\partial I_C}{\partial I_{CO}} = \frac{1 + \beta}{1 - \beta \frac{\partial I_B}{\partial I_C}}$$