Question 14.14:

In a p-n junction diode, the current I can be expressed as

$$I = I_0 \exp\left(\frac{\mathrm{eV}}{2k_B T} - 1\right)$$

where I_0 is called the reverse saturation current, V is the voltage across the diode and is positive for forward bias and negative for reverse bias, and I is the current through the diode, $k_B$is the Boltzmann constant (8.6×10^{-5} eV/K) and T is the absolute temperature. If for a given diode $I_0 = 5 \times 10^{-12}$ A and T = 300 K, then

(a) What will be the forward current at a forward voltage of 0.6 V?

(b) What will be the increase in the current if the voltage across the diode is increased to 0.7 V?

(c) What is the dynamic resistance?

(d) What will be the current if reverse bias voltage changes from 1 V to 2 V?

Answer

In a p-n junction diode, the expression for current is given as:

$$I = I_0 \exp\left(\frac{\mathrm{eV}}{2k_B T} - 1\right)$$

Where,

I_0 = Reverse saturation current = 5×10^{-12} A

T = Absolute temperature = 300 K

k_B = Boltzmann constant = 8.6×10^{-5} eV/K = 1.376×10^{-23} J K^{-1}

V = Voltage across the diode

(a) Forward voltage, V = 0.6 V

∴Current, I $$= 5 \times 10^{-12}\left[\exp\left(\frac{1.6 \times 10^{-19} \times 0.6}{1.376 \times 10^{-23} \times 300}\right) - 1\right]$$

$$= 5 \times 10^{-12} \times \exp[22.36] = 0.0256 \text{ A}$$

Therefore, the forward current is about 0.0256 A.

(b) For forward voltage, $V' = 0.7$ V, we can write:

$$I' = 5 \times 10^{-12}\left[\exp\left(\frac{1.6 \times 10^{-19} \times 0.7}{1.376 \times 10^{-23} \times 300} - 1\right)\right]$$

$$= 5 \times 10^{-12} \times \exp[26.25] = 1.257 \text{ A}$$

Hence, the increase in current, $\Delta I = I' - I$

= 1.257 − 0.0256 = 1.23 A

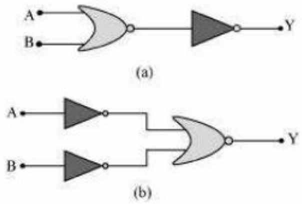
(c) Dynamic resistance $= \frac{\text{Change in voltage}}{\text{Change in current}}$

$$= \frac{0.7 - 0.6}{1.23} = \frac{0.1}{1.23} = 0.081\ \Omega$$

(d) If the reverse bias voltage changes from 1 V to 2 V, then the current (I) will almost remain equal to I_0 in both cases. Therefore, the dynamic resistance in the reverse bias will be infinite.

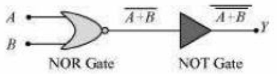
Question 14.15:

You are given the two circuits as shown in Fig. 14.44. Show that circuit (a) acts as OR gate while the circuit (b) acts as AND gate.



Answer

(a) *A* and *B* are the inputs and *Y* is the output of the given circuit. The left half of the given figure acts as the NOR Gate, while the right half acts as the NOT Gate. This is shown in the following figure.



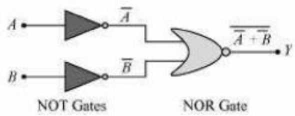
Hence, the output of the NOR Gate = $\overline{A + B}$

This will be the input for the NOT Gate. Its output will be $\overline{\overline{A + B}}$ = *A* + *B*

∴*Y* = *A* + *B*

Hence, this circuit functions as an OR Gate.

(b) *A* and *B* are the inputs and *Y* is the output of the given circuit. It can be observed from the following figure that the inputs of the right half NOR Gate are the outputs of the two NOT Gates.



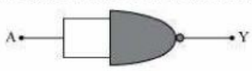
Hence, the output of the given circuit can be written as:

$$Y = \overline{\overline{A} + \overline{B}} = \overline{\overline{A}} \cdot \overline{\overline{B}} = A \cdot B$$

Hence, this circuit functions as an AND Gate.

Question 14.16:

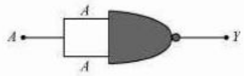
Write the truth table for a NAND gate connected as given in Fig. 14.45.



Hence identify the exact logic operation carried out by this circuit.

Answer

A acts as the two inputs of the NAND gate and *Y* is the output, as shown in the following figure.



NAND Gate

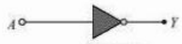
Hence, the output can be written as:

$Y = \overline{A \cdot A} = \overline{A} + \overline{A} = \overline{A}$ ... (i)

The truth table for equation (i) can be drawn as:

A	**Y** $(= \overline{A})$
0	1
1	0

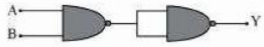
This circuit functions as a NOT gate. The symbol for this logic circuit is shown as:



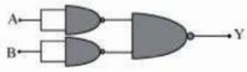
NOT Gate

Question 14.17:

You are given two circuits as shown in Fig. 14.46, which consist of NAND gates. Identify the logic operation carried out by the two circuits.



(a)



(b)

Answer

In both the given circuits, A and B are the inputs and Y is the output.

(a) The output of the left NAND gate will be $\overline{A.B}$, as shown in the following figure.

*********** END **********