

# Mani Tripathi

## Web Developer

Motivated individual who demonstrates strong work ethic & creative ability. I could offer my contribution positively for my personal growth as well as for the growth of organisation.



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Gorakhpur, Uttar Pradesh,  
India



github.com/manitripathi

## SKILLS

HTML5

CSS

Javascript

GIT

C/C++

Verilog HDL

FPGA

MS-Office

## LANGUAGES

English

Native or Bilingual Proficiency

Hindi

Native or Bilingual Proficiency

## INTERESTS

Sketching

Travelling

Yoga

## EDUCATION

### B.Tech (Electronics & Communication Engineering)

IET MJP Rohilkhand University

06/2016 - 09/2020

Bareilly, India

Courses

▫ 8.10 cpga

### Passed 10+2

RPM Academy (CBSE Board)

06/2016

Gorakhpur, India

Courses

▫ 72%

### Passed 10

RPM Academy (CBSE Board)

06/2014

Gorakhpur, India

Courses

▫ 8.8 cgpa

## WORK EXPERIENCE

### Graduate Engineer Trainee

Huawei Technologies India PVT LTD

05/2021

Gurgaon, India

Role:

▫ Working as an RF Engineer, monitoring and analysing the data according to standards of telecommunications.

## CERTIFICATES

### VLSI DESIGN Using Verilog HDL and FPGA (06/2019 - 07/2019)

Completed 6 Weeks Industrial training in VLSI Design using Verilog HDL & FPGA from DKOP LABS PVT LTD, NOIDA, U.P.

### C++ Programming Language (06/2017)

Completed 4 Weeks training on C++ Programming Language from NIIT

## PERSONAL PROJECTS

### Major Project: Pipelined 16-bit RISC Processor using Verilog HDL (10/2019 - 02/2020)

▫ Final year Project Implemented & simulated on Modelsim using Verilog HDL in which multiple instructions can be executed using a fewer cycle per instruction.

### TODO LIST APP

▫ This project contains the capabilities of JS connecting the HTML pages with functionality written in JS files, will be using multiple DOM functions.

### Digital Clock

▫ Responsive web design of Digital Clock using HTML, CSS & Javascript.

### Car Animation

▫ Web page with CSS Animation effects, where car looks like moving/running on the road.