Manjeet Hooda

E-mail: email@manjeethooda.com
Phone: +91-7022957556

SKILLS

LANGUAGES: Java, C++, C, MATLAB, System Verilog
TECHNOLOGIES: Amazon AWS, Git, Perforce, **Play Framework, MongoDB**, **Spring Framework, Postgress,** prior experience in **Open CV**
OPERATING SYSTEMS: Windows, **Linux** (or any POSIX compliant OS)
UNDERGRAD RESEARCH: Image Processing, Machine Vision, Stereo Vision, Mean-Shift Object Tracking, Bootloader on Intel Atom, Linux and Open CV for ARM SoC, Machine Vision in VHDL on FPGA

WORK EXPERIENCE

Amazon India — Jan 2016 — Present

Software Development Engineer

Working on developing a framework to automate the process of reviewing ads following the amazon policy and guidelines submitted sellers and merchandisers .

- Used Spring Framework for developing backend API
- Used Postgress JDBC driver to interact with DB
- Languages Used: Java

Nvidia India — August 2015 — Dec 2016

CPU - Denver Engineer

- Owns CCLA in XAVIER CPU
- Developed entire verification unit of CCLA
- Only new recruit to be given ownership
- Languages Used: System Verilog, UVM

Kosync — Sep 2016 — Present

Attempt at Starting Up

Kosync is an add on for Bitbucket Jira ticketing platform for creating a jira issue to automate the process of tracking the code revisions and documentations. May expand to some other areas too.

- Developed entire **backend api**
- Worked on various technologies like **MongoDB, Play Framework, AWS**.
- Languages used: **Java**

Flindr — Sep 2015 — Feb 2016

Attempt at Starting Up

An Android Chat App where users could interact based on their interests and location
Developed entire **Android UI**
Worked on Various Technologies like **Android SDK**, patch9, Android API and libraries
Languages Used: **Java, XML**

Robotics and Machine Intelligence Lab (DTU)

Nov 2012 — May 2015

Member

Worked on various projects in Machine Vision, Computer Architecture and FPGA

- Implemented color based object tracking in Open-CV on Intel Atom
- Booted Linux OS on Intel Atom by hacking bootloader
- Simulated MIPS architecture in Xilinx ISE and using branch prediction for better IPC

EDUCATION

B.Tech. in Electronics and Communication Engineering

— May 2015

Delhi Technological University

CPI: 81%

Intermediate (CBSE Board)

C.R.P.F. Public School

Percentage: 88

High School (CBSE Board)

Kendriya Vidyalaya

Percentage: 85

UNDERGRAD RESEARCH

- **STEREO VISION | FORMATION OF 3D IMAGES FROM 2D IMAGES**

Implemented Stereo Vision algorithm on FPGA using Open-CV (C++ library) and VHDL which takes 2 images of the same frame to find 3D image.

- **MEAN SHIFT ALGORITHM | OBJECT TRACKING ALGORITHM**

Implemented mean shift tracking algorithm on FPGA using Open-CV (C++ library) and VHDL track the moving object from the images taken by camera.

REFERENCES

Mr. Rajesh Rohilla, Associate Professor, Delhi Technological University
Email: rajesh@dce.ac.in