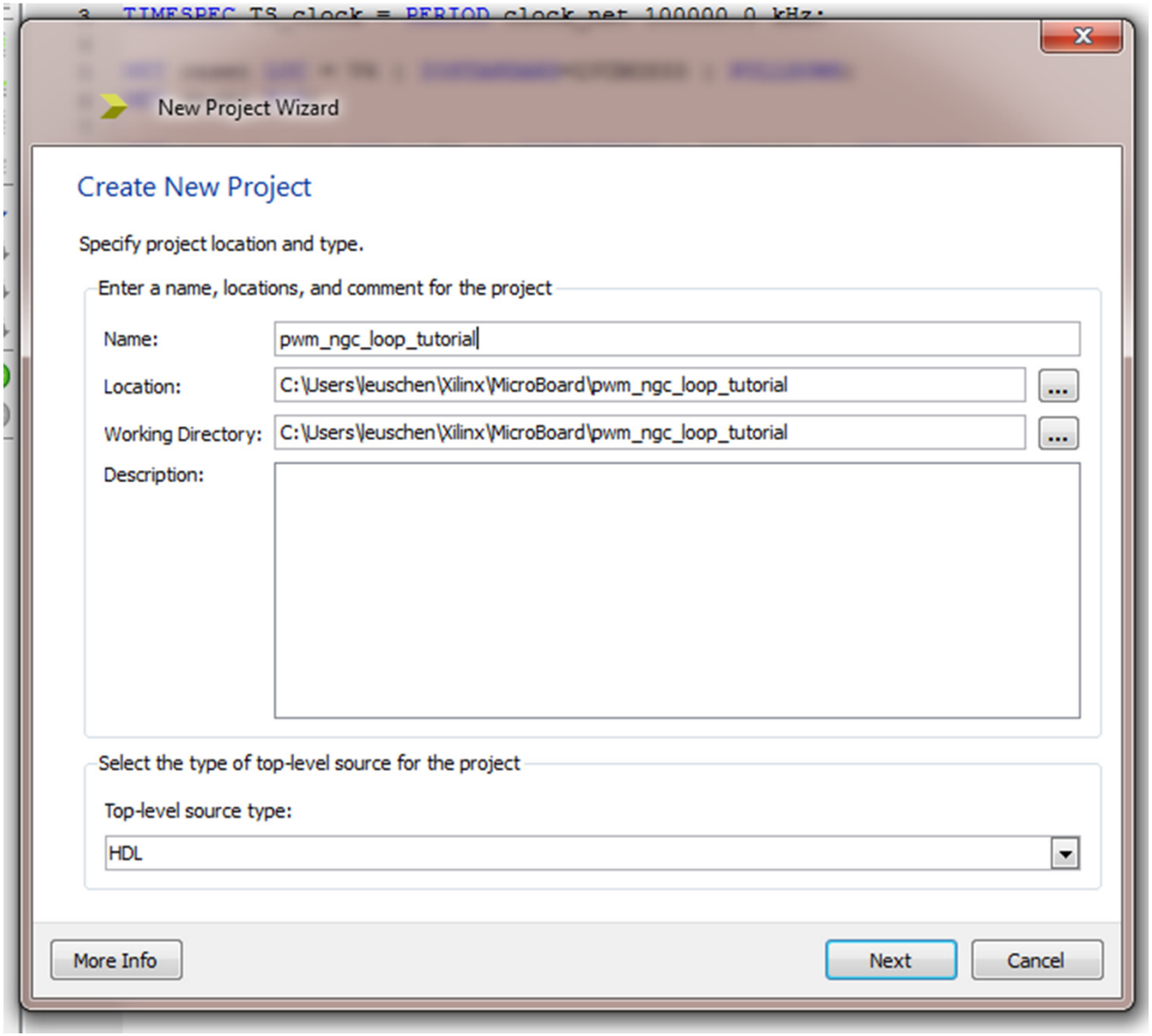
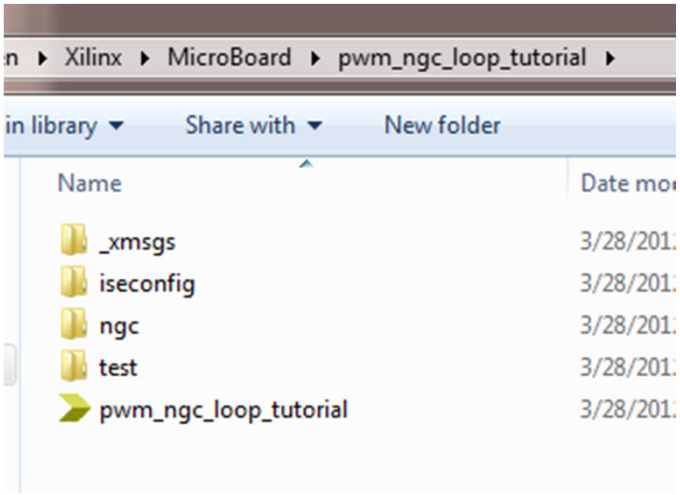
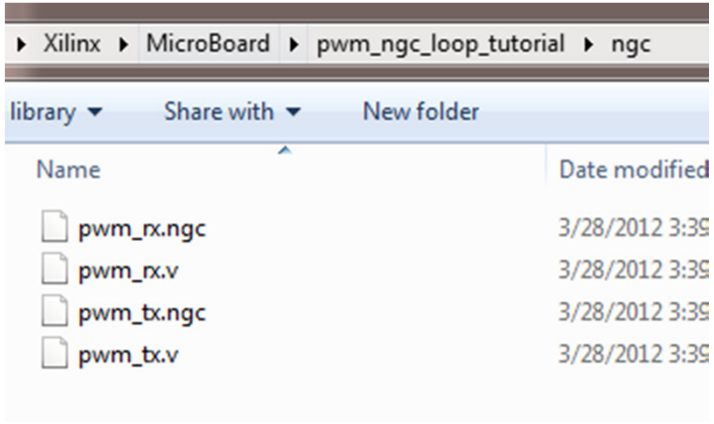
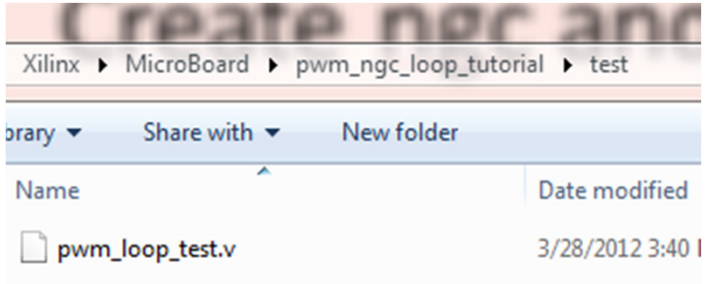
Start a new project



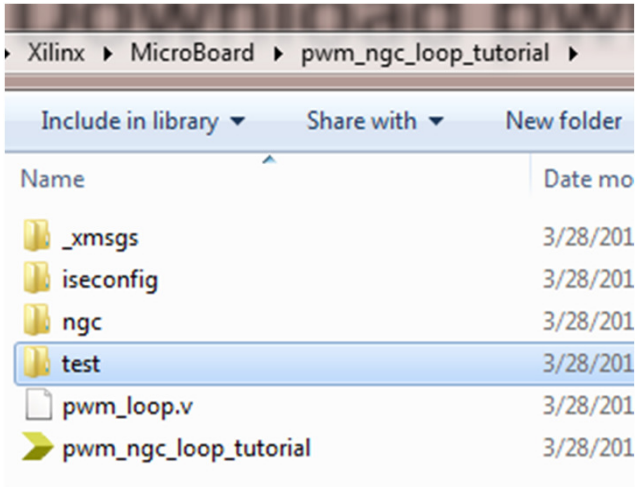
Create ngc and test folders and download pwm_tx.ngc, pwm_tx.v, pwm_rx.ngc, pwm_rx.v to ngc and pwm_loop_test.v to test.

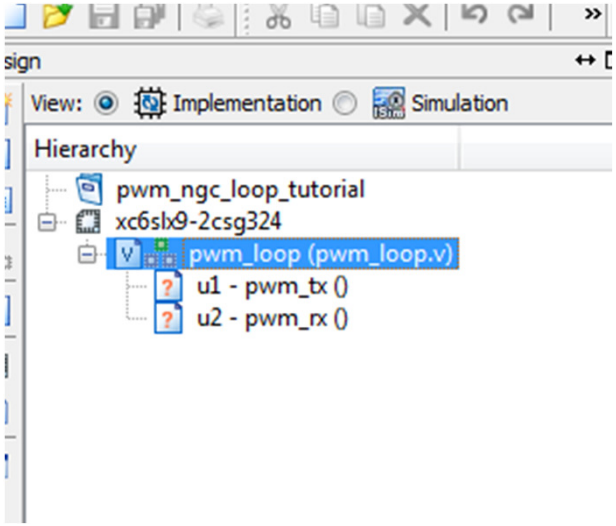






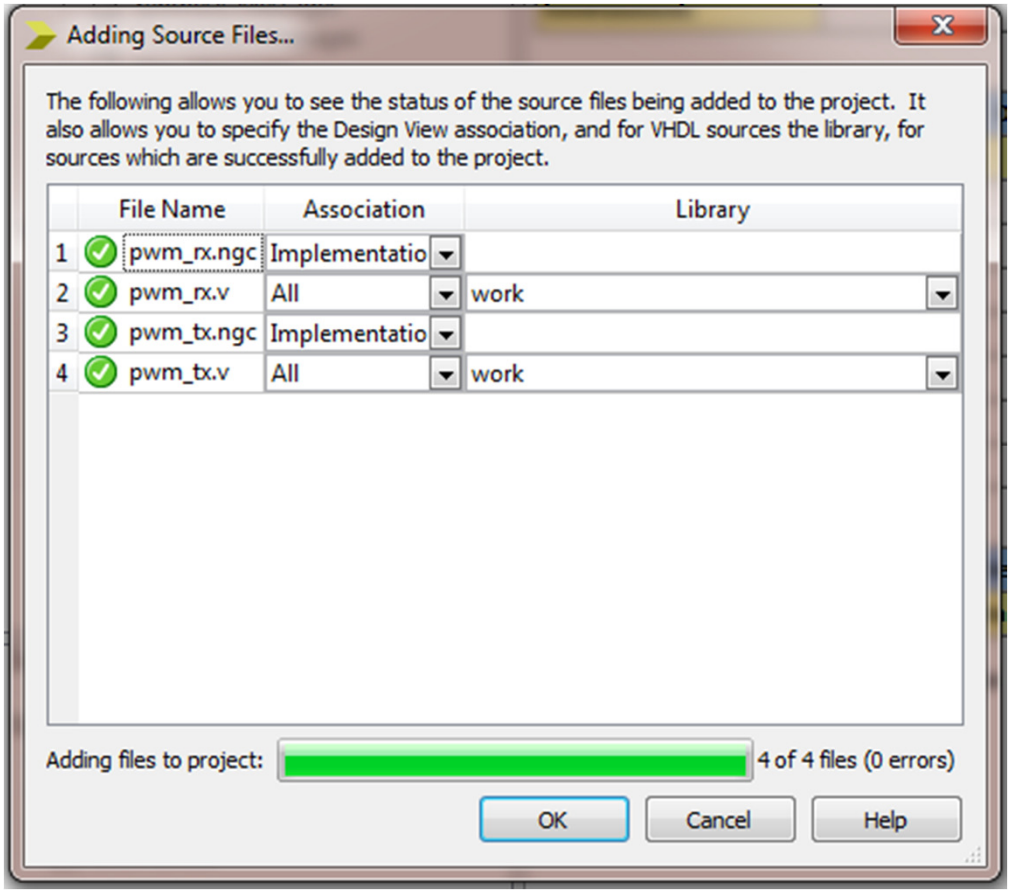
Download pwm_loop.v to project directory and add as a source

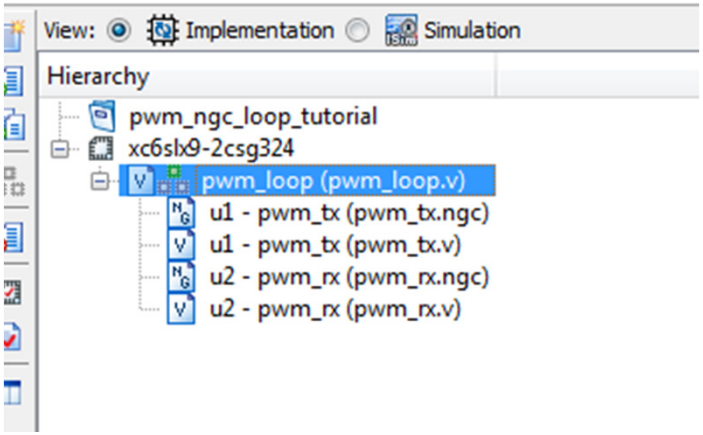




Notice u1 and u2 in the Hierarchy have ? because ISE does not know what file to use for them.

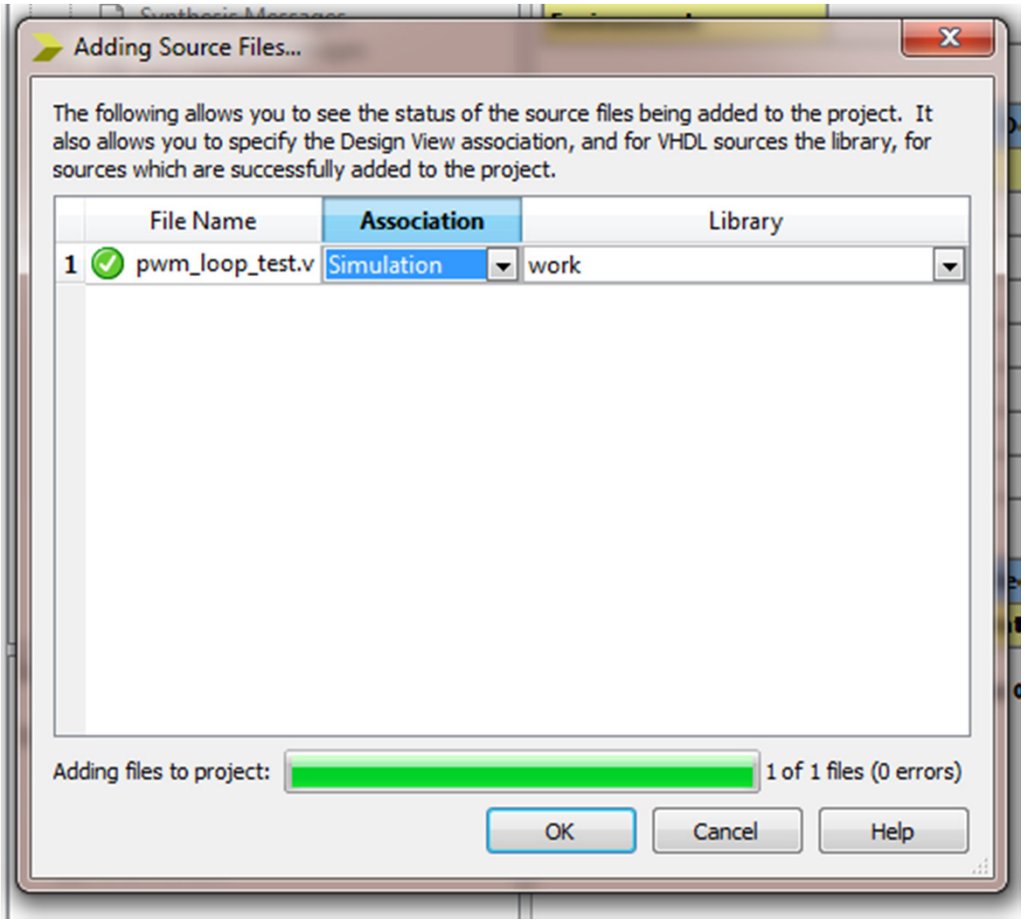
add all files in ngc folder



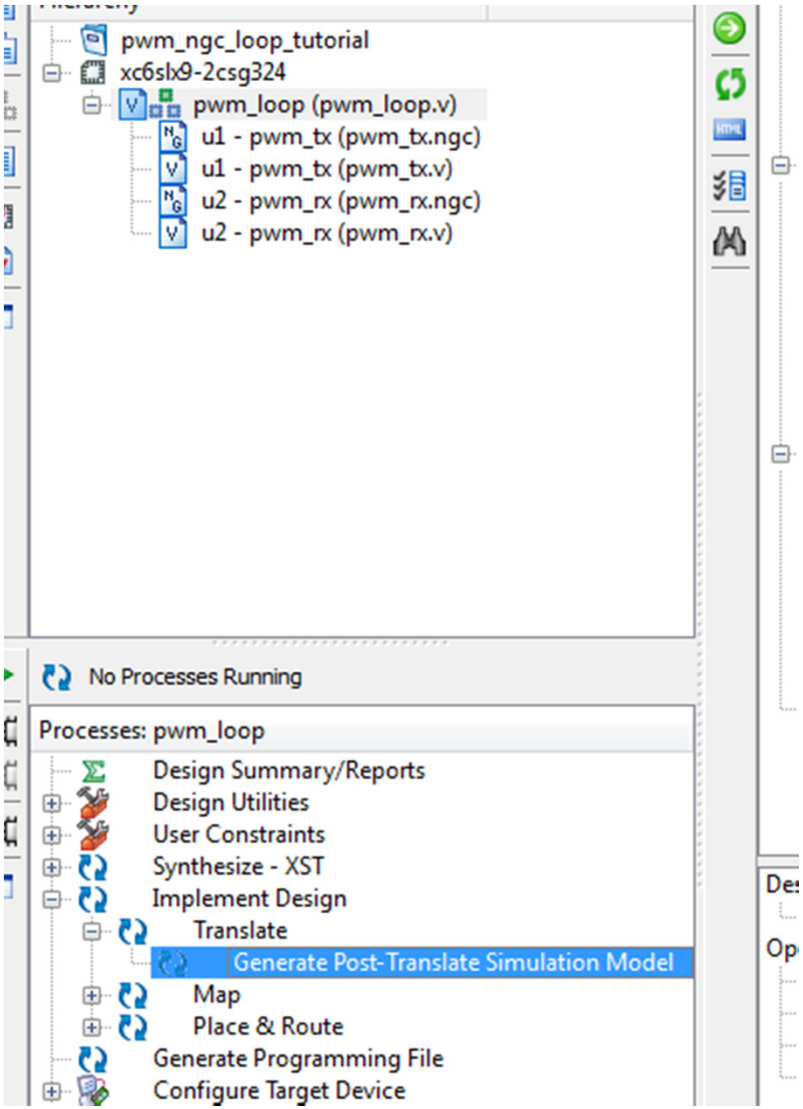


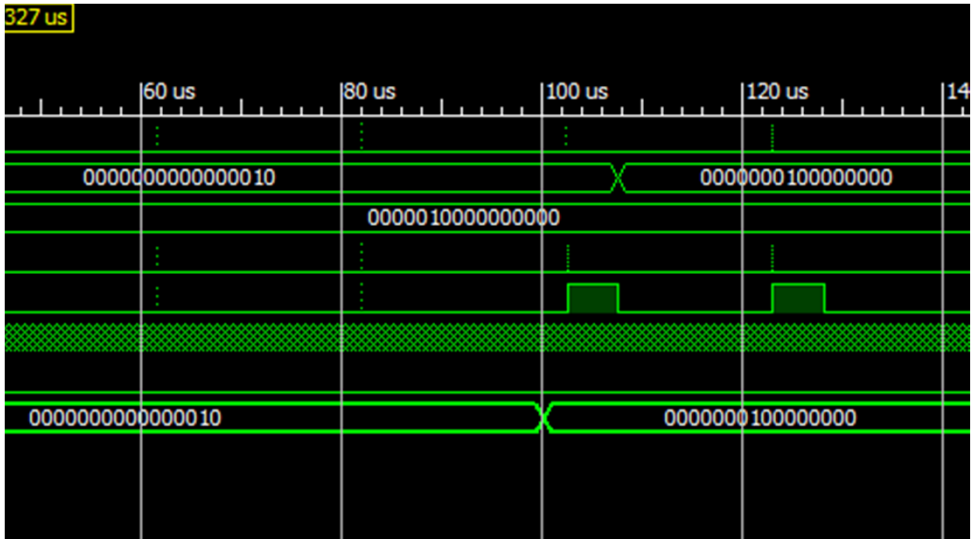
Notice u1 and u2 no longer have ?.

Add test file



Create post translate simulation model and simulate





Modify top level

```
module pwm_loop(
  input  wire        clock,
  input  wire        reset,
//  input  wire [15:0] data_in,
//  output wire        done_tx,
//  output wire [15:0] data_out,
//  output wire [15:0] period,
//  output wire        done_rx,
  input  wire [3:0]  switches,
  output wire [3:0]  leds,
  input  wire        loop_in,
  output wire        loop_out);

  wire        [15:0] data_in;
  wire        [15:0] data_out;
//  wire               loop;

  assign leds = data_out[9:6];
  assign data_in = {6'b000000,switches,6'b000000};
//  assign loop_out = loop;

  pwm_tx u1 (
    .clock(clock),
    .reset(reset),
    .data(data_in),
    .tx(loop_out),
    .done(done_tx));

  pwm_rx u2 (
    .clock(clock),
    .reset(reset),
    .rx(loop_in),
    .data(data_out),
    .period(period),
    .done(done_rx));

endmodule
```

Create a UCF

```
1  NET clock LOC = C10 | IOSTANDARD = LVCMOS33;
2  NET clock TNM_NET = clock_net;
3  TIMESPEC TS_clock = PERIOD clock_net 100000.0 kHz;
4
5  NET reset LOC = V4 | IOSTANDARD=LVCMOS33 | PULLDOWN;
6  NET reset TIG;
7
8  NET leds[0] LOC = P4 | IOSTANDARD = LVCMOS18;
9  NET leds[1] LOC = L6 | IOSTANDARD = LVCMOS18;
10 NET leds[2] LOC = F5 | IOSTANDARD = LVCMOS18;
11 NET leds[3] LOC = C2 | IOSTANDARD = LVCMOS18;
12
13 NET switches[0] LOC = B3  | IOSTANDARD = LVCMOS33 | PULLDOWN;
14 NET switches[1] LOC = A3  | IOSTANDARD = LVCMOS33 | PULLDOWN;
15 NET switches[2] LOC = B4  | IOSTANDARD = LVCMOS33 | PULLDOWN;
16 NET switches[3] LOC = A4  | IOSTANDARD = LVCMOS33 | PULLDOWN;
17
18 NET loop_out LOC = F15 | IOSTANDARD = LVCMOS33;
19 NET loop_in LOC = F16 | IOSTANDARD = LVCMOS33;
20
21 CONFIG VCCAUX = 3.3;
22
```

Generate bit and run