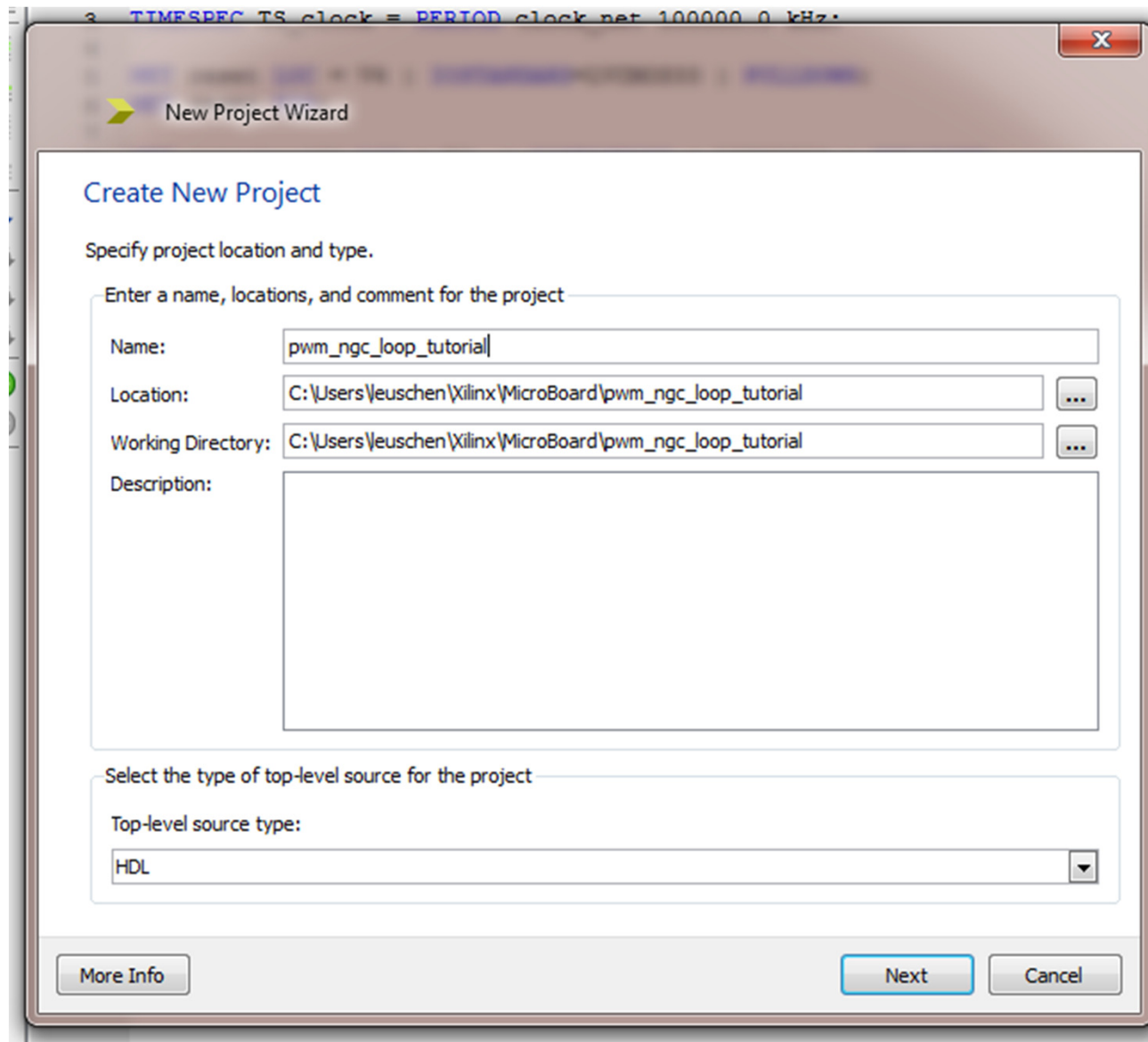


Start a new project



3 TIMESPEC TS_clock = PERIOD_clock.net 100000.0 kHz:

New Project Wizard

Create New Project

Specify project location and type.

Enter a name, locations, and comment for the project

Name: pwm_ngc_loop_tutorial

Location: C:\Users\euschen\Xilinx\MicroBoard\pwm_ngc_loop_tutorial

Working Directory: C:\Users\euschen\Xilinx\MicroBoard\pwm_ngc_loop_tutorial

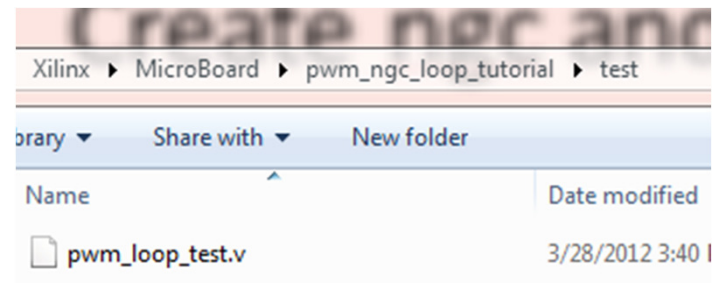
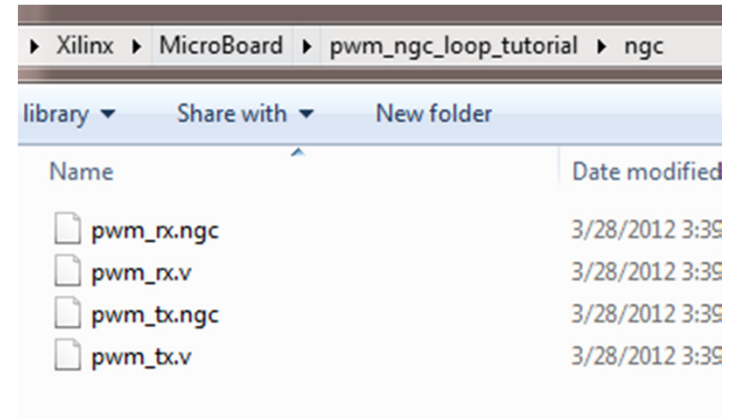
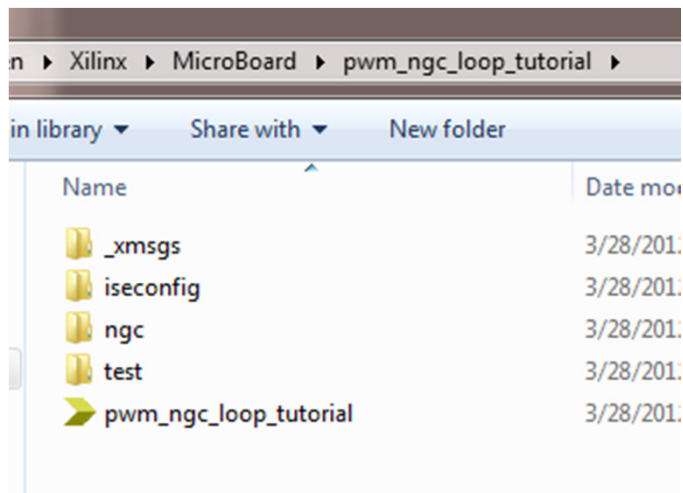
Description:

Select the type of top-level source for the project

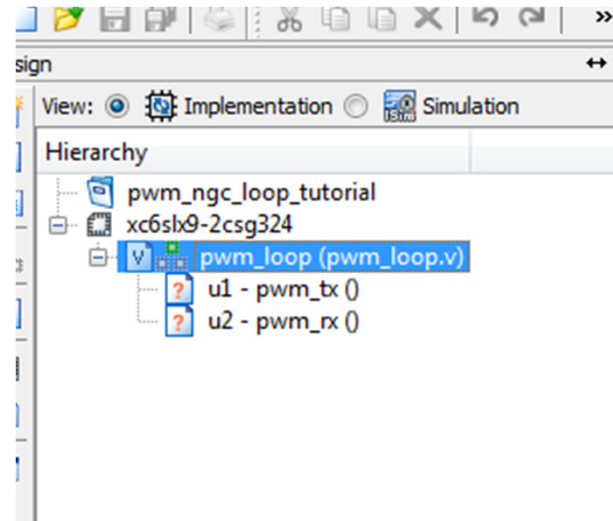
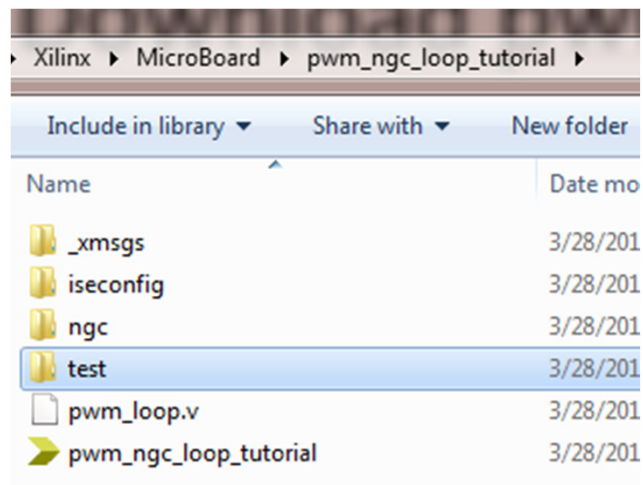
Top-level source type: HDL

More Info Next Cancel

Create ngc and test folders and download pwm_tx.ngc, pwm_tx.v, pwm_rx.ngc, pwm_rx.v to ngc and pwm_loop_test.v to test.

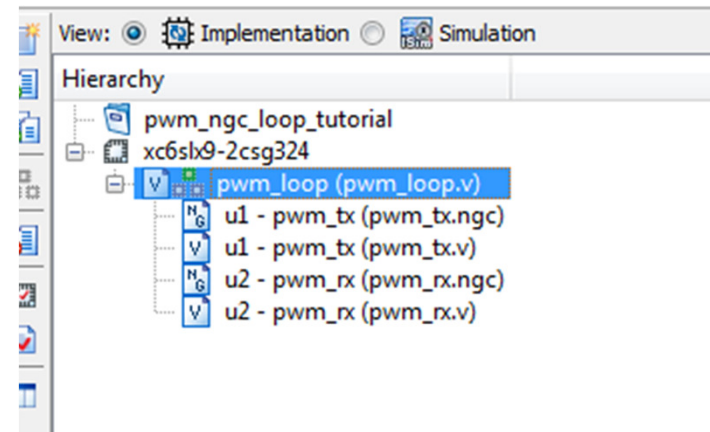
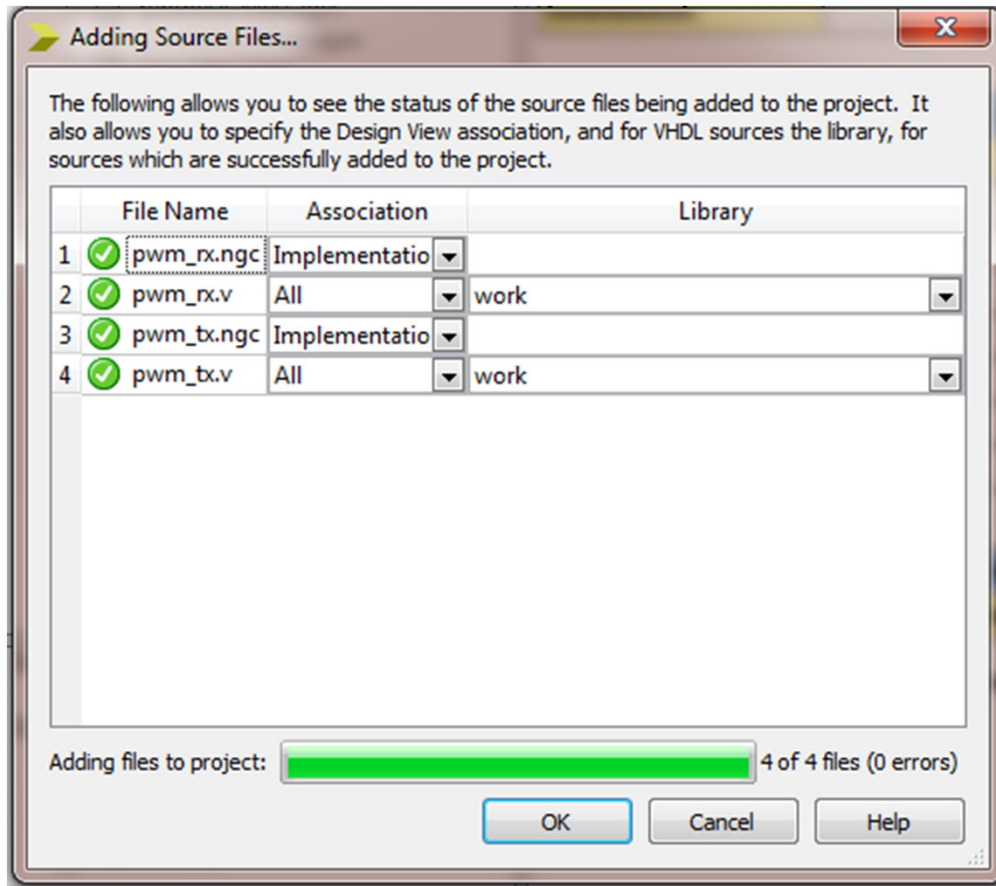


Download pwm_loop.v to project directory and add as a source



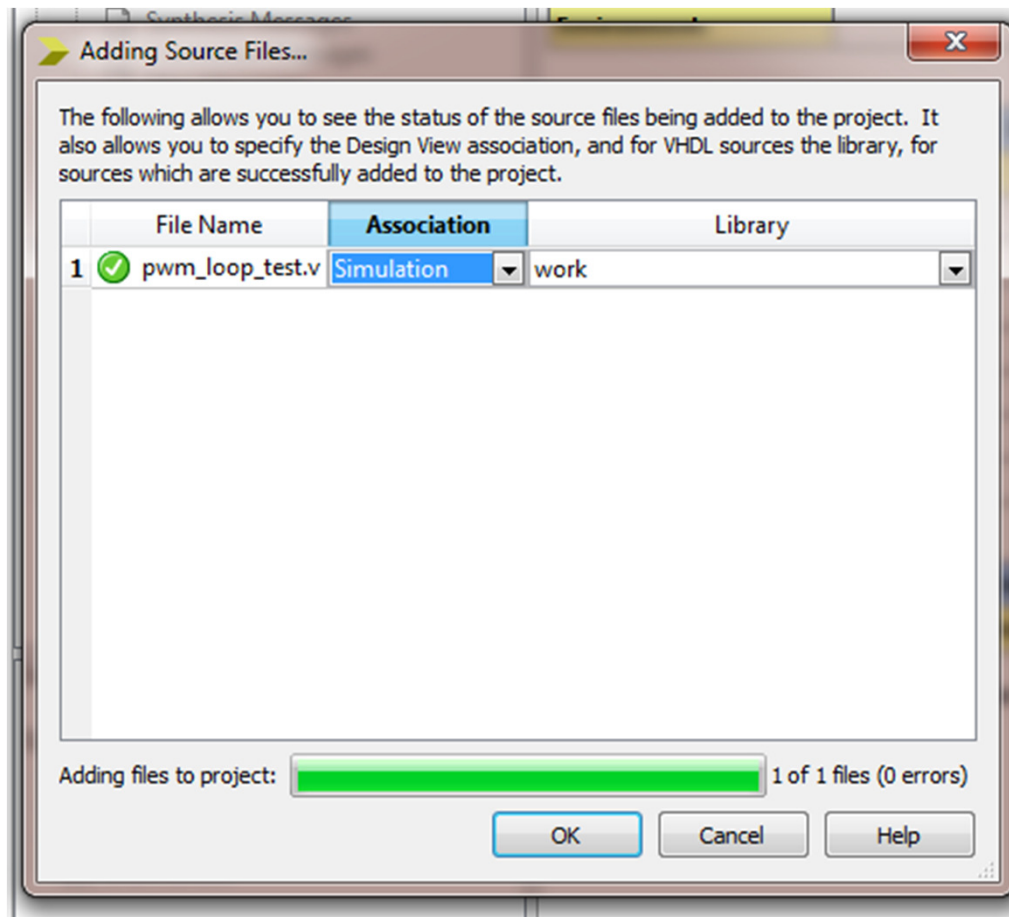
Notice u1 and u2 in the Hierarchy have ? because ISE does not know what file to use for them.

add all files in ngc folder

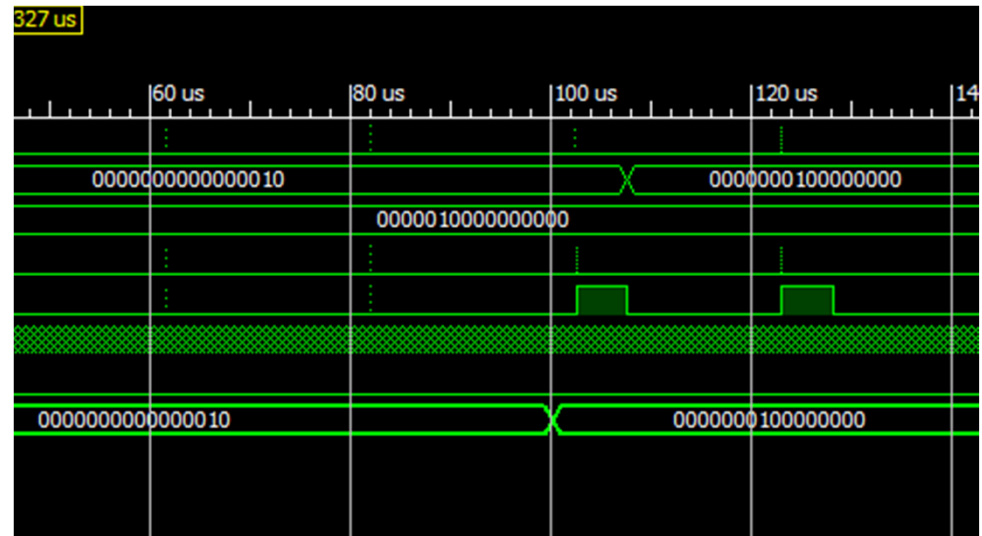
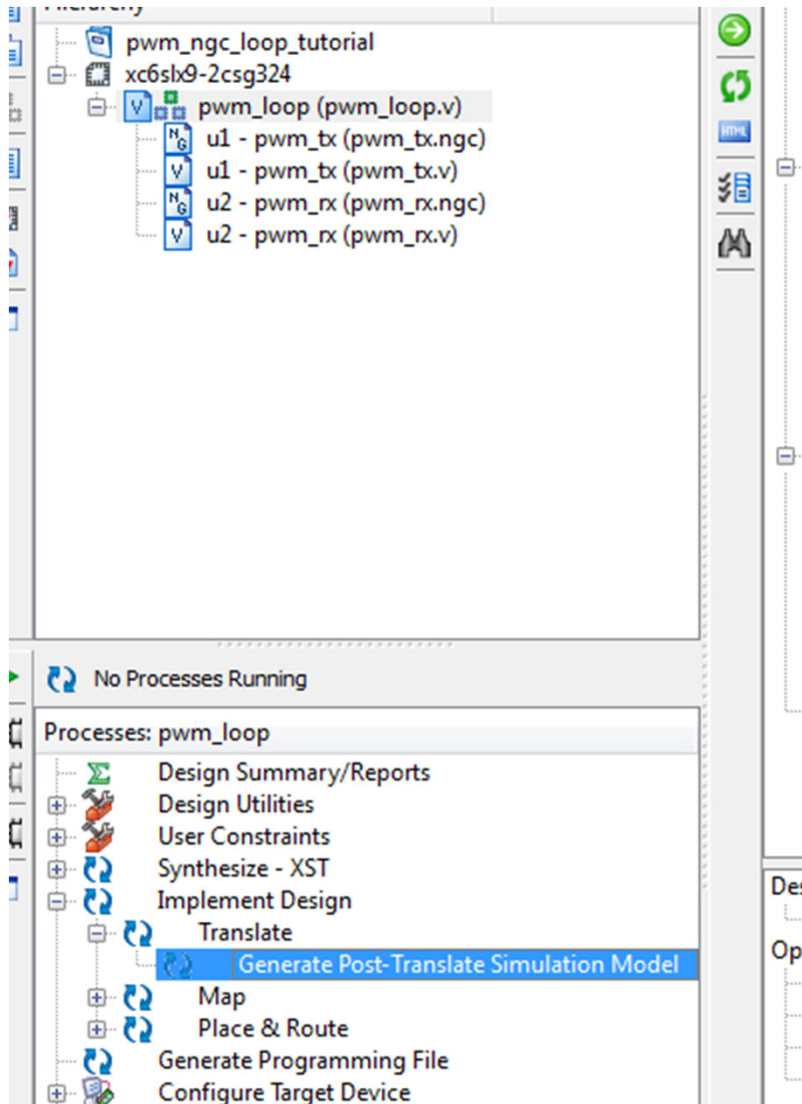


Notice u1 and u2 no longer have ?.

Add test file



Create post translate simulation model and simulate



Modify top level

```
1 module pwm_loop(  
2     input wire      clock,  
3     input wire      reset,  
4     // input wire [15:0] data_in,  
5     // output wire   done_tx,  
6     // output wire [15:0] data_out,  
7     // output wire [15:0] period,  
8     // output wire   done_rx,  
9     input wire [3:0] switches,  
10    output wire [3:0] leds,  
11    input wire      loop_in,  
12    output wire      loop_out);  
13  
14    wire [15:0] data_in;  
15    wire [15:0] data_out;  
16    // wire      loop;  
17  
18    assign leds = data_out[9:6];  
19    assign data_in = {6'b000000, switches, 6'b000000};  
20    // assign loop_out = loop;  
21  
22    pwm_tx u1 (  
23        .clock(clock),  
24        .reset(reset),  
25        .data(data_in),  
26        .tx(loop_out),  
27        .done(done_tx));  
28  
29    pwm_rx u2 (  
30        .clock(clock),  
31        .reset(reset),  
32        .rx(loop_in),  
33        .data(data_out),  
34        .period(period),  
35        .done(done_rx));  
36  
37 endmodule  
38
```

Create a UCF

```
1 NET clock LOC = C10 | IOSTANDARD = LVCMOS33;
2 NET clock TNM_NET = clock_net;
3 TIMESPEC TS_clock = PERIOD clock_net 100000.0 kHz;
4
5 NET reset LOC = V4 | IOSTANDARD=LVCMOS33 | PULLDOWN;
6 NET reset TIG;
7
8 NET leds[0] LOC = P4 | IOSTANDARD = LVCMOS18;
9 NET leds[1] LOC = L6 | IOSTANDARD = LVCMOS18;
10 NET leds[2] LOC = F5 | IOSTANDARD = LVCMOS18;
11 NET leds[3] LOC = C2 | IOSTANDARD = LVCMOS18;
12
13 NET switches[0] LOC = B3 | IOSTANDARD = LVCMOS33 | PULLDOWN;
14 NET switches[1] LOC = A3 | IOSTANDARD = LVCMOS33 | PULLDOWN;
15 NET switches[2] LOC = B4 | IOSTANDARD = LVCMOS33 | PULLDOWN;
16 NET switches[3] LOC = A4 | IOSTANDARD = LVCMOS33 | PULLDOWN;
17
18 NET loop_out LOC = F15 | IOSTANDARD = LVCMOS33;
19 NET loop_in LOC = F16 | IOSTANDARD = LVCMOS33;
20
21 CONFIG VCCAUX = 3.3;
22
```


Generate bit and run