# EECS 700 FPGA PRJ01: Synthesizer

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This design was similar to the knight rider project in certain aspects so the real challenge was to design the pdm which took a lot of time. Apart from that the initialization file for the memory was not provided in the beginning thus delaying the designing of the synthesizer. Also unclear explanation about the design requirements in v1 of the project created design difficulties.

When the issue about the design requirements was clear there wasn’t enough time to check each and every module and merge them together, The synthesis and implementation also took a lot of time.

In part2b playlist, composing the song notes was difficult because of the unfamiliarity with musical signs such as half notes quarter notes etc. so just created a random tone list for this part with 64 ×8 rom.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Tone | Note | Frequency  (HZ) | Rate Divider  (freq in MHZ) | Error (Hz) | RateCounter Limit |
| X | 0000 | - | - | - | - |
| C | 0001 | 130.81 | 2.1432 | 0.948 | 47 |
| D | 0010 | 146.83 | 2.4057 | 1.5082 | 42 |
| E | 0011 | 164.81 | 2.7002 | -0.1499 | 37 |
| F | 0100 | 174.61 | 2.8608 | 0.2238 | 35 |
| G | 0101 | 196.00 | 3.2213 | -0.8876 | 31 |
| A | 0110 | 220.00 | 3.6045 | 2.0173 | 28 |
| B | 0111 | 246.94 | 4.0459 | 2.7994 | 25 |
| C | 1000 | 261.63 | 4.2685 | -3.7402 | 23 |
| D | 1001 | 293.66 | 4.8113 | 3.0164 | 21 |
| E | 1010 | 329.63 | 5.4007 | 8.3923 | 19 |
| F | 1011 | 349.23 | 5.7218 | -9.8003 | 18 |
| G | 1100 | 392.00 | 6.4225 | 10.5303 | 16 |
| A | 1101 | 440.00 | 7.2090 | 4.0346 | 14 |
| B | 1110 | 493.88 | 8.0917 | -14.7463 | 12 |
| C | 1111 | 523.25 | 8.5729 | -31.6137 | 11 |
|  |  |  |  |  |  |

Direct Digital Synthesizer (DDS)

For the 523.25 Hz frequency and 493.88 Mhz tones, the rate counter limits were both 12 so changed the former to be 11 and later one to be 12 thus giving high error value.

Apart from that, everything is working fine, only need proper song file to test it.

Overall it was quite an interesting project particularly when it started to play “Hello” and pure tones. Learnt a lot about vivado and vhdl and the importance of initialization and looking out all the possibilities.