NB-IoT CRC Calculation: A Comparison Between Series and Parallel Architecture

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Problem statement

Hardware implementation of 16-bit series and parallel CRC for 34-bit input data in an NB-IoT system.

Objectives

- Design and implementation of 16-bit Series CRC for 34-bit data.
- Design and implementation of 16-bit Parallel CRC for 34-bit data.
- Performance comparison of series and parallel CRC for power , area and time speed.

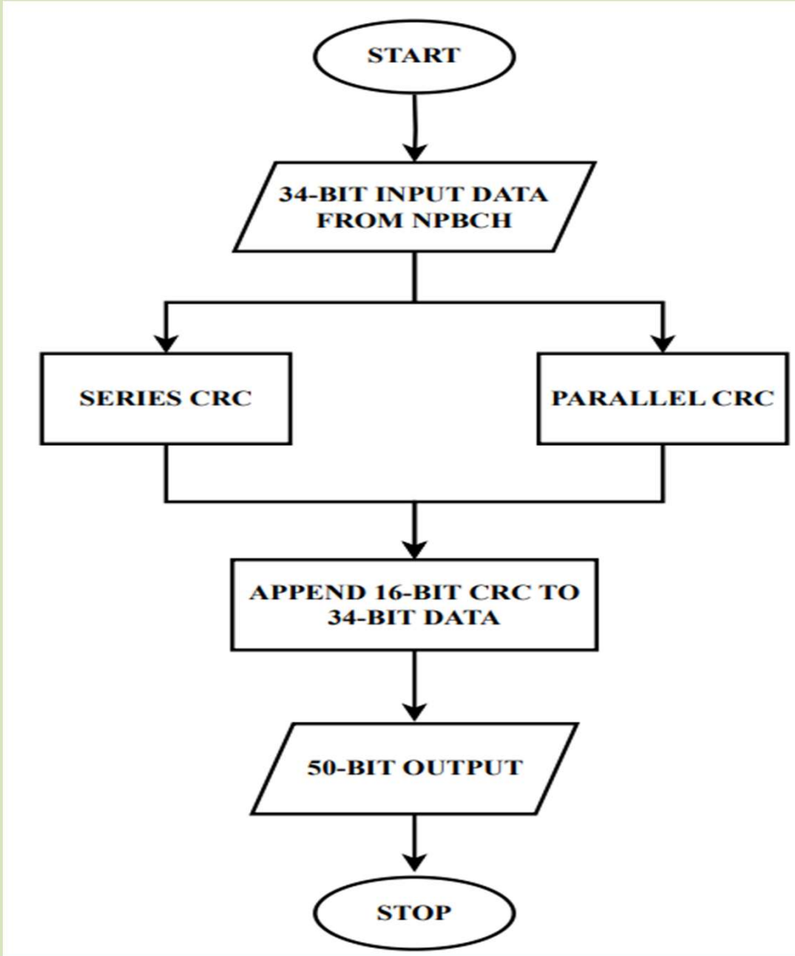
Contributions

An efficient CRC block implementation for NB-IoT system for required specifications.
Performance comparison table of series and parallel CRC block.

Literature survey

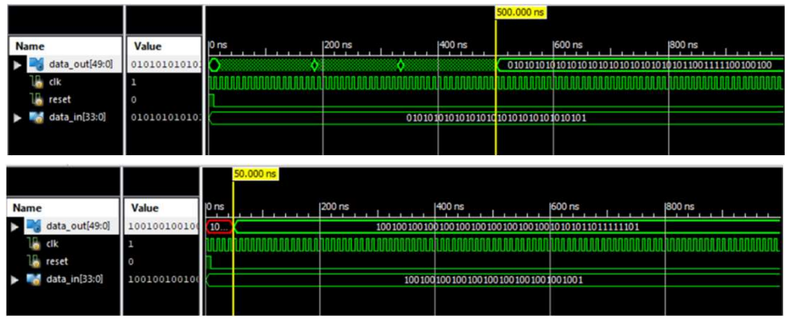
- Steps to implement parallel CRC using the table method.
- Information about the physical layer design of NB-IoT.
- CRC polynomial selection for embedded networks.

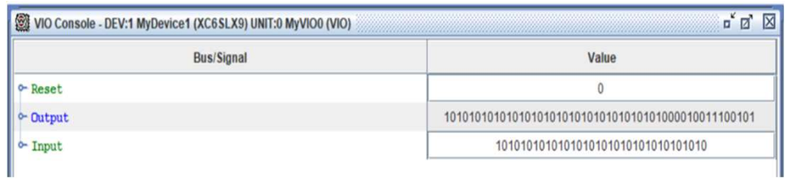
Methodology



Step 1: Verilog coding of series CRC and its hardware implementation.
Step 2: Verilog coding of parallel CRC and its hardware implementation.
Step 3: Comparison of both architectures.

Results





Optimization details

In parallel CRC computation optimization can be obtained by performing 34 shifts which takes 1 clock cycle, instead of 8 shift tables which presently takes 5 clock cycles.

Conclusions

Analyzing the parameters like area, power, delay of series and parallel architecture is performed. It is observed that parallel architecture is 90% faster than series architecture, which is the preferred architecture for applications that need faster outputs. Series architecture when compared to parallel is 48.33% lesser in area and 72.42% lesser power is observed.