CMOS OPEN ENDED

4-BIT PARALLEL ADDER

TEAM - 02

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A. CMOS LOGIC :

1. 2 INPUT AND GATE

Figure 1. 2 Input AND Gate Schematic

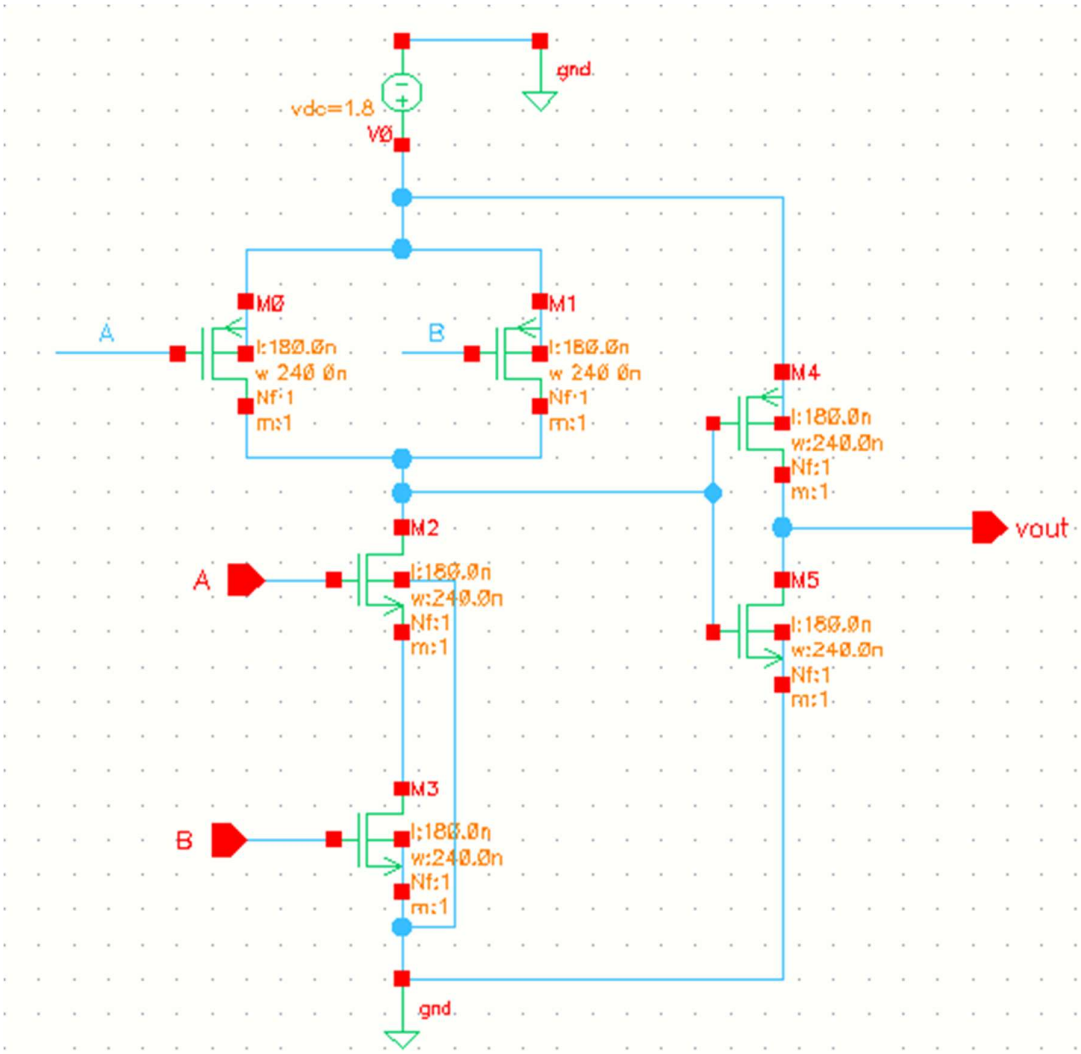
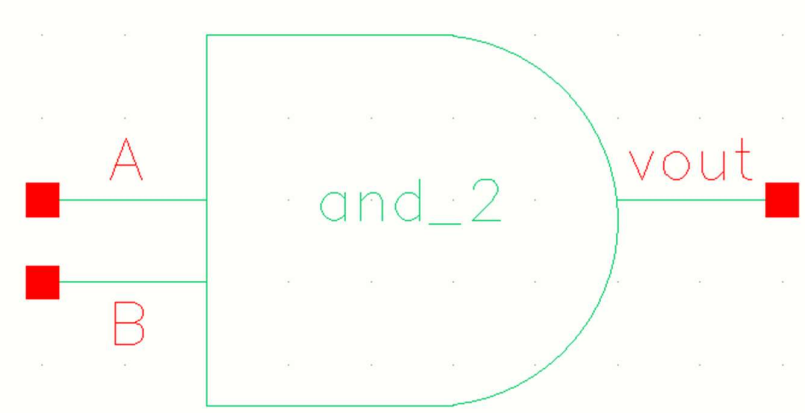


Figure 2. 2 Input AND Gate Symbol



2. 3 INPUT OR GATE

Figure 3. 3 Input OR Gate Schematic

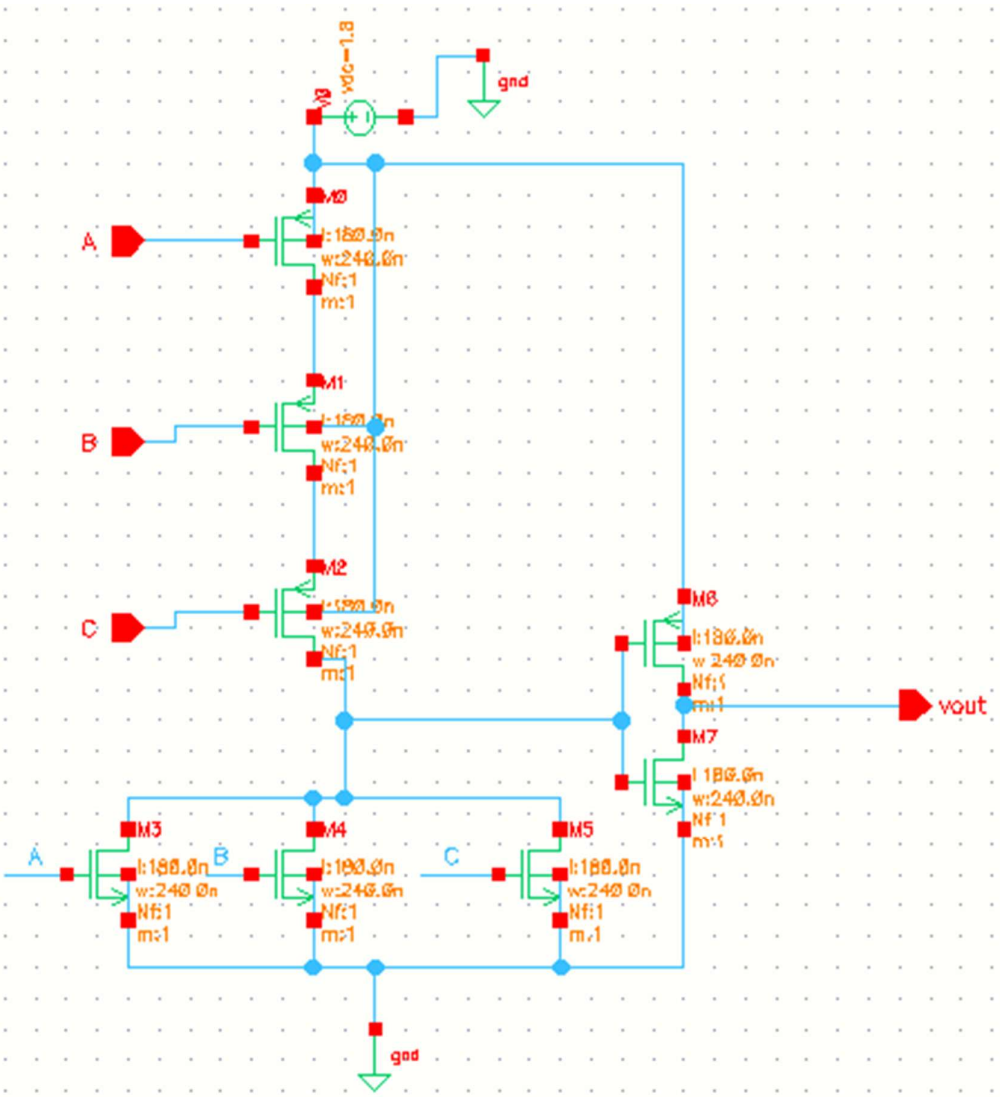
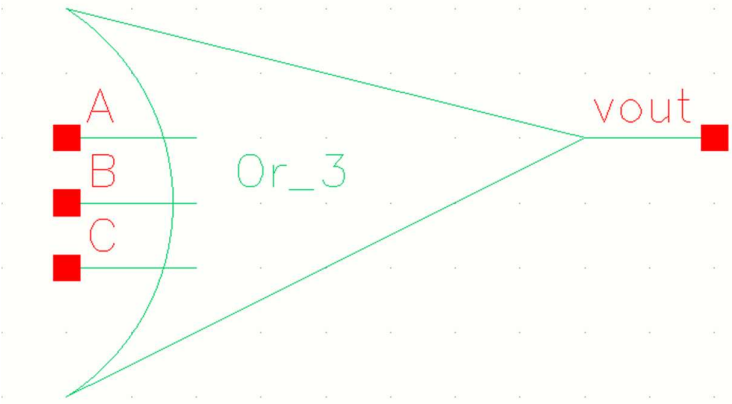


Figure 4. 3 Input OR Gate Symbol



3. 3 INPUT XOR GATE

Figure 5. 3 Input XOR Gate Schematic

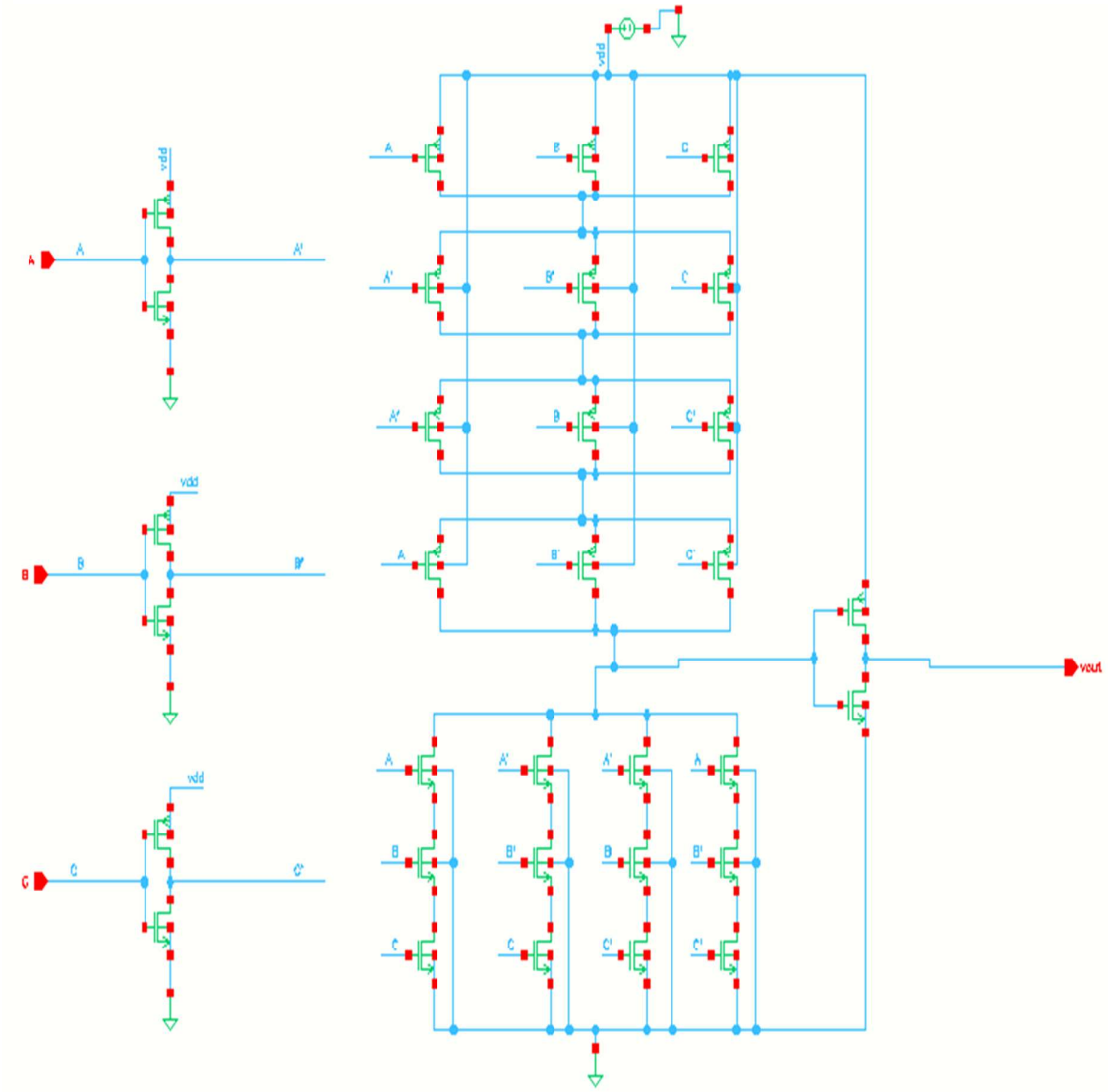
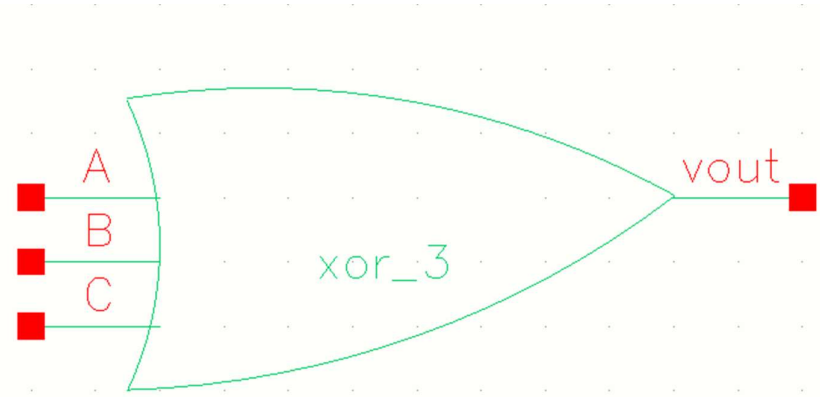


Figure 6. 3 Input XOR Gate Symbol



4. FULL ADDER

Figure 7. Full Adder Schematic

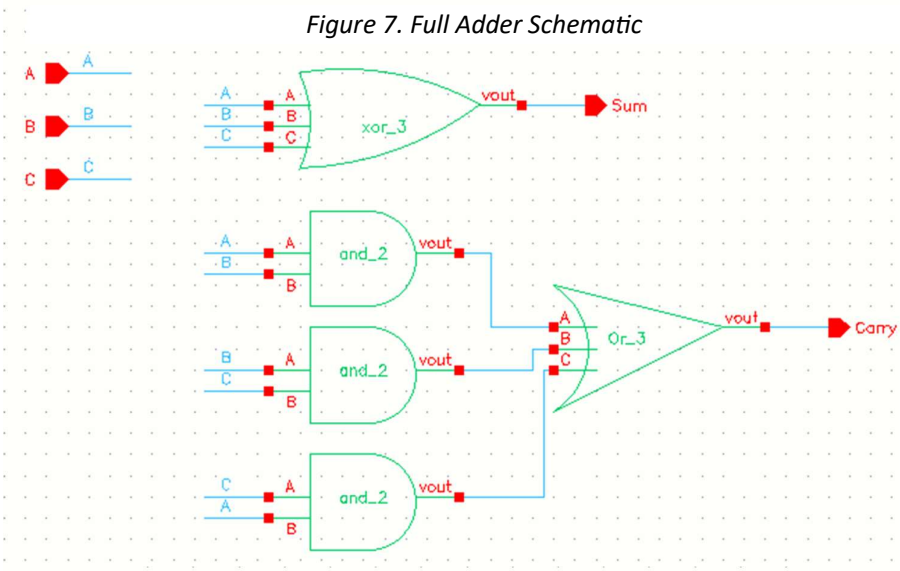


Figure 8. Full Adder Symbol

5. 4 BIT PARALLEL ADDER

Figure 9. 4 Bit Parallel Adder Schematic

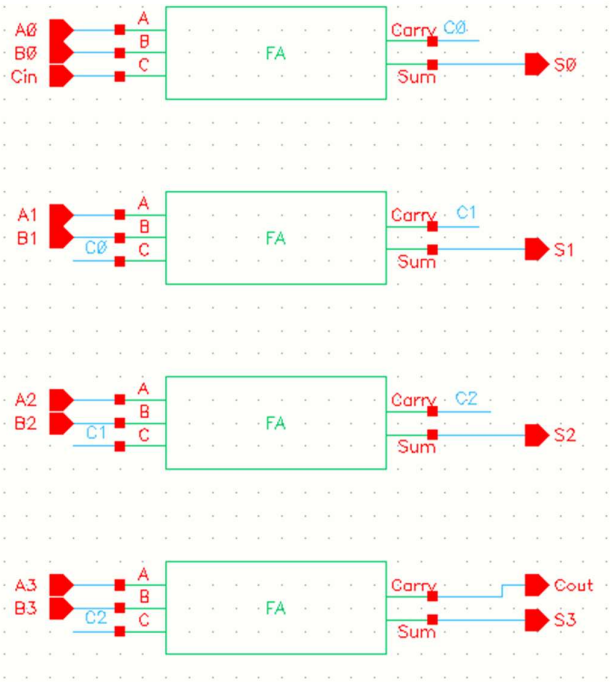


Figure 10. 4 Bit Parallel Adder Symbol

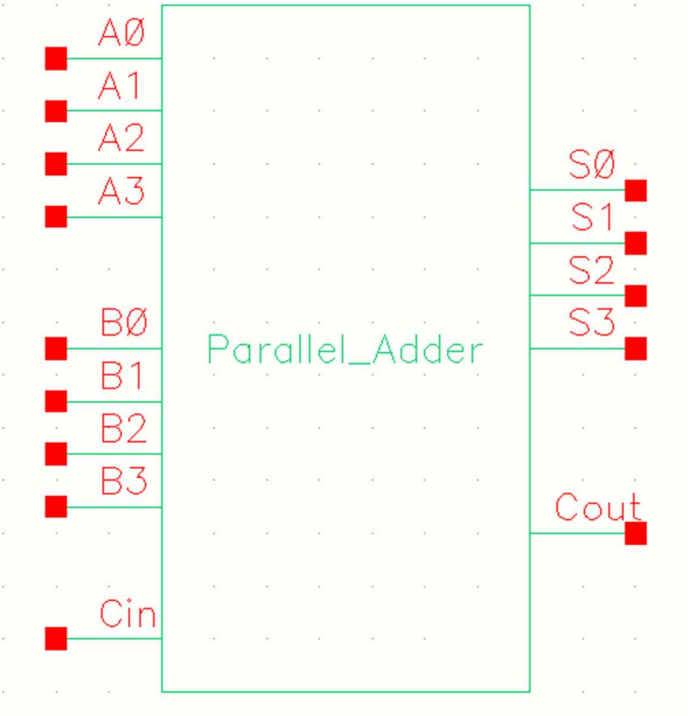


Figure 11. 4 Bit Parallel Adder Test Schematic

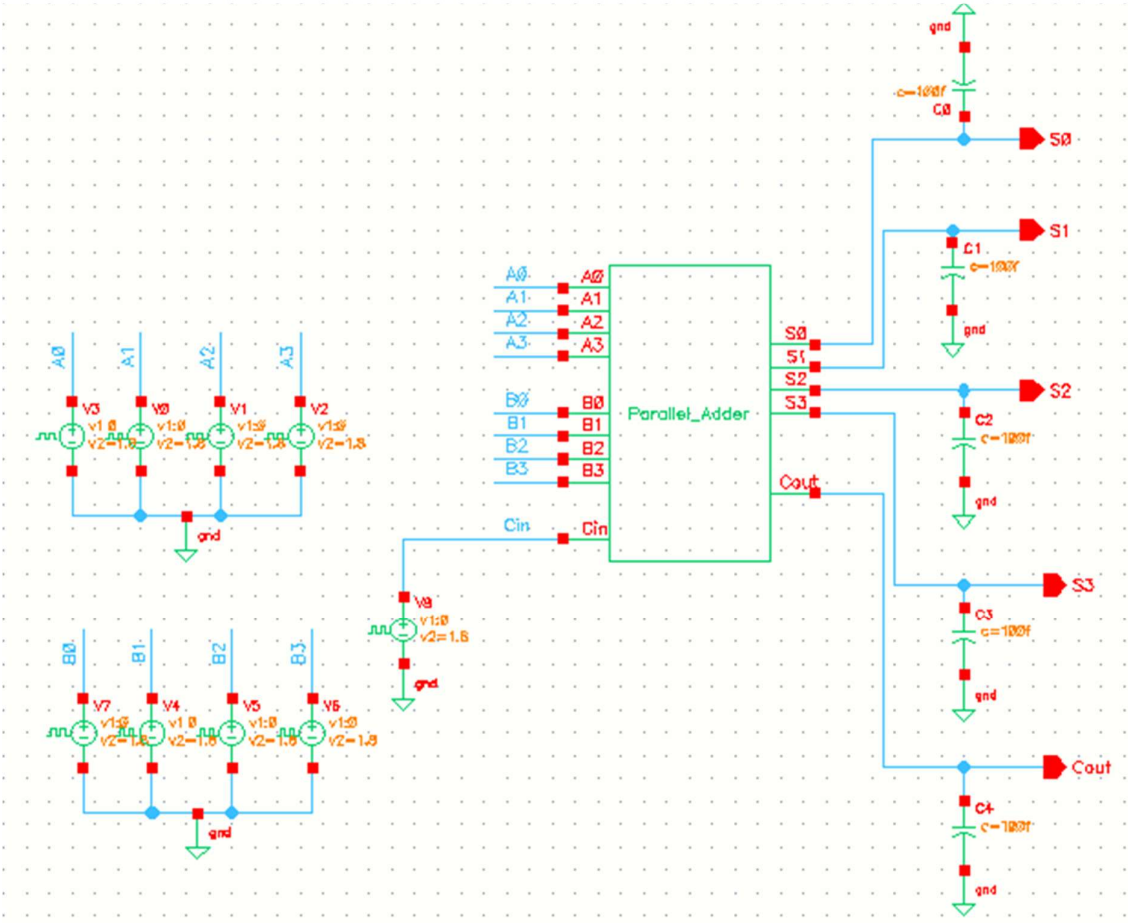
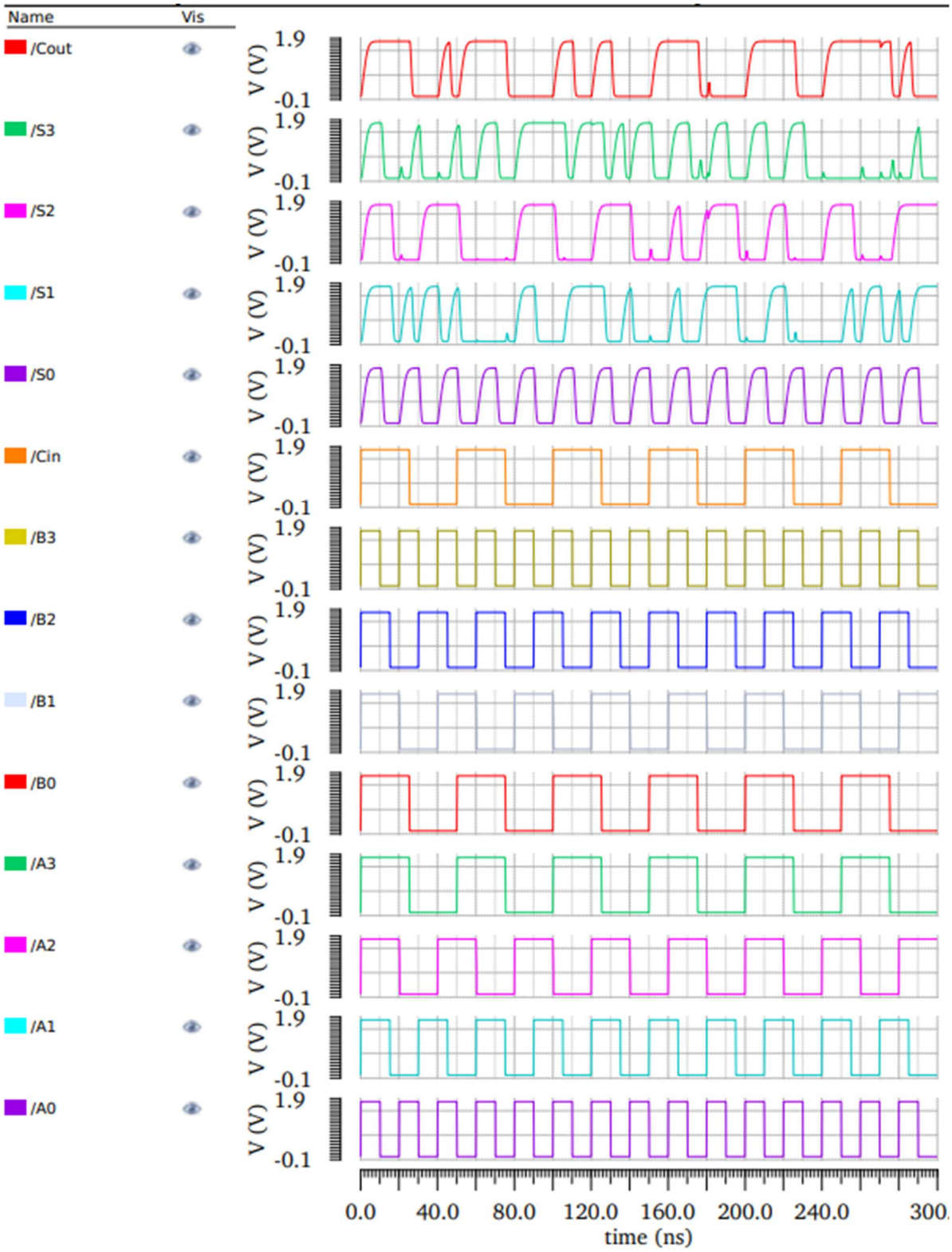


Figure 12. Output



B. PSEUDO NMOS LOGIC :

1. 2 INPUT AND GATE

Figure 13. 2 Input AND Gate Schematic

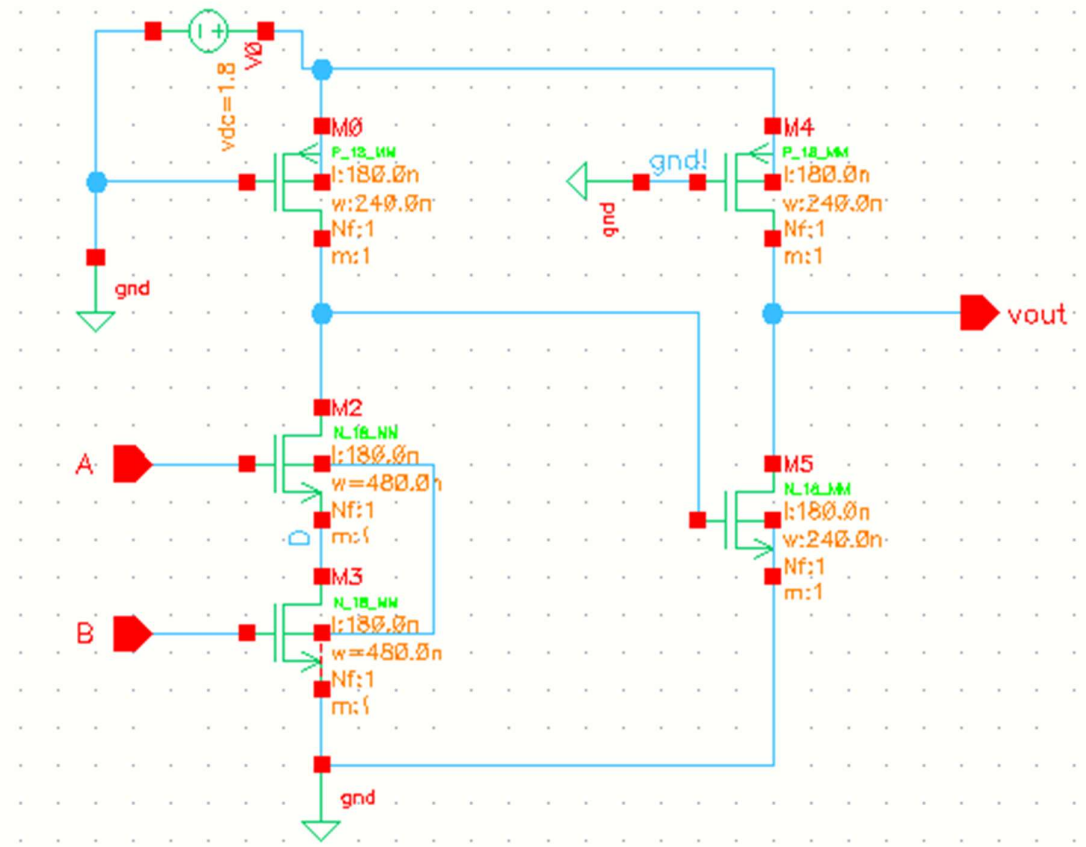
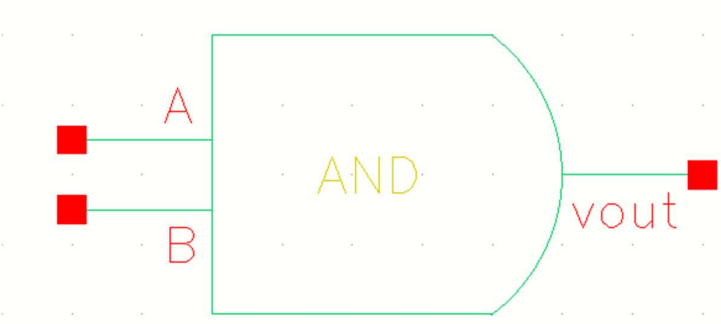


Figure 14. 2 Input AND Gate Symbol



2. 3 INPUT OR GATE

Figure 15. 3 Input OR Gate Schematic

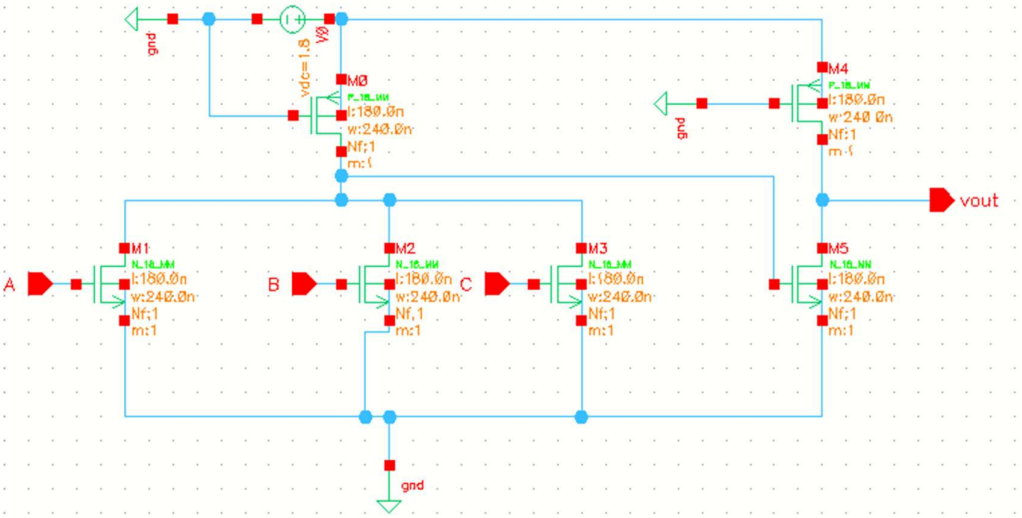
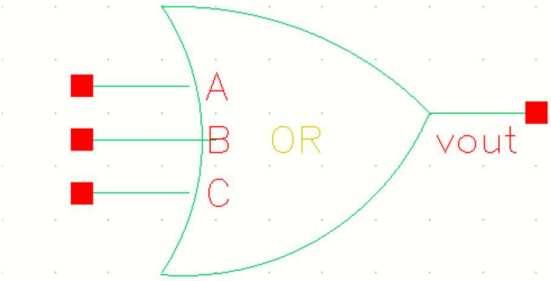


Figure 16. 3 Input OR Gate Symbol



3. 3 INPUT XOR GATE

Figure 17. 3 Input XOR Gate Schematic

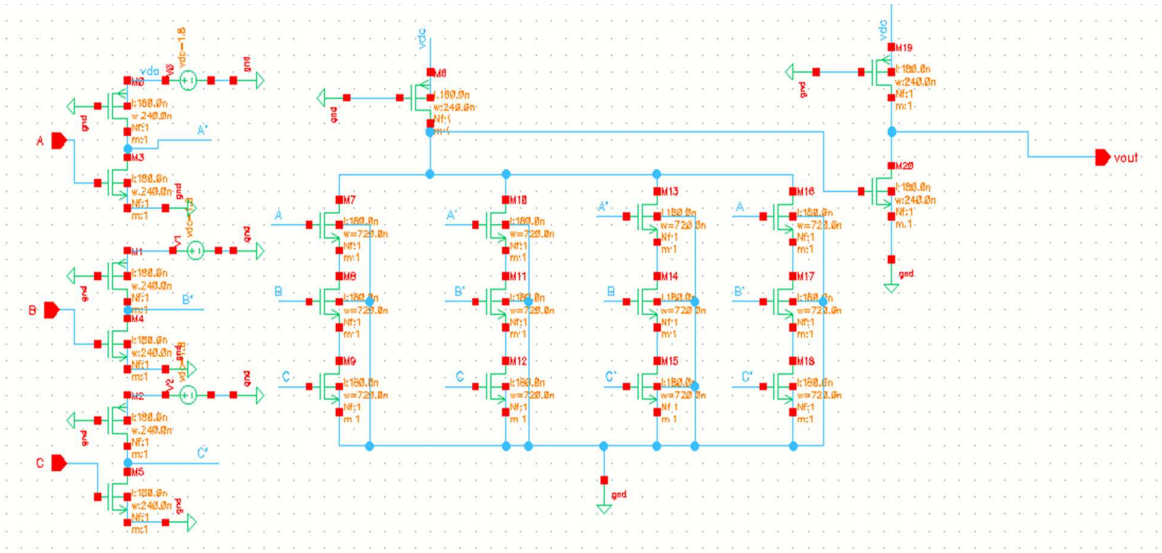
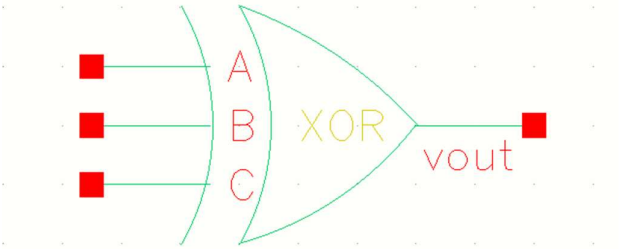


Figure 18. 3 Input XOR Gate Symbol



4. FULL ADDER

Figure 19. Full Adder Schematic

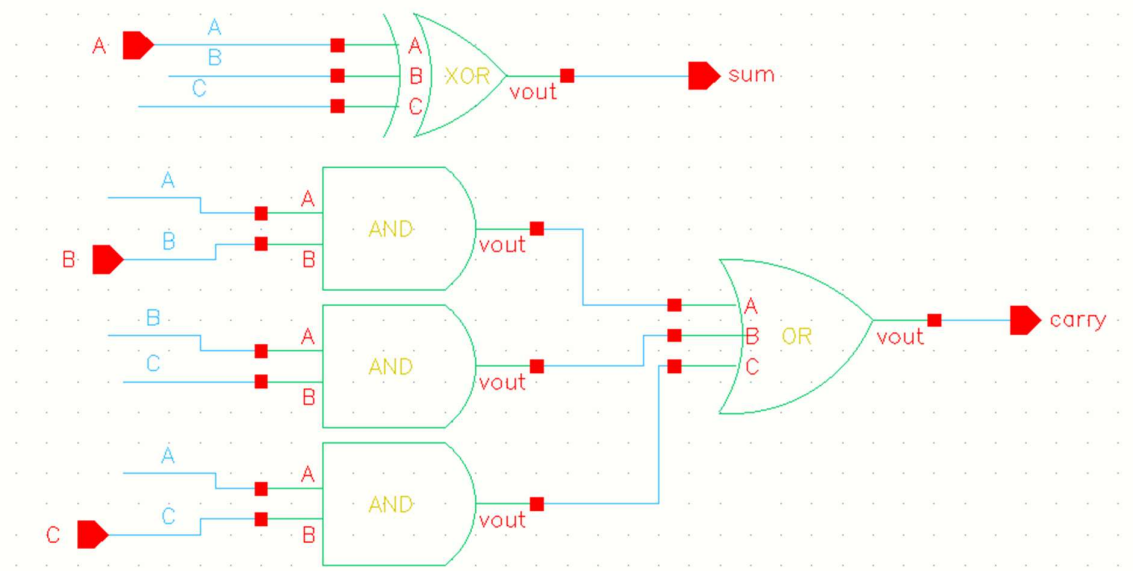
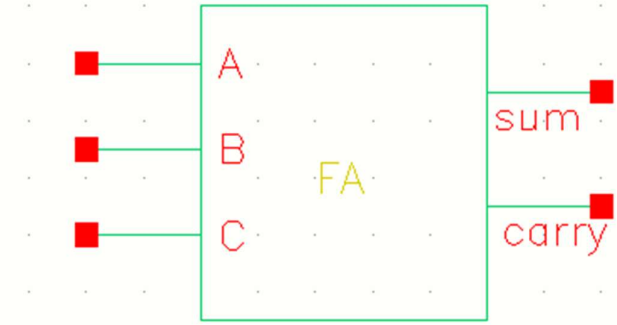


Figure 20. Full Adder Symbol



5. 4 BIT PARALLEL ADDER

Figure 21. 4 Bit Parallel Adder Schematic

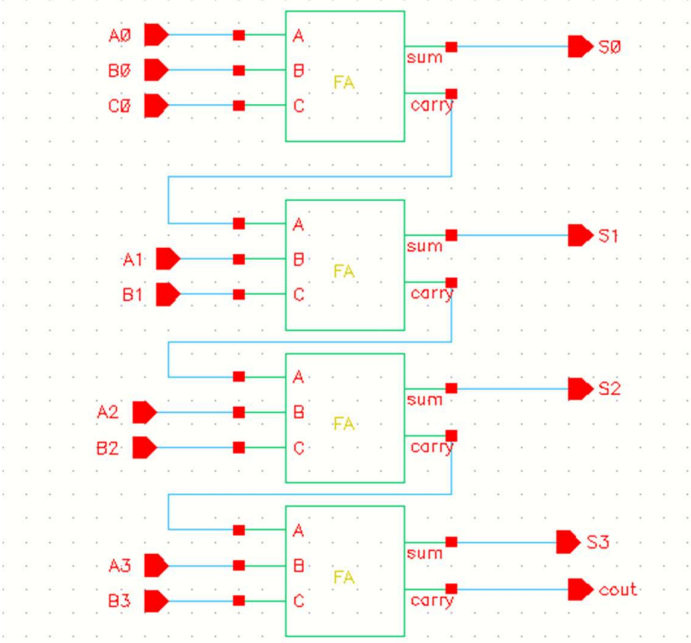


Figure 22. 4 Bit Parallel Adder Symbol

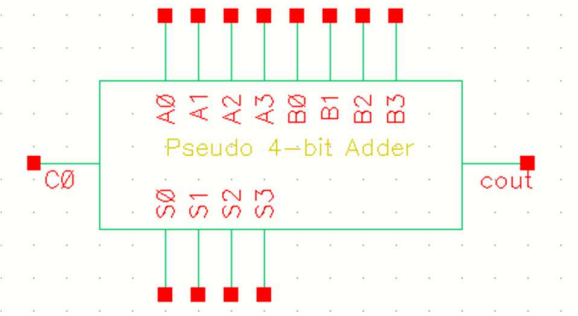


Figure 33. 4 Bit Parallel Adder Test Schematic

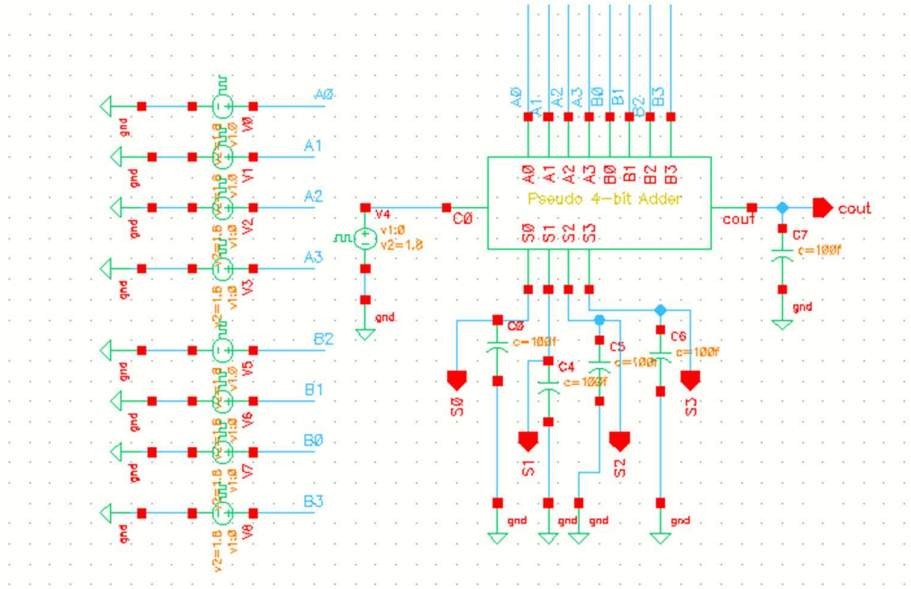
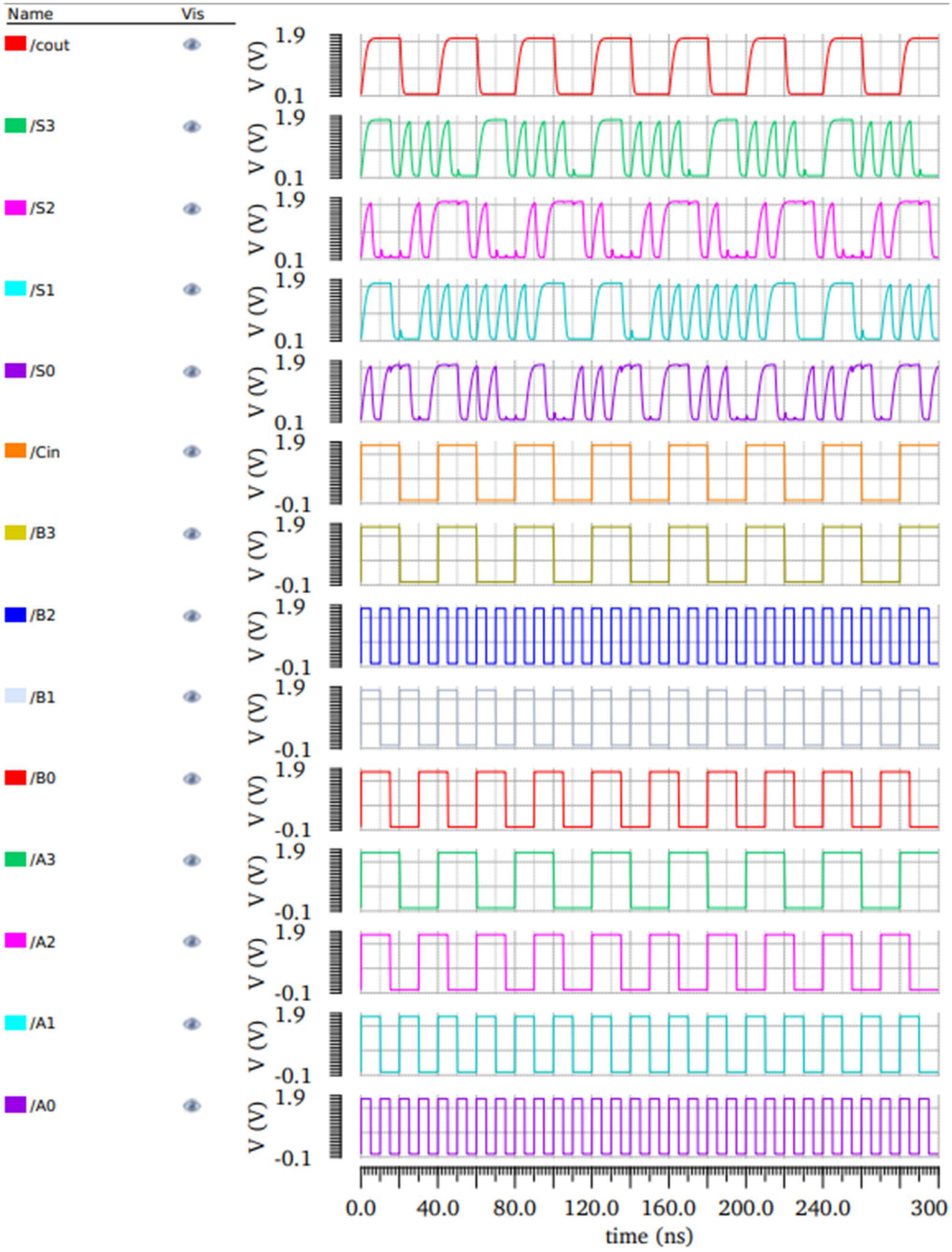


Figure 24. Output



C. COMPARISION

		CMOS LOGIC	***NMOS LOGIC***
Rise Time	**S0**	*3.597 n s*	*3.547 n s*
	S1	*3.633 n s*	*3.613 n s*
	S2	*3.638 n s*	*3.569 n s*
	S3	*3.631 n s*	*3.574 n s*
	Cout	*3.563 n s*	*3.573 n s*
Fall Time	**S0**	*1.346 n s*	*2.156 n s*
	S1	*1.346 n s*	*2.148 n s*
	S2	*1.297 n s*	*2.157 n s*
	S3	*1.299 n s*	*2.145 n s*
	Cout	*1.121 n s*	*2.102 n s*
Power	**S0**	*818.7 m Watt*	*904.1 m Watt*
	S1	*805.8 m Watt*	*906 m Watt*
	S2	*861.7 m Watt*	*897.6 m Watt*
	S3	*844.7 m Watt*	*903 m Watt*
	Cout	*876 m Watt*	*970.9 m Watt*
Area	-	*NMOS - 116* *PMOS - 116*	*NMOS - 116* *PMOS - 52*

D. CONCLUSION

By observing the table, we can conclude that CMOS Logic outperforms Pseudo NMOS Logic regarding speed (rise and fall time) and power consumption. Therefore, CMOS Logic can be used in applications where there is a requirement for low power consumptions and faster while Pseudo NMOS Logic is preferable in scenarios where minimizing area is crucial, since the number of transistors used are comparatively less.