Design and Implementation of UART

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Problem statement

Design the UART based on the specifications floated by the industry and implement it on the Arty-7 FPGA board.

Objectives

1. To design a UART system in Verilog that adheres to industry-specified parameters.
2. To implement it on the ARTY-7 FPGA platform to validate the functionality.
3. To ensure the UART meets all specified baud rates, data bit configurations, parity, and stop bit settings.

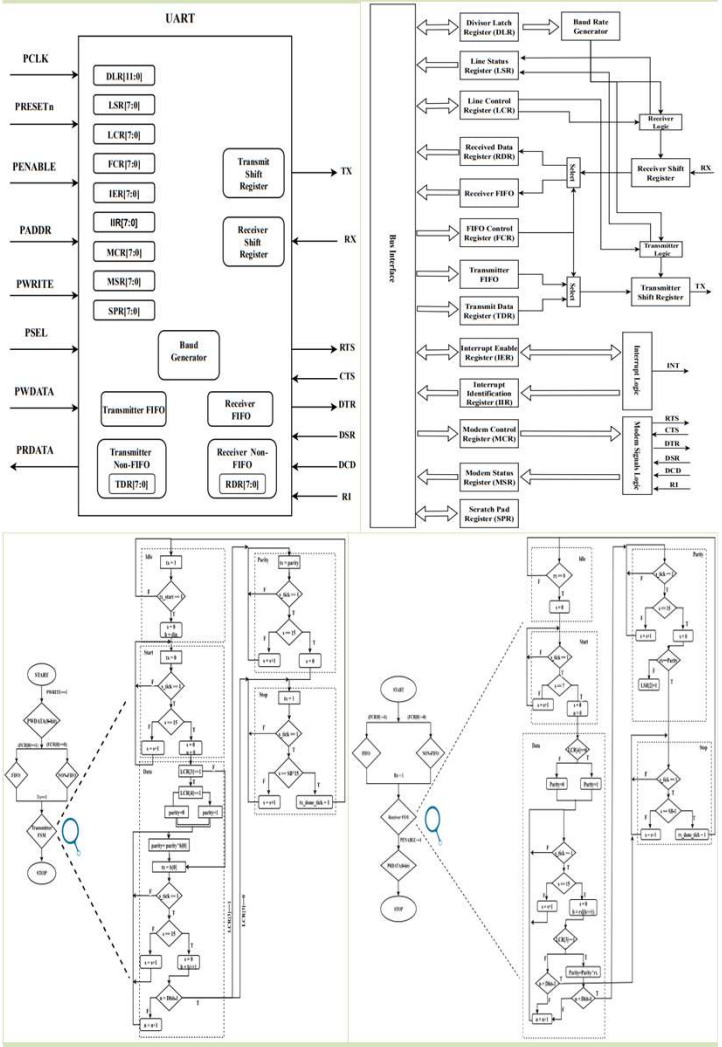
Contributions

Ensured compatibility with various baud rates, data bits, stop bits, and parity settings, providing flexibility for different applications. Conducted thorough verification using simulation tools to validate functionality and performance. Conducted hardware testing to confirm the module's performance in real-world scenarios.

Literature survey

- TI KeyStone Architecture UART User Guide: provides a comprehensive overview of the UART module.
- UART16550 Core Technical Manual.

Proposed Framework



Results and Discussion

- The UART module successfully transmitted and received data at various baud rates, ranging from 9600 to 115200 bps, without any data loss or corruption.
- Integration of the UART module into an FPGA (Field-Programmable Gate Array) platform was successful, with the module operating correctly in hardware tests.
- The module provided clear status indicators and error flags, aiding in debugging and system monitoring.
- The project produced valuable educational materials, including detailed documentation and example code.
- Compatibility with standard communication protocols and peripheral devices was confirmed, ensuring wide applicability in embedded systems and communication interfaces.

Conclusions

The project successfully delivered a robust, efficient, and flexible UART module, contributing valuable insights and resources to the field of serial communication.