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Thin-film synthesis of superconductor-on-insulator A15 vanadium silicide

Wenrui Zhang¹, Anthony T. Bollinger², Ruoshui Li^{1,3}, Kim Kisslinger¹, Xiao Tong¹, Mingzhao Liu^{1✉} & Charles T. Black^{1✉}

We present a new method for thin-film synthesis of the superconducting A15 phase of vanadium silicide with critical temperature higher than 13 K. Interdiffusion between a metallic vanadium film and the underlying silicon device layer in a silicon-on-insulator substrate, at temperatures between 650 and 750 °C, favors formation of the vanadium-rich A15 phase by limiting the supply of available silicon for the reaction. Energy dispersive X-ray spectroscopy, X-ray photoelectron spectroscopy, and X-ray diffraction verify the stoichiometry and structure of the synthesized thin films. We measure superconducting critical currents of more than 10⁶ amperes per square centimeter at low temperature in micron-scale bars fabricated from the material, and an upper critical magnetic field of 20 T, from which we deduce a superconducting coherence length of 4 nm, consistent with previously reported bulk values. The relatively high critical temperature of A15 vanadium silicide is an appealing property for use in silicon-compatible quantum devices and circuits.

In the early 1950s, the cubic A15 phase (A₃B) was discovered to be superconducting, with the notable example of A15 vanadium silicide (V₃Si) briefly having the highest known critical temperature (T_c) of any material (17.1 K)^{1,2}. Other A15 superconductors were soon found to have higher T_c [e.g., Nb₃Sn (18 K)³, Nb₃Ge (23 K)⁴], and the later discovery of cuprate perovskites^{5,6} heralded an era of intense study of so-called high- T_c superconductivity—leaving the material V₃Si largely unexplored. As a silicide, V₃Si is also appealing for its compatibility with silicon technology. In microelectronic devices, transition metal silicides are thoroughly studied and used for low-resistance metallic contacts to field-effect transistors^{7–10}. V₃Si is an *s*-wave, type-II superconductor with isotropic energy gap, suitable for superconducting devices such as Josephson junctions and superconducting quantum interference devices (SQUIDs)^{11,12}. Furthermore, geometrical lattice matching analysis shows that V₃Si forms a high-quality, epitaxial interface with Si with very small lattice mismatch (0.4%) and common cell area (40 Å²)¹³.

In this work, we report a new method for synthesis of phase pure, superconducting V₃Si thin films on silicon dioxide/silicon substrates (SiO₂/Si)—a process amenable to fabrication of superconductor-on-insulator devices leveraging silicon technology, and potentially compatible with silicon CMOS fabrication. In the bulk, V₃Si is typically synthesized by melting together a stoichiometric mixture (3:1) of elemental vanadium (V) and Si in an inert atmosphere¹⁴. Thin films have been previously prepared by vapor phase deposition, including electron-beam co-evaporation of V and Si¹⁵, magnetron sputtering from a stoichiometric target¹⁶, and molecular beam epitaxy¹⁷. In silicon microelectronics, transition metal silicides are formed by silicidation—the process of annealing metal films deposited on silicon⁸. However, silicidation of V deposited on Si typically forms the Si-rich vanadium silicide phase (VSi₂), which is not superconducting, due to the excess supply of available Si during the reaction^{18,19}. Silicidation of V deposited on thermally-grown SiO₂ can form the A15 phase V₃Si under the right conditions^{18,19}, presumably because diffusion of Si out of SiO₂ is slow enough to permit formation of the V-rich phase. However, this process also results in oxygen from the SiO₂ reacting with V to form vanadium oxides that are mixed with V₃Si in the final structure.

Results and discussion

Thin film synthesis. Here, we synthesize phase-pure, vanadium-rich V₃Si thin films by silicidation, by reacting only the thin Si device layer of a silicon-on-insulator (SOI) wafer (Fig. 1). By optimizing the silicidation anneal conditions, we completely convert the Si device layer into V₃Si without reacting with the underlying SiO₂,

¹Center for Functional Nanomaterials, Brookhaven National Laboratory, Upton, NY 11973, USA. ²Condensed Matter Physics and Materials Science Division, Brookhaven National Laboratory, Upton, NY 11973, USA. ³Department of Chemistry, Stony Brook University, Stony Brook, NY 11794, USA. ✉email: mzliu@bnl.gov; ctblack@bnl.gov

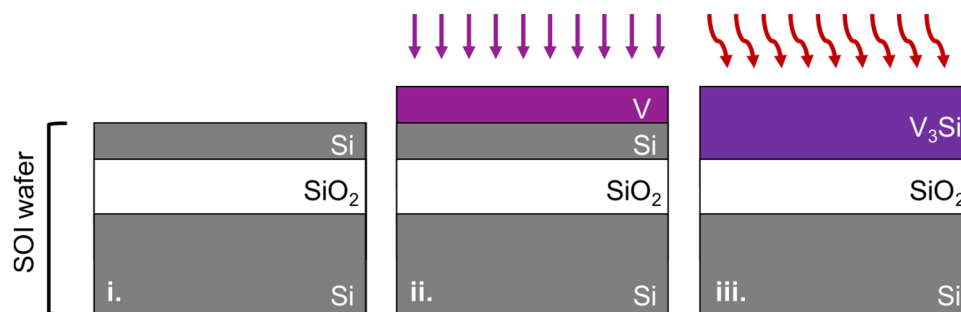


Figure 1. Thin-film synthesis of A15 vanadium silicide on insulator. **(i)** Silicon on insulator (SOI) substrate. **(ii)** Vanadium deposition by thermal evaporation. **(iii)** Silicidation by annealing in vacuum.

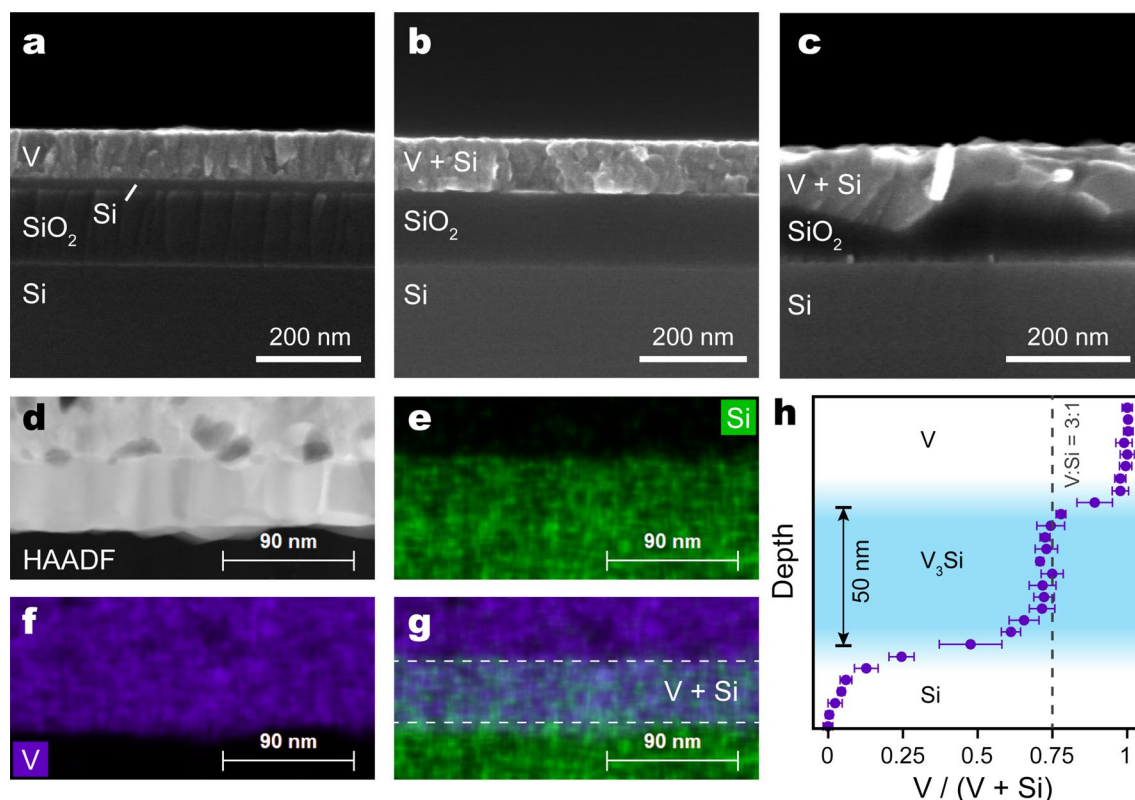


Figure 2. Cross-sectional SEM images of: **(a)** V film deposited onto a SOI substrate, and similar samples after annealing in vacuum at **(b)** 700 °C and **(c)** 900 °C. **(d)** HAADF STEM image of the film annealed at 700 °C. **(e, f)** EDX mapping of the area shown in **(d)**, denoting location of **(e)** Si and **(f)** V. **(g)** Overlapped maps **(e)** and **(f)** show the vanadium silicide region contains both V and Si. **(h)** Quantitative EDX analysis shows a 3:1 V:Si ratio within the V_3Si layer.

leaving a sharp and smooth V_3Si/SiO_2 interface. In our experiments, we start with SOI wafers having a 20-nm Si (100)-oriented device layer on top of a 140 nm thick thermal SiO_2 . Stoichiometric conversion of the entire 20 nm thick Si layer to V_3Si by silicidation requires the number of V atoms supplied by a 42 nm thick film (see “Methods” section). Most typically, we deposit 90 nm of V—which provides an oversupply of V to ensure complete silicidation of the Si device layer. Prior to annealing, we observe a sharp V/Si interface from cross-sectional scanning electron microscope (SEM) images (Fig. 2a). The samples are annealed in high vacuum (10^{-7} Torr) for 15 min, at temperatures (T) ranging from 650 °C to 900 °C. The V/Si interface disappears after annealing at sufficiently high temperature (Fig. 2b), due to V-Si interdiffusion. Silicidation at $T = 800$ °C or lower maintains a sharp, smooth interface at the underlying SiO_2 layer, while higher T roughens this interface, indicating a reaction with the SiO_2 (Fig. 2c).

Scanning transmission electron microscopy (STEM) reveals more details of the silicidation process. High-angle annular dark field (HAADF) cross-sectional images of a sample annealed at 700 °C (Fig. 2d–f) show two distinct regions within the V-Si layer: an upper, porous region and an underlying, denser layer (Fig. 2d).

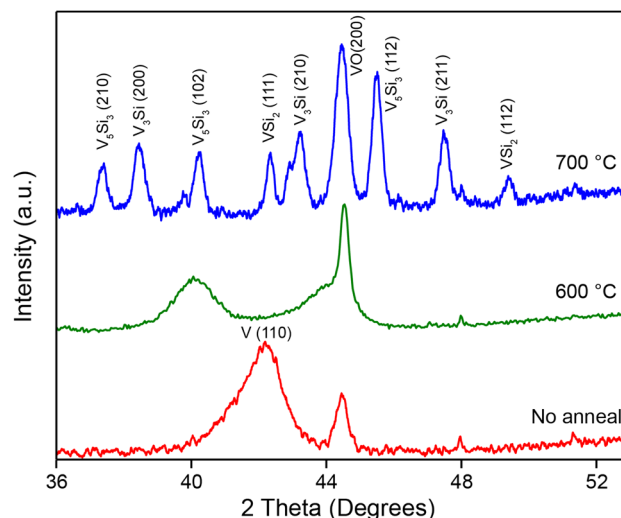


Figure 3. X-ray diffraction spectra (XRD) of V films deposited on SOI, before annealing, and after vacuum annealing at 600 °C and 700 °C. The pattern after annealing at 700 °C shows the formation of the A15 V_3Si phase. The 600 °C pattern shows a transition from metallic V to vanadium silicide. Due to exposure to air during sample handling, vanadium oxide (VO) is also formed and evident in the diffraction patterns.

Energy dispersive X-ray spectroscopy (EDX) shows that the top layer is pure V and the bottom layer contains both V and Si (Fig. 2e–g), consistent with our supplying excess V for the silicidation reaction. The porosity of the V layer is a result of deposition by thermal evaporation, as deposited V atoms quickly lose kinetic energy on the cold substrate and have insufficient mobility to form close-packed films. Quantitative analysis of the EDX maps shows that the bottom layer contains V and Si in a 3:1 ratio (Fig. 2h). X-ray diffraction (XRD) confirms formation of the A15 phase of V_3Si for samples annealed at 700 °C, along with impurities of VSi_2 and V_5Si_3 (Fig. 3). Annealing at 600 °C shifts the broad V (110) peak at 42° to 40°, which is matched to V_5Si_3 (102) but is very broad and likely reflects an intermediate amorphous phase formed during interdiffusion. The presence of VO (200) peak in all samples suggests partial oxidation of the deposited V due to air exposure. For any sample annealed at less than 800 °C, we do not expect reaction between vanadium and SiO_2 , which is evident from the sharp interface between the V/Si layer and the SiO_2 layer (Fig. 2b). According to the EDX maps, the V_3Si layer is about 50 nm in thickness, which matches closely the thickness expected from stoichiometric conversion of Si (52 nm, see “Methods” section). The dense V_3Si layer suggests that V is the predominant diffusion species, i.e., that silicidation occurs primarily by V diffusing into the Si lattice. Significant Si diffusion would result in the silicide inheriting the porous appearance of the deposited V layer. Our observation is consistent with those of previous studies, which noted an ‘ordered Cu_3Au rule’²⁰, suggesting that majority atoms are the most mobile ones in the class of A_3B compounds²¹.

Profiling the vanadium silicide film by sequential argon ion milling and X-ray photoelectron spectroscopy (XPS) verifies its composition (Fig. 4). The film top surface is composed of excess V that has been oxidized upon air exposure, with the V $2p_{3/2}$ peak positioned at 515.6 eV, corresponding to a V^{3+} oxidative state (Fig. 3a, black color). Beginning with spectra taken from 12 nm below the top surface, this peak shifts to 513 eV, which corresponds to elemental V (Fig. 4a, red color). The emergence of the Si $2p$ peak at 99.0 eV (Fig. 4b, green color) at a depth of 70 nm and beyond indicates the conversion to V_3Si . In this region, the Si $2p$ peak position is very close to elemental Si (99.4 eV), while the V $2p_{3/2}$ peak remains at 513 eV, consistent with the metallic nature of V in A15 V_3Si ²². By analyzing the peak areas and sensitivity factors associated with V $2p_{3/2}$ and Si $2p$ elements in the V_3Si region, at a depth of 77 nm (Fig. 4, blue color), the relative elemental ratio between V and Si is obtained at 3:1, consistent with EDX measurements (Fig. 2h). The O 1s peak at 531 eV across all depths indicates the presence of vanadium oxide (VO) in both metallic V and vanadium silicide region due to exposure to air.

Transport measurements. Four-probe resistance measurements of V_3Si films versus T reveal their metallic nature and the superconducting transition temperature (T_c). We measure the film in-plane resistance using a constant-current bias of 50 μA and vary T at a rate of ~ 1 K min^{-1} with no magnetic field. The sheet resistance of a 50 nm thick V_3Si film silicided at 700 °C decreases from 2.8 to 1.0 Ω/sq upon cooling from room T to 20 K, a resistance ratio of 2.8 (Fig. 5a, inset). These values reflect the parallel normal state resistance of both the V_3Si and the overlaying metallic V layer (also about 50 nm thick). At $T_c = 13.75$ K, the film resistance abruptly decreases to zero with a transition width of 0.3 K, marking the onset of superconductivity. Films silicided at T between 650 and 750 °C all showed superconducting transitions, with T_c decreasing with decreasing silicidation T (Fig. 5a). We do not observe a superconducting phase transition in films silicided at $T \leq 600$ °C measured to temperatures as low as 4 K (Fig. 5a, inset). The critical current density is determined from voltage-current measurements of strips fabricated from V_3Si thin film annealed at 700 °C. The strips are 30 μm in width and are patterned using photolithography, with etching performed in an argon ion mill (2.5 mA/cm² beam density), and electrical con-

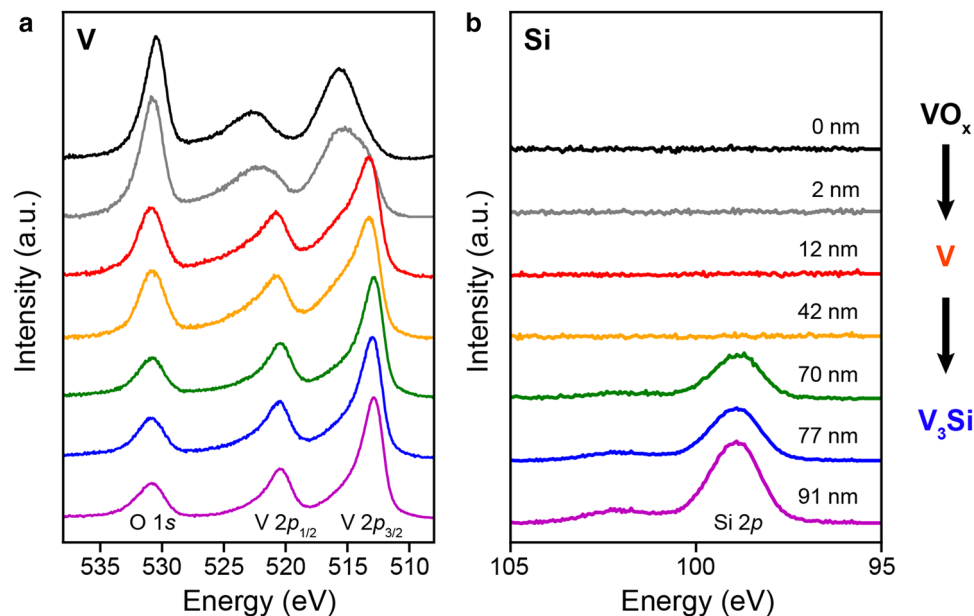


Figure 4. Depth-profiled X-ray photoelectron spectra of a V_3Si thin film, probed from the film top surface (upper curve) toward the bottom (lower curve). (a) the V 2p and O 1s levels, and (b) the Si 2p level. Depth-profiling is carried out by Ar ion milling. The depth values are calculated by assuming a uniform ion mill rate. Offsets are applied for clarity of viewing.

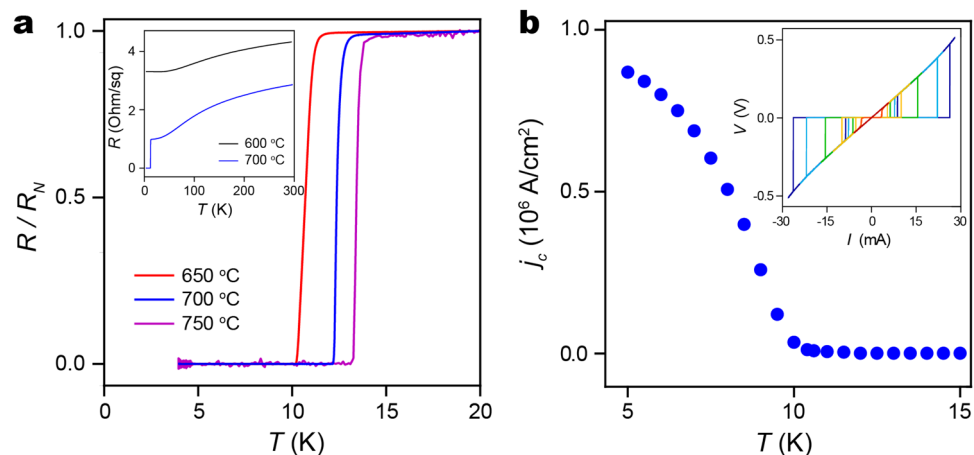


Figure 5. (a) Electrical resistance versus temperature with no magnetic field, for vanadium silicide films annealed at 650 °C (red), 700 °C (blue), and 750 °C (magenta), normalized against normal state resistance at 20 K (inset). Electrical resistance from room temperature to 4 K, for vanadium silicide films annealed at 600 °C (black) and 700 °C (blue). No superconductivity is observed in the 600 °C sample, consistent with the absence of a V_3Si phase. (b) Critical current density (j_c) of a 30 μm wide bar fabricated from V_3Si thin film annealed at 700 °C (inset). Representative voltage-current curves used to determine the critical current density ($T = 5$ –15 K).

tacts deposited by e-beam evaporation of 10 nm titanium and 300 nm gold. The voltage-current behavior of strips patterned from a V_3Si film change from linear behavior above T_c to non-linear near the superconducting transition (Fig. 5b, inset). Films display sharp, fully developed, critical currents at $T < T_c$, which increase as T is further reduced. At $T = 5$ K, the critical current density (j_c) is 8.7×10^5 A cm^{-2} , slightly higher than previous reports taken on V_3Si single crystals²³. This is likely due to the presence of impurity phases acting as flux-pinning centers, which lead to the observed higher critical current densities. Because the T_c of metallic V is 5.4 K for single crystals²⁴, and lower for amorphous films deposited from the vapor phase²⁵, the only contributions from the 50-nm-thick amorphous V film to j_c that we would expect within the range of measured temperatures (5–15 K) is a proximity effect induced superconducting layer near the V_3Si that serves to increase the effective thickness that carries supercurrent, which is taken into account in the main panel of Fig. 5b.

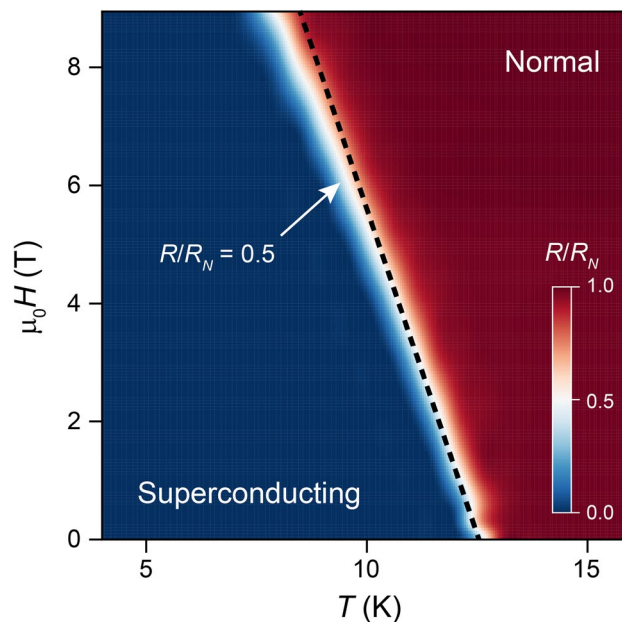


Figure 6. Magnetic field dependence of superconducting critical temperature. The white region separating the normal state (red) and superconducting state (blue) are separated by a thin white region denoting the upper critical field, $H_{c2}(T)$. A linear fit to $H_{c2}(T)$ near zero applied field (dashed line) is used to calculate $H_{c2}(0)$ using Eq. (1).

The A15 phase of vanadium silicide is a known type II superconductor that undergoes phase transitions at two different applied magnetic fields. At a lower critical magnetic field (H_{c1}) the superconducting order parameter is locally suppressed and the material supports magnetic vortices, and at an upper critical field (H_{c2}) the material reverts to the normal state. We measured the V_3Si film resistance versus T in a series of increasing applied magnetic fields (H) in order to determine $H_{c2}(0)$, the upper critical field at 0 K. The T_c of a V_3Si film silicided at 700 °C and having $T_c(0) \sim 13$ K is continuously suppressed with increasing magnetic field (Fig. 6). For each H , we determine the corresponding $T_c(H)$ using the criteria $R/R_N = 0.5$ (midpoint T_c), where R_N is the normal state resistance. In the color map shown in Fig. 5, the dependence of H_{c2} on T appears as a narrow white region separating normal and superconducting behaviors. Because the highest magnetic fields available in our experiment (9 T) are insufficient to completely suppress superconductivity in our films, we deduce $H_{c2}(0)$ for the material indirectly using the Werthamer-Helfand-Hohenberg model, which gives:

$$H_{c2}(0) = -\frac{\pi^2 T_c(0)}{8e\gamma} \left. \frac{dH_{c2}}{dT} \right|_{T=T_c(0)}, \quad (1)$$

where $\gamma \approx 0.5772$ is Euler's constant²⁶. A linear fit to the $H_{c2} - T$ relation in the range of $0 \text{ T} < \mu_0 H_{c2} \leq 1 \text{ T}$ provides both the tangent term in Eq. (1) and zero field $T_c(0)$, respectively, as the slope and the T -axis intercept (Fig. 5). From this analysis, we obtain $\mu_0 H_{c2}(0) = 20 \text{ T}$, which is consistent with the previously-reported bulk value of $H_{c2} = 23.5 \text{ T}$ for V_3Si ²⁷. Knowing $H_{c2}(0)$, we can also calculate the superconducting coherence length $\xi(0)$ in our V_3Si to be 4 nm, using the relation $\mu_0 H_{c2}(0) = \Phi_0 / 2\pi \xi^2(0)$ ²⁸, where $\Phi_0 = h/2e$ is the magnetic flux quantum, also consistent with previous reports²⁹.

Summary and outlook

In summary, we have described a new method for synthesis of the A15 phase of vanadium silicide by silicidation of metallic vanadium layers deposited on silicon-on-insulator substrates. The limited supply of silicon available for silicidation facilitates formation of the superconducting, vanadium-rich A15 phase. V_3Si thin films synthesized on silicon-on-insulator substrates are type-II superconductors with $T_c > 13 \text{ K}$. The relatively high T_c is an appealing property for use in silicon-compatible quantum devices and circuits.

Methods

Fabrication of V_3Si thin films. The substrates, which are silicon-on-insulator (SOI) wafers with a 20 nm Si device layer and a 140 nm oxide SOI wafer, are dipped in a 10:1 buffered oxide etch (BOE) for 1 min to remove the native silicon oxide. Immediately after the oxide stripping, vanadium layers of different thicknesses are deposited by thermal evaporation in high vacuum ($\sim 10^{-7}$ Torr). After metal deposition, the substrate is annealed in high vacuum for 15 min, at temperatures ranging from 650 °C to 900 °C, to form V_3Si by V-Si interdiffusion.

Vanadium thickness for 3:1 V:Si stoichiometry. The molar volume (V_m) of a substance is given by $V_m = M/\rho$, where M and ρ are, respectively, the substance's molar mass and volumetric mass density. For crystalline Si, $M_{\text{Si}} = 28.085 \text{ g mol}^{-1}$ and $\rho_{\text{Si}} = 2.33 \text{ g cm}^{-3}$, which gives $V_{m, \text{Si}} = 12.05 \text{ cm}^3 \text{ mol}^{-1}$. For V metal, $M_{\text{V}} = 50.94 \text{ g mol}^{-1}$ and $\rho_{\text{V}} = 6.0 \text{ g cm}^{-3}$, which gives $V_{m, \text{V}} = 8.49 \text{ cm}^3 \text{ mol}^{-1}$. As such, the stoichiometric conversion of one unit volume of Si to V_3Si requires $3 \times V_{m, \text{V}}/V_{m, \text{Si}} = 2.11$. For a 20 nm layer of Si, this corresponds to 42 nm of V. After the conversion, with $M_{\text{V}_3\text{Si}} = 180.9 \text{ g mol}^{-1}$ and $\rho_{\text{V}_3\text{Si}} = 5.77 \text{ g cm}^{-3}$, a similar calculation gives an expected thickness of 52 nm for the V_3Si layer.

Scanning transmission electron microscopy (STEM) imaging. The specimen for STEM studies is a 40 nm-thick vertical cross-sectional slice of the silicide film mounted on a copper grid using the in situ focused ion beam milling and lift-out technique (Helios 600 dual beam FIB). High-angle annular dark field (HAADF) and energy dispersive X-ray spectroscopy (EDX) mapping images are collected over the same area simultaneously, using an FEI Talos F200X microscope.

Transport measurements on V_3Si thin films. Electrical transport measurements are performed in either a closed-cycle cryocooler or a top loading He-3 cryostat equipped with a 9 T magnet. Resistance is determined by delta mode averaging with a DC bias current provided by a source meter and sample voltage measured with a nanovoltmeter. Measurements of the T -dependence of the upper critical field are made by constant field temperature sweeps and verified by constant temperature magnetic field sweeps. The critical current density is determined from voltage-current measurements of strips fabricated from V_3Si thin film annealed at 700 °C. The strips are 30 μm in width and are patterned by standard photolithography, with etching performed in an argon ion mill (2.5 mA/cm² beam density), and electrical contacts deposited by e-beam evaporation of 10 nm Ti and 300 nm Au, followed by liftoff.

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Author contributions

C.T.B. and M.L. designed the study. W.Z., R.L., and M.L. deposited and prepared the samples. A.B. conducted low temperature transport characterization and data analysis. K.K. prepared cross-sectional TEM specimens and performed TEM analysis. X.T. performed XPS analysis. W.Z., R.L., M.L., and C.T.B. wrote the manuscript. All the authors discussed the results and reviewed the manuscript.

Competing interests

Two authors (C. T. B. and M. L.) are named inventors on a provisional patent application filed by Brookhaven Science Associates, application number US2019-005-01, currently under evaluation by the US Patent Office. Part of that application details the silicide synthesis method described in this manuscript. All other authors do not have any conflict of interest.

Additional information

Correspondence and requests for materials should be addressed to M.L. or C.T.B.

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