IR-aware Power Net Routing for Multi-Voltage Mixed-Signal Design

Shuo-Hui Wang, Guan-Hong Liou, Yen-Yu Su, and Mark Po-Hung Lin
Department of Electrical Engineering and Advanced Institute of Manufacturing with High-tech Innovations
National Chung Cheng University
Chiayi, Taiwan

***Abstract*—Modern mixed-signal design usually contains multiple power signals with different supply voltages driving different sets of mixed-signal circuit blocks. As the process technology advances to nanometer era, IR drop becomes very significant, which may have great impact on circuit performance and reliability. Insufficient power supply to a circuit block will lead to performance degradation or even functional failure. Although such IR-drop problem can be minimized by widening metal wires or applying mesh routing structures of the power network, excessive metal usage of those power nets with different supply voltages will significantly increase both chip area and cost. This paper presents a new IR-aware routing method to simultaneously route multiple power nets in a mixed-signal design with the considerations of routing congestion, routing tree splitting, wire tapering, and metal layer optimization. Experimental results show that the presented method can effectively reduce total metal usage and satisfy IR-drop constraints.**

I. Introduction

IR drop has great impact on circuit performance and reliability. It may lead to insufficient power supply of voltage signals because of excessive resistance on the nets delivering supply voltage. In modern mixed-signal design, there are usually multiple power supplies with different supply voltages for different circuit blocks. Although many previous works [1]–[5] optimize power delivery network (PDN) based on a mesh structure, such mesh structure is not suitable for multi-voltage mixed-signal design. It may waste too much routing resource by applying mesh structures for multiple power signals. On the contrary, the tree structure [6]–[9] is more desirable for constructing the PDN of each power supply in a mixed-signal design because the tree structure results in less metal usage and routing area. In order to save routing resource for mixed-signal design, it is desirable to minimize overall metal usage of multiple PDNs. Fig. 1 shows a routing instance of a multi-voltage mixed-signal design with ten circuit blocks driven by four different power nets, where the IR-drop constraint of each pin on a circuit block must be satisfied. In Fig. 1, each power net is routed with tapered wires, where the wires at the source of the routing tree are wider than those at the sinks. Higher metal layers are preferable because of lower sheet resistance, and hence resulting in less IR drop.

Although some recent works [10]–[13] tried to solve the IR-drop problem based on the tree structure with tapered wires, most of them only handle single-layer routing for one or two nets. They did not address the complicated multiple-power-net routing problem with many power supplies delivering different voltage signals to various pins on different mixed-signal circuit blocks with different IR-drop constraints. More specifically, they did not simultaneously consider routing congestion, routing tree splitting, and layer/width optimization of each wire segment. TABLE I summarizes the previous works on IR-aware routing, and our work.

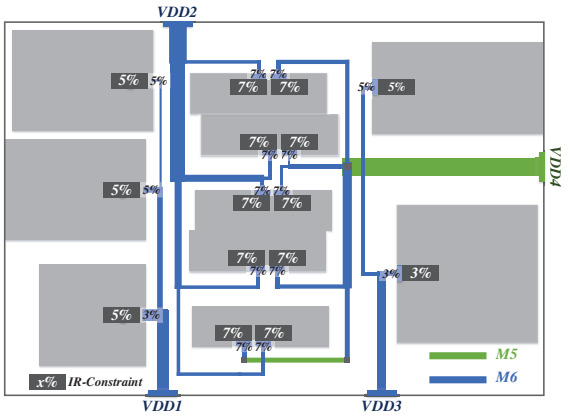

Fig. 1. A routing instance of a mixed-signal design with multiple power nets.

TABLE I
Comparison of IR-aware routing among recent works and ours

	[10]	[11]	[12]	[13]	Ours
Number of nets	One	One	Two (P/G)	Two (P/G)	Multiple
Routing objective	min WL	min WL	min WL	min WL	min Metal Usage
Wire tapering	Yes	Yes	Yes	Yes	Yes
Routing tree splitting	No	No	No	No	Yes
Routing congestion	No	Yes	No	No	Yes
Layer assignment	No	No	No	No	Yes

The contributions of this paper is summarized as follows:

- Instead of performing IR-aware routing for only one or two nets, we present a new IR-aware routing method to route multiple power nets simultaneously.
- Different from most of the previous works which aim to minimize total wirelength (WL), we propose to minimize total mental usage instead.
- Given an initial routing tree of each power net, we propose a nonlinear programming formulation to minimize total metal usage with wire tapering. We additionally introduce routing tree splitting and layer assignment methods to further minimize metal usage of all power nets while satisfying the given IR-drop constraints.

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- Experimental results show that the proposed approach integrating wire tapering, routing tree splitting, and layer optimization can effectively reduce total metal usage and satisfy IR-drop constraints.

The rest of this paper is organized as follows. Section II presents our problem formulation. Section III details the proposed method, including the flow and algorithms. Section IV demonstrates the experimental results, and finally, Section V concludes this paper.

II. Problem Formulation

We are given the following inputs:

- a circuit netlist containing multiple power nets;
- locations of all mixed-signal circuit blocks;
- N metal layers for power net routing;
- a set of routing blockages on each metal layer;
- design rules;
- sheet resistance, ρ_{M_i}, of each metal layer, M_i;
- the current value, I_{n_j}, and IR-drop constraint, ΔV_{p_k}, at each pin, p_k, connected by the power nets, n_j.

The problem is to complete the routing of all power nets with minimized total metal usage while satisfying all the IR-drop constraints. The total metal usage, Φ, of a routing solution is evaluated by the following equation:

$$\Phi = \sum_{i=1}^{N} A_{M_i}, \tag{1}$$

where A_{M_i} is the total area of M_i used for the whole power net routing.

III. The Propose Method

To solve the aforementioned problem, we propose an IR-aware multiple-power-net routing flow, as shown in Fig. 2, which consists of four major steps: (1) congestion-aware multiple power net routing, (2) IR-aware routing tree splitting, (3) IR-aware wire tapering, and (4) IR-aware metal layer optimization.

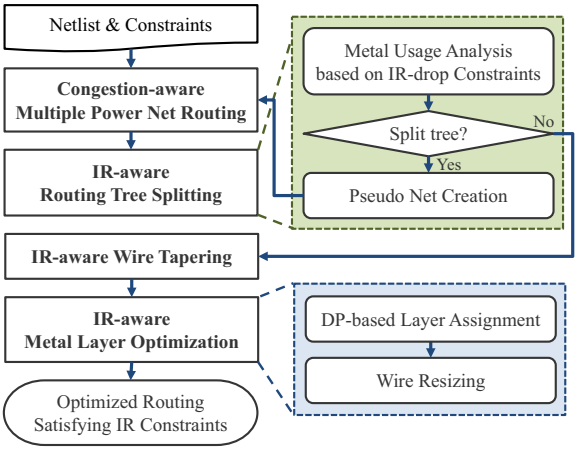


Fig. 2. The proposed IR-aware multiple-power-net routing flow with wire tapering and layer optimization.

Congestion-aware routing adopts a commercial router by inputting an estimated wire width according to the given IR-drop constraints. It produces initial routing while considering routing blockages and congestion. IR-aware routing tree splitting performs metal usage analysis for each net, and then determines whether to split routing subtrees for less overall metal usage. IR-aware wire tapering resizes the width of each wire segment and minimizes total metal area subject to the IR-drop constraints. Finally, IR-aware metal layer optimization further optimizes the metal layer of each wire segment with simultaneous wire resizing based on a dynamic programming algorithm.

A. Congestion-aware Multiple Power Net Routing

Without the consideration of IR-drop constraints, the state-of-the-art commercial routers already handle the general congestion-aware multiple net routing problem very well. In order to obtain appropriate routing path planning for all power nets while considering routing congestion and blockages, we resort to the state-of-the-art commercial routers. When applying commercial routers, the metals existing in the mixed-signal functional blocks are considered as routing blockages.

Instead of applying the minimum wire width during congestion-aware routing, the routing width of each metal layer must be appropriately provided to the commercial routers. If the wire width is too small, we may not have enough space to perform the succeeding wire tapering and wire resizing after congestion-aware routing. On the contrary, if the wire width is too large, the routing path of a power net may become much longer or even unroutable due to severe routing congestion.

Before estimating appropriate wire width for congestion-aware routing, we first determine the lower bound, $w^L_{M_i}$, and upper bound, $w^U_{M_i}$, of the wire width of each metal layer, M_i, by the following equations, where I_{p_k} denotes the current at p_k, l_{p_k} denotes the Manhattan distance from p_k to its voltage source, I_{n_j} denotes the maximum current of n_j, and l_{n_j} represents the half-perimeter wirelength of n_j.

$$w^L_{M_i} = \max_k \left(\rho_{M_i} \times \frac{I_{p_k} \times l_{p_k}}{\Delta V_{p_k}} \right). \tag{2}$$

$$w^U_{M_i} = \max_j \left(\rho_{M_i} \times \frac{I_{n_j} \times l_{n_j}}{\min_{p_k \in n_j} \Delta V_{p_k}} \right). \tag{3}$$

We estimate the wire width according to the available routing space using the corner stitching data structure [14]. We construct the horizontal (vertical) tile plane, as shown in Fig. 3(a) (Fig. 3(b)), to identify horizontal (vertical) routing space. For each space tile, T_j, in the tile plane, we first count the potential number of nets, m_{T_j}, to be routed inside T_j, where m_{T_j} is equal to the total number of nets connecting the adjacent block tiles of T_j. Once m_{T_j} is obtained, the wire width for layer M_i is then estimated by Equation (4), where w_{T_j} is the width (height) of the horizontal (vertical) tile, T_j, and S_{M_i} is the minimum spacing rule between two adjacent parallel wires for M_i.

$$w^{Est}_{M_i} = \min_j \left(\frac{w_{T_j}}{m_{T_j} + 1} - S_{M_i} \right). \tag{4}$$

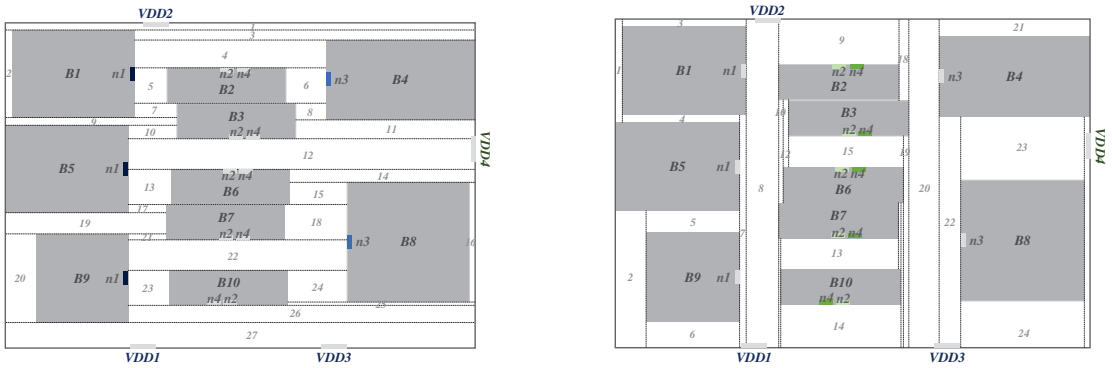


Fig. 3. Routing space identification using the corner stitching data structure. (a) A horizontal tile plane. (b) A vertical tile plane.

Based on $w^L_{M_i}$, $w^U_{M_i}$, and $w^{Est}_{M_i}$ resulting from Equations (2), (3), and (4), the wire width of each metal layer for the congestion-aware router is given by Equation (5). If the estimated wire width, $w^{Est}_{M_i}$, resulting from Equation (4) is out of both lower and upper bounds, we use either low bound, $w^L_{M_i}$, or upper bound, $w^U_{M_i}$, as the estimated wire width.

$$w_{M_i} = \begin{cases} w^U_{M_i}, & \text{if } w^{Est}_{M_i} > w^U_{M_i}; \\ w^{Est}_{M_i}, & \text{if } w^L_{M_i} \leq w^{Est}_{M_i} \leq w^U_{M_i}; \\ w^L_{M_i}, & \text{if } w^{Est}_{M_i} < w^L_{M_i}. \end{cases} \quad (5)$$

B. IR-Aware Routing Tree Splitting

After obtaining the initial routing, we shall analyze the IR-drop effect of each net based on its routing topology, and then thicken some wire segments to satisfy all IR-drop constraints while minimizing total metal usage. We observed that although the routing topologies resulting from initial routing can achieve shorter wirelength, they may consume more routing space after wire tapering in order to satisfy all IR-drop constraints. One way to reduce such large metal usage is applying routing tree splitting. Fig. 4 gives two examples of different routing topologies of a net without and with routing tree splitting.

In Fig. 4(a), although the routing topology without routing tree splitting has the shortest wirelength, it may result in much more metal usage after tapering wire segments from the power source to each pin, as shown in Fig. 4(b), for satisfying all IR-drop constraints. On the contrary, the routing topology in Fig. 4(c) has an additional routing tree from the power source. Each routing tree drives different set of pins. Although the overall wirelength is longer, the resulting metal usage can be greatly reduced after wire tapering, as shown in Fig. 4(d), while all the IR-drop constraints are still satisfied.

We propose an IR-aware routing tree splitting method to minimize overall metal usage of each net based on the original routing topology. Fig. 5 shows a routing instance of a net and the corresponding routing tree, where the tree root denotes the power source, the internal nodes denote steiner points, and the leaves denote all sinks. The proposed method consists of three steps: 1) metal usage estimation, 2) pin cost calculation, and 3) routing tree splitting subject to metal usage minimization.

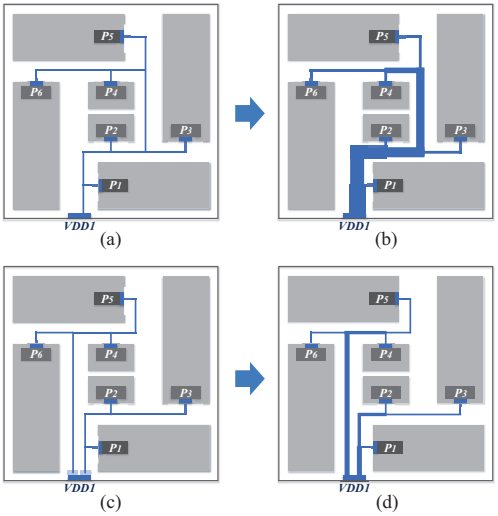
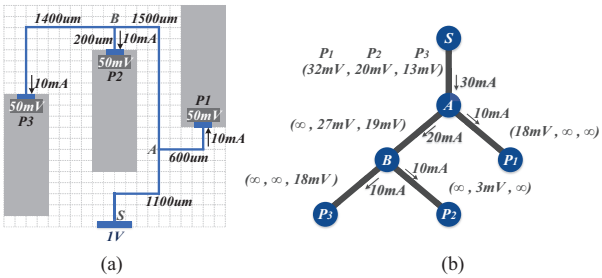


Fig. 4. IR-aware routing tree splitting. (a)(b) A routing topology without routing tree splitting resulting in much more metal usage in order to satisfy all IR-drop constraints. (c)(d) An alternative routing topology with routing tree splitting resulting in much less metal usage while all IR-drop constraints are still satisfied.

1) Metal Usage Estimation: Before determining whether to split the routing tree, we shall estimate the minimal metal usage of the routing tree with the satisfaction of the specified IR-drop constraint at each pin. The estimated total metal usage of a routing tree, $\tilde{\Phi}$, can be computed by Equation (6), where ρ_e, I_e, l_e, and ΔV_e denote the sheet resistance, current value, wirelength, and IR drop of a tree edge, e, respectively. ρ_e and I_e are given from the problem input. l_e is known from the initial routing topology. ΔV_e is calculated according to the IR drop constraint of each pin and the prorated wirelength from the source to the pin. In Fig. 5(b), the routing tree edges have a tuple of three different values of IR drop. Each value corresponds to the prorated IR drop from the power source to each pin. For example, there are two tree edges from S to p_1, and the IR-drop constraint at p_1 is $50mV$. The wirelength of each tree edge is $1100\mu m$ and $600\mu m$, respectively, as



(a) (b)

Fig. 5. Metal usage estimation. (a) The initial routing topology of a power net. (b) The corresponding routing tree.

shown in Fig. 5(a), and hence the prorated IR drop of each tree edge will become $32mV$ and $18mV$ respectively. Similarly, we can obtain the prorated IR drops corresponding to the IR-drop constraints from S to all the other pins. For each tree edge, we choose the minimum prorated IR drop among all to estimate total metal usage based on Equation (6).

$$\tilde{\Phi} = \sum_{e} \frac{\rho_e \times I_e \times l_e^2}{\Delta V_e}. \tag{6}$$

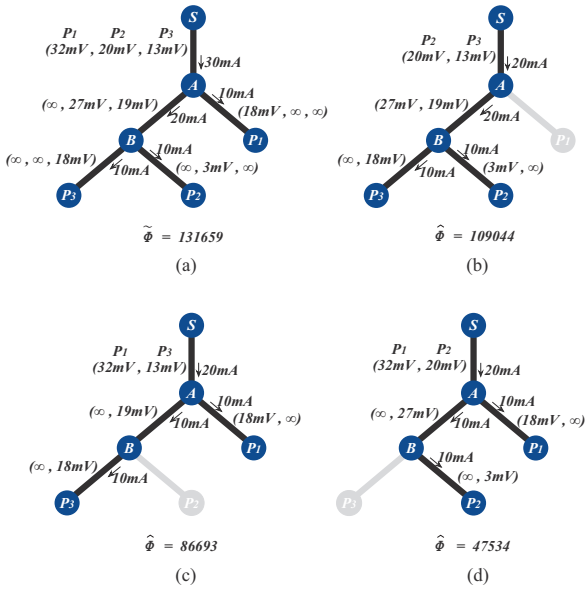


Fig. 6. The estimated metal usages for (a) the original routing tree, (b) the routing tree without p_1, (c) the routing tree without p_2, and (d) the routing tree without p_3.

2) Pin Cost Calculation: Based on the metal usage estimation, we calculate the cost of each pin according to the metal usage from its power source to the pin in the routing tree. To achieve this, we remove one pin from the routing tree at a time, and recalculate total metal usage of the new routing tree after the pin removal. Fig. 6 shows the estimated metal usage for the original routing tree, denoted by $\tilde{\Phi}$, as well as the estimated metal usages for the routing trees after removing p_1, p_2, and p_3, respectively, denoted by $\hat{\Phi}$. The difference between $\tilde{\Phi}$ and $\hat{\Phi}$ indicates the metal consumption of the removed pin.

3) Routing Tree Splitting for Metal Usage Minimization: According to the calculated pin costs of all pins, the pin having the largest difference between $\tilde{\Phi}$ and $\hat{\Phi}$ means that it has the largest amount of metal consumption in the routing tree. We observed that if we split the routing tree by reconnecting the pin to the power source, the amount of metal usage of the whole routing tree can be further reduced. When splitting the original routing tree, we shall create a pseudo net for each sub-tree driving different set of pins from the respective power source, and then the congestion-aware multiple power net routing is performed again. The process of routing tree splitting continues until the total metal total usage cannot be further reduced.

C. IR-aware Wire Tapering

Given the initial routing of each net and pseudo net, the IR-aware wire tapering optimizes the width of each wire segment such that total metal usage is minimized while all IR-drop constraints are satisfied. We propose a nonlinear programing (NLP) formulation to solve the IR-aware wire tapering problem using the NLP solver [15]. The objective of the NLP formulation is to minimize the actual metal usage of all wire segments of a net, as shown in Equation (7), where l_i is a known constant denoting the length of a wire segment, and w_i is an unknown variable denoting the corresponding wire width.

$$\min \sum_{i} l_i \times w_i. \tag{7}$$

$$st. \quad \sum_{e \in p_k \to S} \frac{\rho_e \times I_e \times l_e}{w_e} + V_{via} \leq \Delta V_{p_k}, \quad \forall \text{ pin } k$$
$$w_{min} \leq w_e \leq w_{max}, \quad \forall \text{ edge } e \tag{8}$$

$$\Delta V_i = \frac{\rho_i \times I_i \times l_i}{w_i}. \tag{9}$$

The NLP formulation further includes a set of IR-drop constraints and a set of minimum/maximum wire width constraints, as shown in Equation (8), where V_{via} denotes the voltage drop of each via, which is given from the technology file. For IR-drop constraints, the actual IR drop of each wire segment can be calculated by Equation (9). The IR-drop of the path from the source to each pin can be calculated by summing up the IR drop of each wire segment and vias along the path. It must be less than or equal to the given IR-drop constraint of the pin, ΔV_{p_k}. For minimum/maximum wire width constraints, the width of each wire segment, w_e, must be within the range of minimum and maximum widths, w_{min} and w_{max}, according to design rules and routing blockages. Fig. 7 gives an example of IR-aware wire tapering solved by the presented NLP formulation.

D. IR-aware Metal Layer Optimization

The metal layer of each wire segment was initially determined by congestion-aware routing, which follows a preferred direction of the corresponding metal layer. As different metal layers have different sheet resistances, performing IR-aware layer optimization can help reduce total metal usage and via numbers. We propose a dynamic programming (DP) formulation to optimize the metal layers of all wire segments for

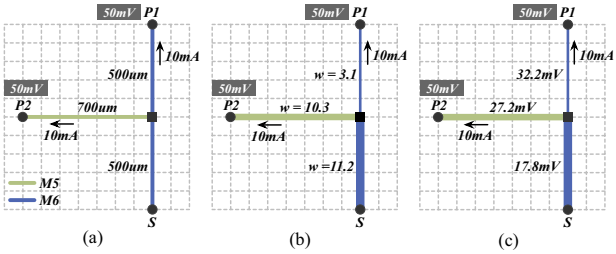


Fig. 7. IR-aware wire tapering. (a) The initial routing without wire tapering. (b) The width of each wire segment solved by the NLP formulation. (c) The IR drop of each wire segment resulting from (b), which satisfies all IR-drop constraints on different pins.

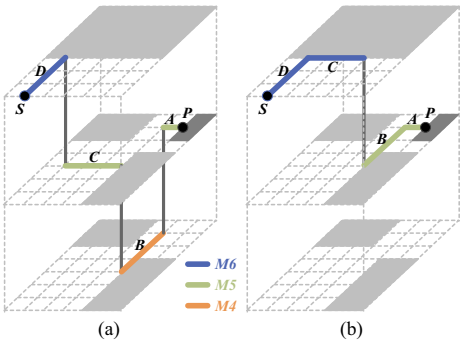


Fig. 8. (a) The routing of a net before metal layer optimization. (b) The routing after applying IR-aware metal layer optimization based on the DP algorithm illustrated in Fig. 9.

each net, as demonstrated in Figs. 8 and 9, by minimizing the resistance of all wires in a net. It also allows non-preferred directions depending on designers' preference. Once the metal layers of all wires are optimized with minimum resistance, we may further reduce wire width and metal usage based on the aforementioned NLP formulation.

In Fig. 8, there are four wire segments in a net denoted by A, B, C, and D, respectively. Assuming that the width of each wire segment is given from the previous step, Fig. 9 shows the process of calculating the total resistance cost of a net based on the DP algorithm, where the vertices, A_i, B_i, C_i, and D_i, denote the wire segment, A, B, C, and D, in Fig. 8 on the different metal layers, M_i. An edge exists between two vertices if their corresponding wire segments are connected. The edge cost indicates the resistance of the connected wire segment on the specified metal layer. The via resistance is also counted if the connected wire segment is on a different metal layer. The infinity cost, ∞, indicates that the connected wire segment cannot be routed on the corresponding metal layer due to some routing blockages. The DP algorithm first calculates the cost from a pin to its source, and then perform backtracking based on the minimum cost. After backtracking, the optimal metal layer assignment for all wire segments of a net is obtained. Fig. 8(b) shows the resulting metal layer assignment after performing the DP algorithm for the routing instance in Fig. 8(a).

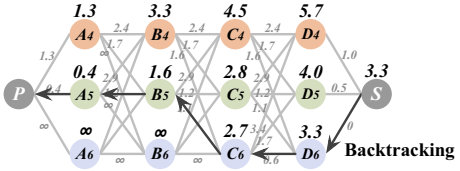


Fig. 9. The proposed DP algorithm for IR-aware metal layer optimization.

TABLE II
STATISTICS OF MULTI-VOLTAGE MIXED-SIGNAL CIRCUITS.

Name	# power nets	# pins	max pin # per net	# obstacles
Case1	3	4	2	3
Case2	1	20	20	13
Case3	6	21	6	15
Case4	4	28	9	19
Case5	4	35	10	22
Case6	8	49	9	30
Case7	7	52	10	37

IV. EXPERIMENTAL RESULTS

We implemented the proposed IR-aware multiple power net routing with wire tapering and layer optimization in the C++ programming language, and performed on a machine with Intel Xeon E5-2620 @ 2.0GHz. The congestion-aware routing and the NLP solver are based on the third-party tools, Cadence SoC Encounter and Ipopt [15], respectively. To evaluate the IR-drop at each pin resulting from our method, we further extracted routing parasitics and performed IR-drop simulation with NGSPICE [16]. We tested our algorithms on seven multi-voltage mixed-signal SoC designs with different numbers of power nets, pins, and obstacles, as shown in Table II.

In order to show the effectiveness of each step in our proposed approach, as seen in Fig. 2, we compare four different configurations, as listed in Table III, where "Congestion-aware Multiple Power Net Routing" is performed by all the configurations; "IR-aware Wire Tapering" is performed by Configurations (2), (3), and (4); "IR-aware Metal Layer Optimization" is performed by Configurations (3) and (4); "IR-aware Routing Tree Splitting" is performed by Configuration (4) only.

Table IV shows the total metal usage and the numbers of satisfied IR-drop constraints resulting from our method based on the four configurations. According to the experimental results in Table IV, Configuration (4) results in the least total metal usage of all power nets. Without routing tree splitting, Configuration (3) has 24% more metal usage than Configuration (4). Configuration (1) and (2) cannot satisfy

TABLE III
FOUR DIFFERENT CONFIGURATIONS FOR EXPERIMENTAL COMPARISON.

Configurations	(1)	(2)	(3)	(4)
Congestion-aware Multiple Power Net Routing	√	√	√	√
IR-aware Wire Tapering		√	√	√
IR-aware Metal Layer Optimization			√	√
IR-aware Routing Tree Splitting				√

TABLE IV
COMPARISONS OF THE TOTAL METAL USAGE AND NUMBERS OF SATISFIED IR-DROP CONSTRAINTS FOR OUR METHOD BASED ON THE FOUR DIFFERENT CONFIGURATIONS GIVEN IN TABLE III.

Name	Configuration (1)		Configuration (2)		Configuration (3)		Configuration (4)	
	Metal Usage (um^2)	# IR Constraints Satisfied	Metal Usage (um^2)	# IR Constraints Satisfied	Metal Usage (um^2)	# IR Constraints Satisfied	Metal Usage (um^2)	# IR Constraints Satisfied
Case1	234490	4	158521	4	60614	4	60614	4
Case2	3728380	12	705493	5	139223	20	79770	20
Case3	1441930	12	986346	12	460489	21	391170	21
Case4	2665020	24	683646	24	304997	28	157679	28
Case5	3224060	34	1101750	34	456523	35	239145	35
Case6	5164040	47	1271620	41	489403	49	474358	49
Case7	4568610	30	2085240	40	754791	52	754791	52
Avg	9.75	0.79	3.24	0.75	1.24	1	1	1

TABLE V
COMPARISONS OF THE TOTAL WIRELENGTH, AVERAGE SOURCE-TO-SINK WIRELENGTH, AND RUNTIME FOR OUR METHOD BASED ON CONFIGURATIONS (3) AND (4).

Case	Total wirelength (um)		Avg. source-to-sink wirelength (um)		Runtime (s)			
	Configuration (3)	Configuration (4)	Configuration (3)	Configuration (4)	Configuration (3)		Configuration (4)	
					SoC Encounter	Others	SoC Encounter	Others
Case1	7274	7274	1899	1899	1	<0.01	1	<0.01
Case2	10918	17560	3723	3119	26	0.10	140	0.88
Case3	22161	26098	2342	2270	3	0.18	8	0.22
Case4	27514	31768	2638	2269	29	0.60	58	0.41
Case5	23897	32801	2875	2428	56	0.71	244	0.75
Case6	54634	63639	2858	2748	109	2.69	371	2.16
Case7	52663	52663	2809	2809	66	2.21	166	2.21
Avg	1	1.16	1	0.92	41.43	0.93	141.14	0.95

all the IR-drop constraints because routing with a preferred direction of each metal layer will result in more layer changes and more vias. Therefore, the total wire resistance will be increased. With layer optimization, Configurations (3) and (4) can easily satisfy all the IR-drop constraints. Consequently, the proposed method with all steps included is very effective in reducing total metal usage of all power nets while satisfying IR-drop constraints.

Table V further compares the total wirelength, average source-to-sink wirelength, and runtime for our method based on Configurations (3) and (4). Although the total wirelength resulting from Configuration (4) is 16% longer than that resulting from Configuration (3), the average source-to-sink wirelength resulting from Configuration (4) is 8% shorter. It should be noted that the total wirelength is not the most important metric for power net routing, but the total metal usage is. The runtime of Configuration (4) is longer because rerouting is required after routing tree splitting.

V. CONCLUSIONS

The IR-drop effect has become one of the most important issues, especially in multi-voltage mixed-signal design. In this paper, we have introduced the multiple power net routing problem with the consideration of IR drop and metal usage in mixed-signal design. We have also proposed a holistic solution to the problem, including routing tree splitting, wire tapering, and metal layer optimization. Our experimental results have shown that the proposed method can effectively reduce total metal usage and satisfy all IR-drop constraints.

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