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A 5 Giga Samples Per Second 8-Bit Analog to Digital Printed Circuit Board for Radio Astronomy

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ABSTRACT. We have designed, manufactured, and characterized an 8-bit 5 Giga samples per second (Gsp/s) ADC printed circuit board assembly (PCBA). An e2v EV8AQ160 ADC chip was used in the design and the board is plug compatible with the field programmable gate array (FPGA) board developed by the Collaboration for Astronomy Signal Processing and Electronics Research (CASPER) community. Astronomical interference fringes were demonstrated across a single baseline pair of antennas using two ADC boards on the Yuan Tseh Lee Array for Microwave Background Anisotropy (AMiBA) telescope. Several radio interferometers are using this board for bandwidth expansion, such as Submillimeter Array; also, several experimental telescopes are building new spectrometers using the same board. The ADC boards were attached directly to the Reconfigurable Open Architecture Computing Hardware (ROACH-2) FPGA board for processing of the digital output signals. This ADC board provides the capability of digitizing radio frequency signals from DC to 2 GHz (3 dB bandwidth), and to an extended bandwidth of 2.5 GHz (5 dB) with derated performance. The following worst-case performance parameters were obtained over 2 GHz: spur free dynamic range (SFDR) of 44 dB, signal-to-noise and distortion (SINAD) of 35 dB, and effective number of bits (ENOB) of 5.5.

Online material: color figures

1. INTRODUCTION

Digital signal processing (DSP) is an essential technology of modern radio astronomy telescopes. The design of the digital instrumentation is highly specialized and its development typically consumes a large amount of resources in terms of labor, time, and budget. In the past decade or so, there has been a trend toward promoting shared hardware development that includes items such as interchangeable digitizers, flexible digital hardware processors, reusable DSP libraries, scalable instrument architectures, and flexible monitor and control and interfaces. Such development benefits the radio astronomy community, especially for those institutes that only support a small group of digital developers. The Collaboration for Astronomy Signal Processing and Electronics Research (CASPER) is one of the major promoters of this effort and has expanded to include several astronomical and engineering institutions around the world. Our contribution to this consortium has been the development of a high-speed analog to digital converter (ADC) board, shown in Figure 1, to be used in conjunction with other hardware available from the CASPER suite.

AMiBA (Array for Microwave Background Anisotropy; Ho et al. 2009) is a radio interferometry telescope dedicated to cosmology experiments. Located at 3,400-meters elevation on the northern slope of Mauna Loa, Hawaii, the telescope consists of thirteen 1.2-meter dishes mounted to a single 6-meter diameter

steerable platform. Each of the thirteen antennas feed a separate dual-polarization receiver and provides wideband sky coverage from 86–102 GHz. The sky signal is down converted to an intermediate frequency (IF) of 2–18 GHz. The current backend hardware consists of an analog 4-lag correlator (Li et al. 2010) that processes the entire 16 GHz IF signal bandwidth and has been in operation since 2006. This analog correlator was designed specifically for continuum detection and does not have the capability to perform spectroscopy.

A new digital correlator is currently under development to provide AMiBA with the capability to perform spectroscopy in addition to the existing continuum science. This new correlator will be based on the CASPER ROACH-2 (Reconfigurable Open Architecture Computing Hardware; Parsons et al. 2006, 2008) board and its associated gate-ware library. The open source library includes functions such as poly-phase filter bank (PFB), fast Fourier transform (FFT), fringe stopping, delay tuning, vector accumulator, and cross correlation, all of which can be linked together to form a complex correlator instrument. The commonly used functional blocks are parameterized to allow custom tailoring for a wide variety of applications.

1.1. Digitation of Large Signal Bandwidths

The ability of interferometers to capture and correlate large frequency bandwidths provides the advantages of increased

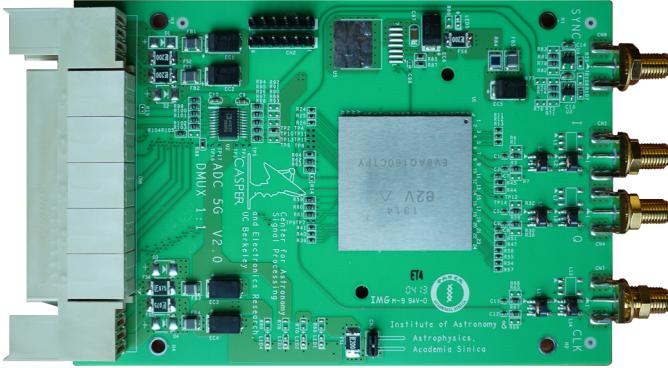


FIG. 1.—The 8-bit, 5 Gps ADC board. SMA input connectors for 1 pulse per second (1 pps) synchronization signal, I-channel, Q-channel, and clock are shown on the right side of the board (*top to bottom*). The e2v EV8AQ160 device is located under the heat sink and the LVDS digitized data outputs are via the white Z-DOK connector. See the electronic edition of the *PASP* for a color version of this figure.

continuum sensitivity and the inclusion of more spectral lines within the observing band. Capturing wide input bandwidth signals can be accomplished with the use of several moderate bandwidth ADCs such as the CASPER iADC, or with fewer

wide band ADCs such as the one described by in this paper. Figures 2 and 3 illustrate the down converter architectures and frequency plan for two 2 Giga sample per second (Gsp) ADCs versus a single 5 Gsp ADC, respectively. Both approaches are targeted to capture 2 GHz of analog input bandwidth for the AMiBA system. In the two ADC approach, two band pass filters (BPFs) are required for frequency separation prior to down conversion using separate mixers and local oscillators (LOs). The 2.75–3.65 GHz band utilizes a high side LO of 3.1825 GHz to prevent leakage into the desired 2.75–3.65 GHz band and results in spectral inversion that is corrected in digital processing. An overlap of 156 MHz (Fig. 3) (*upper left*) is provided between the two bands to ensure undistorted data across the filter band edges. Due to the losses of the overlap and band edges, the effective digitized bandwidth is 1.65 GHz. The 5 Gsp ADC is operated at 4.48 Gsp to accommodate a data rate restriction within the ROACH-2. This approach requires only a single BPF, mixer, and LO, and can capture the entire 2.0 GHz analog input bandwidth including the effects of band edge losses. Additional frequency coverage, e.g., 4–8 GHz and 8–10 GHz, can be provided by extending the methods described above. In general, for a given bandwidth to be digitized, the complexity

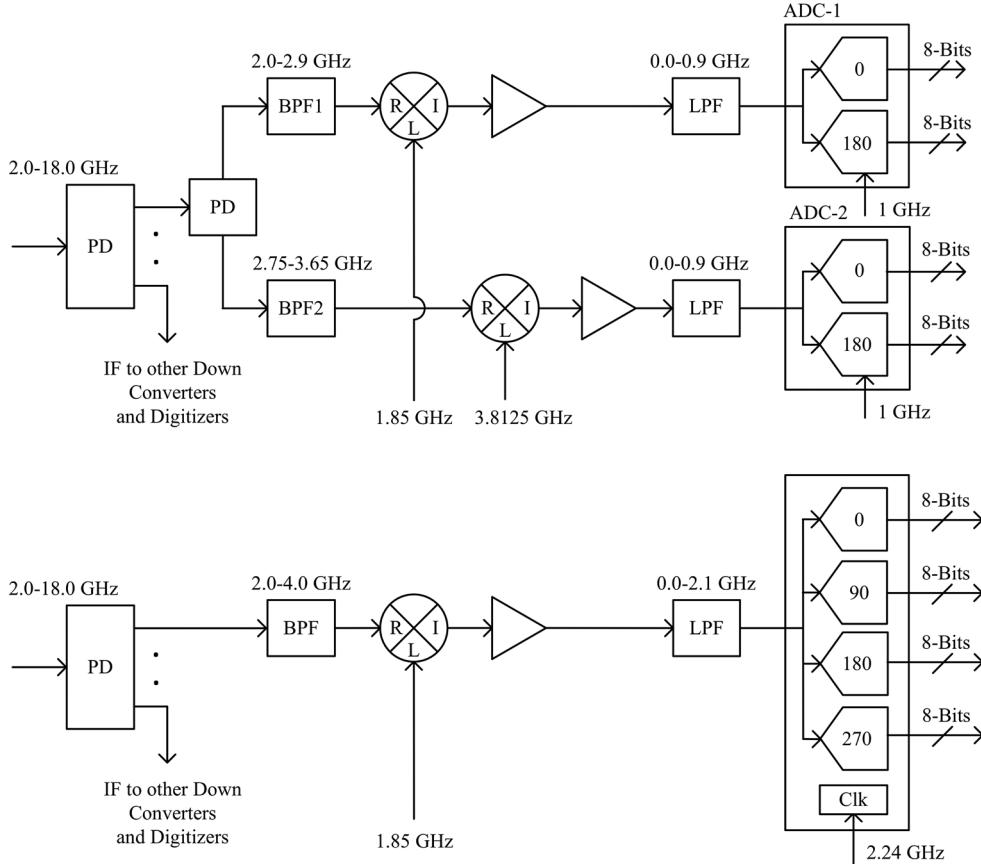


FIG. 2.—Downconverter design comparisons for ADCs of different sample rates. The upper and lower diagrams represent the downconverter architectures for two 2 Gps ADCs and one 5 Gps ADC, respectively. The 2 Gps ADC (*top*) consists of two 8-bit cores each sampled at 1 Gps (maximum). The 5 Gps ADC (*bottom*) consists of four interleaved cores each sampled at 1.12 Gps and results in an overall 4.48 Gps. PD stands for power divider and LPF stands for low pass filter.

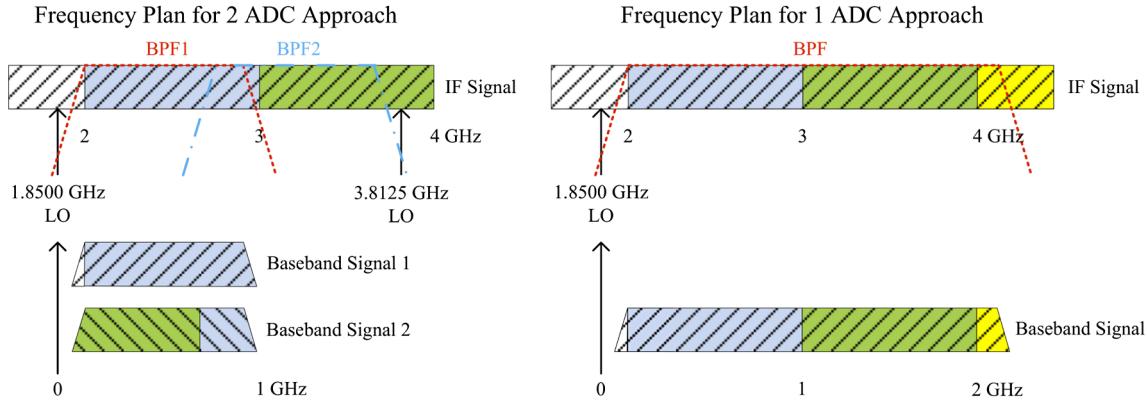


FIG. 3.—Frequency plan comparison for capturing 2 GHz analog bandwidth using two ADC vs. a single ADC. The two ADC approach requires two BPFs with a small amount of overlap to prevent distortion at the band edges. The post filtered analog data is down converted to baseband using the two specified LOs. The single ADC approach requires only one BPF and avoids the overlap. See the electronic edition of the *PASP* for a color version of this figure.

and cost of the IF system reduces by approximately 2.4 times the ratio of the ADC sample rates.

2. DEVICE SELECTION AND HARDWARE DESIGN

When this effort began in 2010, there was only a small selection of fast ADC devices and boards available on the market. Micram had announced a 30 Gsps device (Ellermeyer et al. 2010); however, it was still in the development. Both Acqiris (Petriska et al. 2009) and Tektronix had commercial 8-bit ADC boards operating above 5 Gsps available but were deemed too costly. During that timeframe, e2v had released a 5 Gsps 8/10-bit ADC device. This device was quickly incorporated into an FPGA based FFT spectrometer (Klein et al. 2009, 2012). Our final decision was to design a printed circuit board assembly (PCBA) around a similar e2v device, EV8AQ160 (Klein et al. 2008; Glascott-Jones et al. 2011), which provided 8-bits resolution at 5 Gsps. This PCBA was designed to interface directly with the existing suite of CASPER hardware.

The EV8AQ160 device utilizes four 8-bit cores and can be configured to operate in a variety of modes that include digitization of four input channels, two input channels, or a single input channel. The design of this PCBA permits the end user to select between two input channel and single input channel modes. A maximum sample rate of 5 Gsps is obtained with an input clock frequency of 2.5 GHz that is internally divided down by two to produce the four sampling clocks at a rate of 1.25 Gsps. In the two-channel mode, each of the two inputs are fed to a pair of interleaved ADCs that are clocked 180° out-of-phase resulting in two samples per clock cycle. The single channel input mode provides the same input signal to all four cores that are clocked at 0, 180, 90, and 270°, resulting in four samples per clock cycle (Fig. 4).

The interleaving of multiple ADC cores inevitably introduces misalignments in timing, gain, and offset due to manufacturing variations between the individual cores (Klein et al. 2012). These misalignments result in an overall degraded performance

in addition to producing undesired spurs in the output spectrum. To minimize these undesirable effects, this e2v device provides adjustment of the core parameters and will be discussed further in § 3.

As is common with many high speed ADCs, the e2v device has differential analog signal and clock inputs. The schematic shown in Figure 5 represents the input circuit where a single-ended 50 Ohm input signal drives 1:1 transformers, L2 and L3 (visible in Fig. 1), to produce a pair of signals that are 180° with respect to each other. Capacitors, C1 and C2, are DC blocks with a low end roll-off (-3 dB) of approximately 32 kHz. Note that components L1, R6, and R7 are not populated on the board. The outer two layers of this 4-layer board are composed of Rogers 4003 material to support microwave frequency signals. This entire input circuitry (Fig. 6) has been characterized to produce a loss of 1 dB at 500 MHz, 3 dB at 2 GHz, and 5 dB at 2.5 GHz.

The primary interface for digital inputs, outputs, and power for this ADC board is via a Z-DOK connector (Tyco 2003) visible in Figure 1. This connector provides 40-pairs of controlled impedance transmission lines (100-Ohms line-to-line), each pair consisting of signal⁺, signal⁻, and ground. When operated in 1:1 demux mode, the e2v ADC device outputs 32-pairs (8-bits/core, four cores) of low voltage differential signaling (LVDS) that are routed directly to the Z-DOK connector without re-clocking or buffering. The remaining 8-pairs of the connector are used for clock, sync, telemetry, and control signals. Twenty-four additional nonimpedance controlled utility connections are provided by the Z-DOK for DC power (+5, +3.3, +2.5, and +1.8 VDC). The single channel input mode provides a maximum data rate of 1.25 Gbps and is well within the maximum specified rate of 6.2 Gbps for the Z-DOK connector. An optional 1:2 demux mode offered by the ADC device requires 64-pairs but cannot be used due to the 40-pair limitation of the connector. Though the design of this ADC board has been specifically targeted to interface directly to the CASPER ROACH-2 board as shown in Figure 7, it can be used with

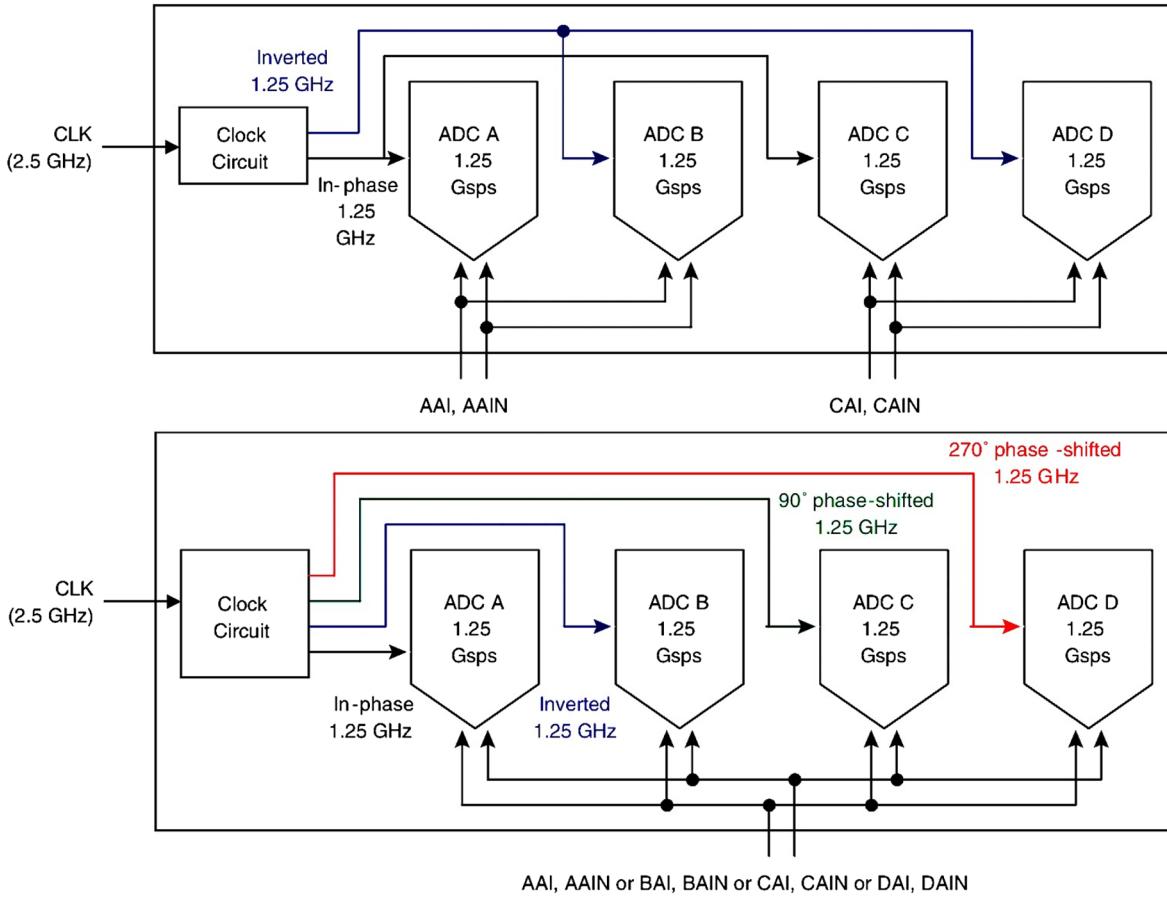


FIG. 4.—Internal ADC configurations. The top and bottom figures illustrate the configurations for two input channel mode and single input channel mode, respectively. See the electronic edition of the *PASP* for a color version of this figure.

other platforms as long as the user conforms to the Z-DOK pin assignments defined by CASPER.

3. CALIBRATION AND PERFORMANCE

The test setup used for calibration and characterization is illustrated in Figure 8. The input to the ADC under test was

stimulated with a variable frequency continuous wave (CW) tone at a level of -6 dBm ($317 \text{ mV}_{\text{pp}}$), 4 dB below the device's $V_{\text{full-scale}}$ specification of -2 dBm ($500 \text{ mV}_{\text{pp}}$). To prevent artifacts of quantization noise and differential nonlinearity (DNL) from affecting the test data, -36 dBm of noise ($10 \text{ mV}_{\text{pp}}$) was added to the CW signal (Dallet et al. 1998; Kester 2007). The

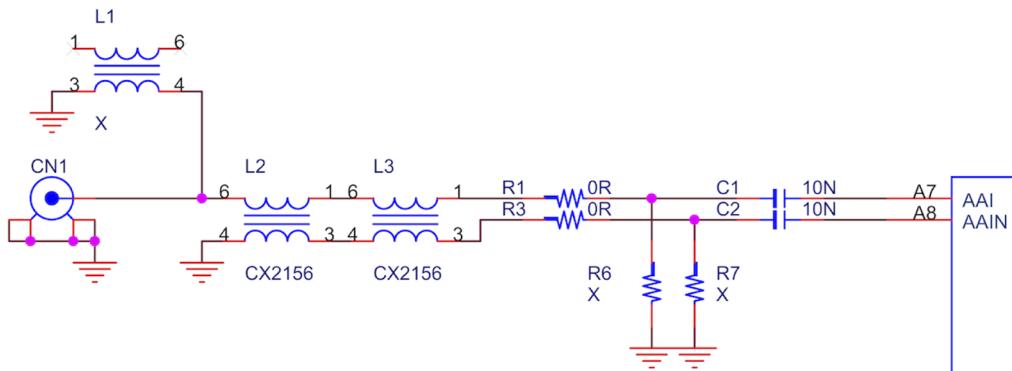


FIG. 5.—Analog input circuitry. Baluns, L2 and L3, are used to convert the single-ended input signal provided at connector CN1 to differential at pins A7 and A8. See the electronic edition of the *PASP* for a color version of this figure.

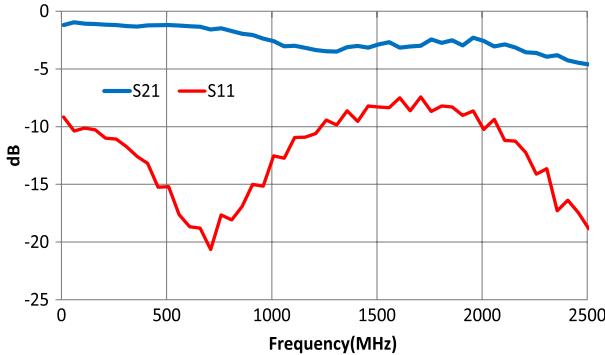


FIG. 6.—RF response of input circuitry. See the electronic edition of the *PASP* for a color version of this figure.

ADC board was connected to a ROACH-2 to provide DC power and control and status to the ADC, and in addition, captured the ADC output data for post processing. The ROACH-2 board consists of a Virtex-6 SX475T FPGA along with a PowerPC 440EPx standalone processor and provides eight 10 gigabit Ethernet (GbE) interfaces. For testing purposes, the ROACH-2 is programmed using a simple model file to capture and save the digitized data from the ADC into block random access memory (BRAM) located on the board. A Python program running on an external PC is used to transfer the data from the BRAM to the external PC for offline spectral analysis.

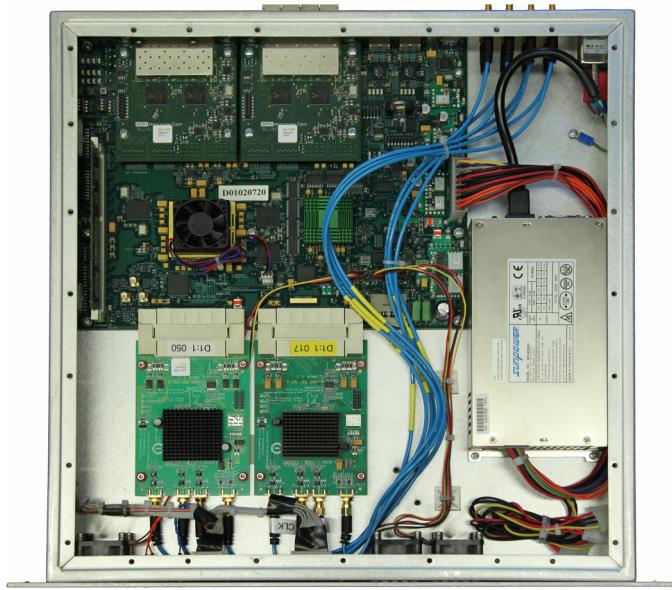


FIG. 7.—ROACH-2 chassis. Two ADC boards interface directly to the ROACH-2 board via Z-DOK connectors. The entire package is self-contained within a 1U high rack mount chassis. Analog, clock, and sync inputs are provided to the ADC via front panel mounted SMA connectors. The post-processed digital output signals are provided via four rear panel mounted small form-factor pluggable + (SFP+) 10 Gigabit Ethernet connectors. See the electronic edition of the *PASP* for a color version of this figure.

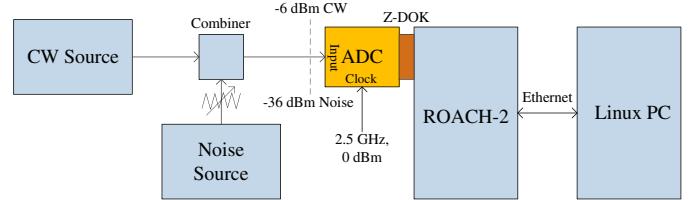


FIG. 8.—Calibration and test setup for ADC. A CW source is used to stimulate to the ADC under test. A small amount of noise is added to the CW signal to reduce the effects of quantization noise and DNL. A ROACH-2 and Linux PC are used to capture and process the digitized data from the ADC. See the electronic edition of the *PASP* for a color version of this figure.

The 5 Gsps ADC chip, when operated in the single channel input mode (Fig. 4), is composed of four interleaved cores running at 1.25 Gsps. DC offset, gain, and phase tuning registers are embedded into each of the four cores and are accessible via serial peripheral interface (SPI) bus. We created an automatic tuning program that adjusted offset first to achieve zero DC offsets for the four digital core outputs. Next, the program gradually tuned the gains and compared the read back amplitudes from the four individual ADC cores. Once the four cores achieved matched amplitudes, the program terminated the adjustments and saved the gain and offset parameters. For this round of tests, we did not attempt to adjust the phase of the four cores. We compared two different tuning methods, the first using a single frequency input test tone, and the second using fifteen different input frequency tones across the 0 to 2.5 GHz band, then averaged the resultant gain and offset parameters. For single frequency tuning, we selected 1400.0977 MHz to correspond to the center of an FFT bin. For the multi-frequency tuning, we selected the fifteen separate frequencies to correspond to the center of fifteen different FFT bins.

The spur free dynamic range (SFDR) for the ADC board was characterized by inputting a single frequency tone at 4 dB below full-scale (-4 dBfs) into the ADC and measuring the ratio of the desired tone to maximum undesired spur at the FFT output (IEEE 2000). This test was performed for 23 discrete frequency tones, and was repeated for the three different calibration conditions. The results are plotted in Figure 9. Note the significant improvement in SFDR after ADC calibration, and the nearly equal results between the two calibration methods. The SFDR specification for the e2v device is 48/56 dB minimum/typical for a 620 MHz input signal driven at -1 dBfs. Our result at the same frequency but 3 dB lower drive is 45 dB, which, ignoring the loss of the balun, corresponds to an SFDR of 48 dB at a drive level of -1 dBfs.

Signal-to-noise and distortion (SINAD) is defined as the ratio of the rms signal amplitude to the root sum square of the noise and all other spectral components, including spurs and harmonics (IEEE 2000). The results are plotted in Figure 10. Note the improvement of approximately 4 dB after ADC calibration, and the nearly equal results between the two

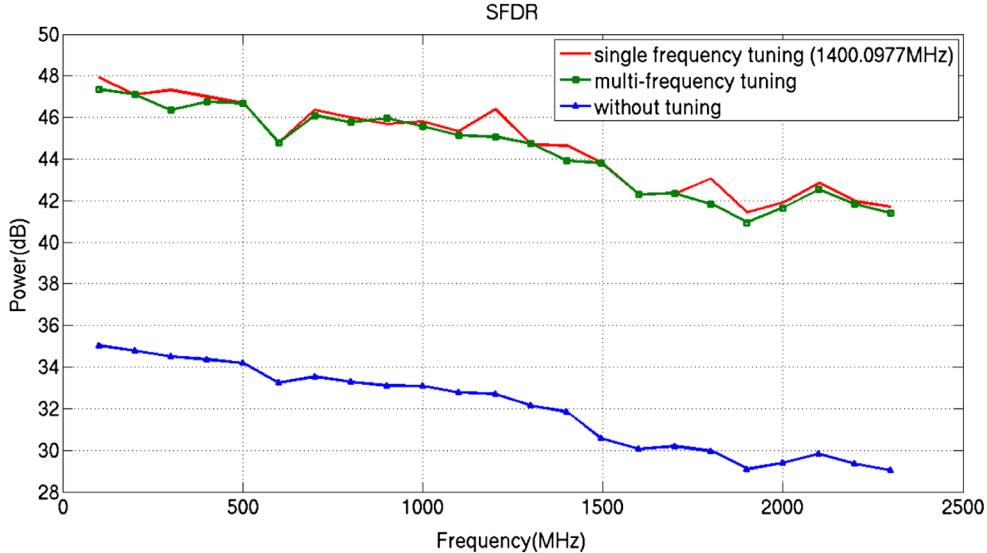


FIG. 9.—SFDR performance at -4 dBfs drive. The green and red lines represent the SFDR performance obtained after calibration using two different methods. The lower blue line represents the SFDR prior to calibration. See the electronic edition of the *PASP* for a color version of this figure.

calibration methods. The SINAD specification for the e2v device is 38.7/40.5 dB minimum/typical for a 620 MHz input signal driven at -1 dBfs. Our result at the same frequency but 3 dB lower drive is 36 dB, which, ignoring the loss of the balun, corresponds to a SINAD of 39 dB at a drive level of -1 dBfs.

SINAD is often converted to effective number of bits (ENOB) using equation (1) below:

$$\text{ENOB} = (\text{SINAD} - 1.76 \text{ dB}) / 6.02 \text{ dB} \quad (1)$$

The ENOB specification for the e2v device is 6.8/7.1 bits minimum/typical for a 620 MHz input signal defined at a drive level of -1 dBfs. Since our SINAD measurements were conducted at a drive level of -4 dBm, we added 3 dB to the numerator in equation (1) to represent ENOB at an equivalent drive of -1 dBm. The results are shown in Figure 11. Note the improvement of approximately 1.5-bits after ADC calibration, and the nearly equal results between the two calibration methods. Our ENOB result at 620 MHz is approximately 6.2-bits.

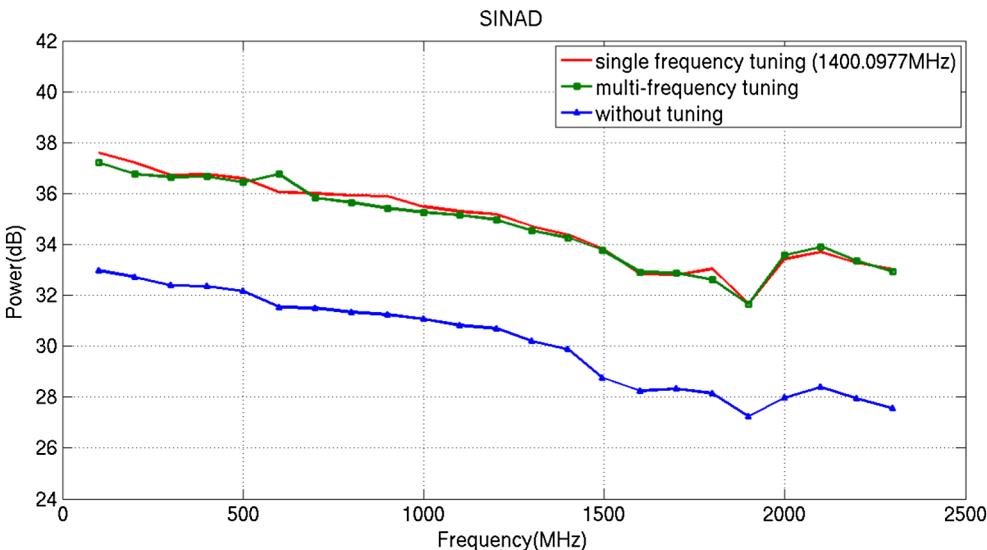


FIG. 10.—SINAD performance at -4 dBfs drive. The green and red lines represent the SINAD performance obtained after calibration using two different methods. The lower blue line represents the SINAD prior to calibration. See the electronic edition of the *PASP* for a color version of this figure.

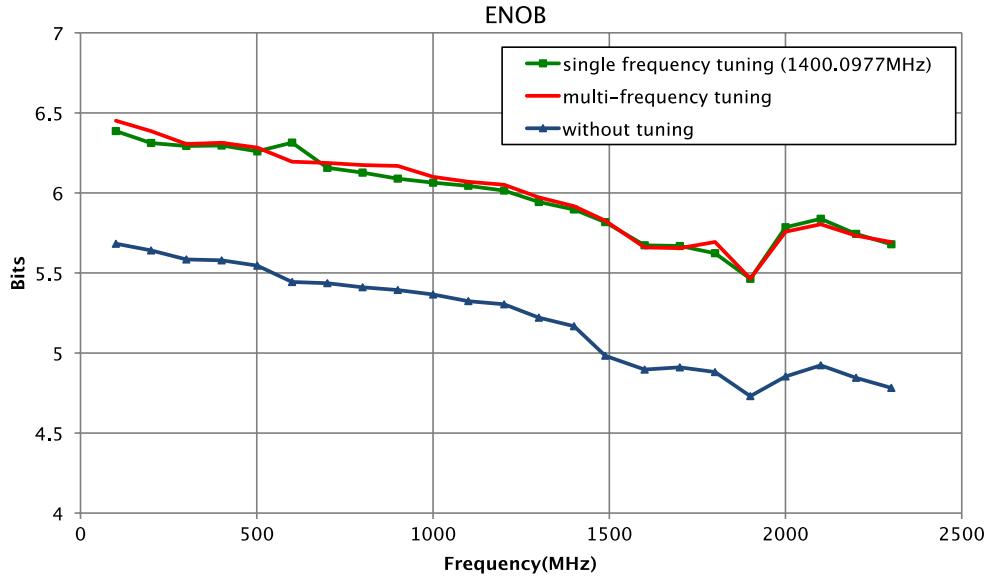


FIG. 11.—ENOB performance at -1 dBfs drive. The green and red lines represent the ENOB performance obtained after calibration using two different methods. The lower blue line represents the ENOB prior to calibration. See the electronic edition of the *PASP* for a color version of this figure.

3.1 Optimal Input Noise Power

This ADC board is intended for use in astronomical applications where the input signal consists largely of Gaussian noise. A question arises as to what the optimum input signal drive level is relative to $V_{\text{full-scale}}$ of the ADC device. Under driving the ADC results in a lower SINAD and ENOB, whereas over driving will lead to clipping and generate undesired harmonics.

The traditional method for determining the optimal input drive is by performing a noise power ratio (NPR) test. This test consists of using a broadband noise source with a notch filter to remove a portion of the noise prior inputting into the ADC under test. An FFT is performed on the digitized ADC output, and the NPR, the ratio of the desired noise to the undesired residual noise in the notched portion of the spectrum, is characterized at different input power levels. The optimum drive occurs when the NPR is at a maximum. For an ideal 8-bit ADC, the maximum NPR is 40.6 dB and occurs at an input drive of -11.87 dBfs (IEEE 2000).

We chose to generate our Gaussian noise in MATLAB, including a notch filter in the center of the band, and created a data set representing this noise. This data set was ported to a Tektronix 7102 arbitrary waveform generator (AWG) that produced the desired analog baseband signal using its internal digital-to-analog converter (DAC). The output power of the AWG was varied to perform the NPR test with the results shown in Figure 12. Note the theoretical NPR value of 40.6 dB occurring at -13.87 dBm, whereas our empirical results produced an NPR of 26 dB at -12.5 dBm. The 14.6 dB difference in NPR values corresponds to a loss of approximately 2.7-bits producing an effective ENOB of 5.3 dB over a 100 MHz to 2300 MHz.

4. DETECTION OF ORION KL

A one-baseline prototype correlator consisting of two ADC boards and a ROACH-2 board (Fig. 7) was deployed on the AMiBA telescope at the end of 2012. The objective of this test was to demonstrate the feasibility of this digital correlator approach prior to investing in the full 13-element system. For this demonstration, the sample clocks to the ADC boards were reduced to 1.6 GHz to accommodate an FPGA timing issue. This

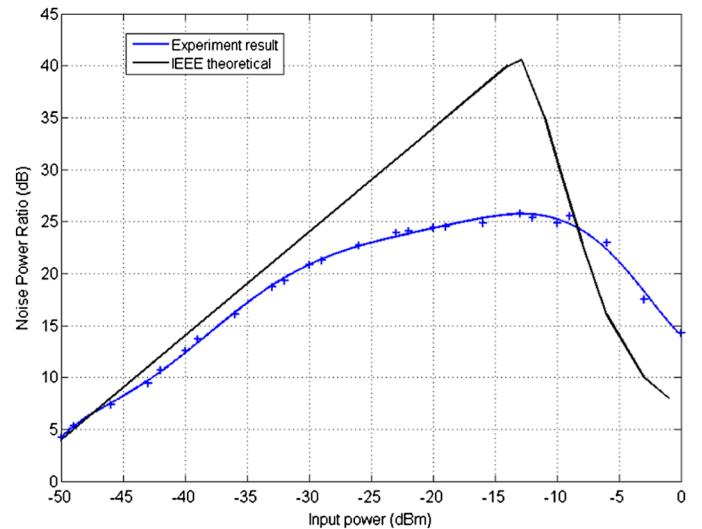


FIG. 12.—NPR performance. The black line represents the NPR for an ideal 8-bit ADC with the optimum drive occurring at -13.87 dBm. The blue line represents our empirical results with the optimum drive occurring at -12.5 dBm. See the electronic edition of the *PASP* for a color version of this figure.

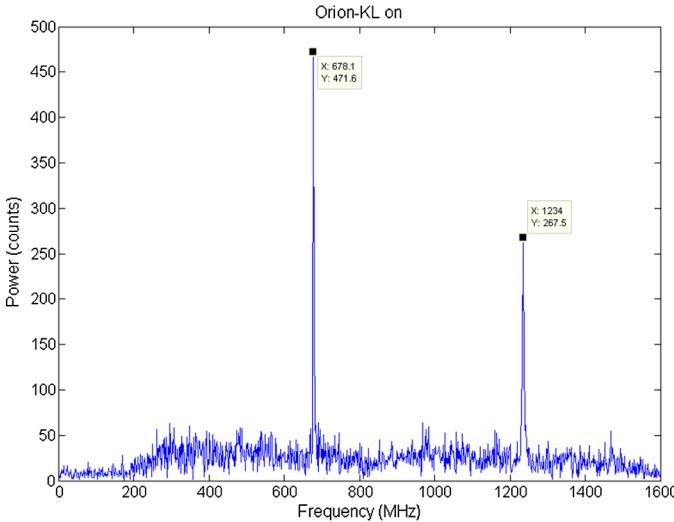


FIG. 13.—Detection of spectral lines in Orion KL. The two detected molecular lines, left to right, are HCO+ and HCN, after 59.5 minutes of integration. See the electronic edition of the *PASP* for a color version of this figure.

timing issue has since been solved and we plan to use a 2.24 GHz sample clock for an effective ADC sampling rate of 4.48 Gsp/s in our final configuration. The FPGA was programmed to transform the digitized time domain signal from each ADC into 1024 spectral channels using a poly phase filter bank (PFB) and FFT (Parsons et al. 2009). Signal correlation between the selected pair of antennas was constructed by performing a complex multiply followed by a period of integration of the channelized data within the FPGA. A PC was used to retrieve the correlated data at the end of each integration period. Figure 13 shows the results of observing Orion KL with our one-baseline correlator. The horizontal axis represents sky frequencies of 89.85 to 88.25 GHz that have been down-converted 0 to 1.6 GHz, respectively (note the spectral inversion produced by the down-conversion). The two detected spectral lines represent HCO+ and HCN with resonant rest frequencies of 88.923 and 88.367 GHz, respectively. The integration time for this observation was 59.5 minutes.

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5. SUMMARY

Prior to this work, the ADCs offered in the CASPER suite were suitable for digitizing modest amounts of analog bandwidths for applications involving a large number of apertures. We developed an ADC board that permits digitization of up to 2.4 GHz of analog signal bandwidth with 8-bits quantization. This effort was geared toward applications such as AMiBA and the Smithsonian Sub-millimeter Array (SMA) where the receiver output bandwidths are 16 GHz and 8 GHz, respectively. The ability to capture larger portions of the IF spectrum reduces the complexity and cost of the IF distribution system.

The ADC board's performance parameters were characterized over its operating bandwidth for SFDR, SINAD, and ENOB, with worst-case values of 44 dB, 35 dB, and 5.5-bits, respectively, all referring to an input drive level of -1 dBfs. These performance values were obtained after core alignment of DC offset and gain, but not phase. We believe that additional performance improvements may be gained with the optimization of the core phase alignments. It is noted that, for most astronomical observations, the input signal to the ADC is dominated by Gaussian noise where a reduction of ENOB to 4-bits (16-levels) results in only a 1% loss in sensitivity relative to continuous sampling (Thompson et al. 2001).

Having a larger dynamic range, however, leads to a more flexible instrument that can accommodate resistance to RFI. This may become important for the AMiBA telescope located on Mauna Loa because we have future plans to lower the operating frequency from W-band to 30 GHz where RFI may become an issue. Finally, for users of the ADC board in Gaussian noise dominated applications, we recommend an input drive level of -13 dBm (11 dB below full-scale drive).

The authors wish to acknowledge the assistance and support of the CASPER community, especially the University of California at Berkeley, Smithsonian Astrophysical Observatory, National Radio Astronomy Observatory, and the MeerKAT in South Africa. This work was funded, in part, by the National Science Council, Taiwan, under Grant NSC 98-2119-M-001-024-MY4, and by Academia Sinica.

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