Wafer-Level Packaging of Aluminum Nitride RF MEMS Filters

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Abstract

Aluminum nitride (AlN) radio frequency (RF) MEMS filters utilize piezoelectric coupling for high-performance electrical filters with frequency diversity in a small form factor. Furthermore, the compatibility of AlN with CMOS fabrication makes AlN extremely attractive from a commercial standpoint. A technological hurdle has been the ability to package these suspended resonator devices at a wafer level with high yield. In this work, we describe wafer-level packaging (WLP) of AlN MEMS RF filters in an all silicon package with solder balls on nickel vanadium / gold (NiV/Au) bond pads that are subsequently ready for flip chip bonding. For this integration scheme, we utilize a 150 mm device wafer, fabricated in a CMOS foundry, and bond at the wafer level to a cavity silicon wafer, which hermetically encapsulates each device. The cavity wafer is then uniformly plasma etched back using a deep reactive ion etcher resulting in a 100 μm thick hermetic silicon lid encapsulating each die, balled with 250 μm 90/10 Pb/Sn solder balls and finally diced into individually packaged dies. Each die can be frequency-trimmed to an exact frequency by rapid temperature annealing the stress of the metallization layers of each resonator. The resulting technology yields a completely packaged wafer of 900 encapsulated die (14 mm^2 by 800 μm thick) with multiple resonators and filters at various frequencies in each package.

Introduction

Piezoelectric RF MEMS have become ever more prevalent in commercial microelectronics with wide commercial acceptance of bulk acoustic wave (BAW) and surface acoustic wave devices (SAW) in portable electronics. Their use in 2G, 3G, and 4G wireless has been essential to the continual progression of portable electronics performance with their low insertion loss, high quality factor resonances, and good out of band rejection and isolation. Each method of acoustic frequency transduction has its advantages and disadvantages with regards to flexibility in fabrication, performance, and size. In this work, we employ a suspended contour mode acoustic resonator in transducing frequencies from low megahertz to gigahertz on the same chip [1]. With this method, the frequency can be defined photo lithographically, by the width of the resonator, permitting different frequencies to exist simultaneously on the same wafer and even on the same die [2]. However, suspended MEMS devices require protection once released; even singulation of the die would damage most of the devices if left unprotected. Wafer level packaging (WLP) offers a cost effective packaging alternative, while offering excellent protection for the suspended devices [3], [4], [5].

In the work presented here, we describe a process for a low cost, high yield WLP using a silicon lid wafer attached to the AlN device wafer during fabrication. A gold-silicon eutectic wafer bonds the two wafers and a plasma etch thinning process defines a 100 μm thick hermetic encapsulation. For flip chip applications, we utilize 250 μm Pb-Sn solder balls as well as a post fabrication rapid thermal anneal to provide device frequency trimming offsetting any variation effects from fabrication. This work will discuss phenomenon encountered during fabrication, such as metal induced lateral crystallization, spur dependence on metal thickness, and performance analysis of devices at low and high frequencies, 22 MHz and 500 MHz.

Device and Wafer Level Packaging Process

In this section, the fabrication sequence for creating WLP RF resonators and filters will be detailed. The essential aspect of the process is separate fabrication of the lid wafer device wafer are manufactured in Sandia's CMOS MESA Fab. This permits variation in resonator or filter design and frequency while holding the packaging process constant and independently tunable. A device wafer is fabricated consisting of contour mode acoustic AlN MEMS resonators and a lid wafer is etched to create the cavity for the silicon package. The two wafers are then brought together, and bonded with a eutectic bond. The lid wafer is then thinned forming a 100 um thick hermetic, silicon shell around the devices at the wafer level.

The device wafer is fabricated using a multilayer metal process, which can be with back end of the line (BEOL) tools. Poly silicon is first deposited in silicon dioxide trenches and planarized on a 150 mm wafer; these silicon pits become the resonator dry release layer. A frequency compensating silicon dioxide is then deposited 1.5 um thick; although this reduces the k_{eff}^2 of the AlN resonator devices it does improve thermal-frequency stability to low ppm levels by offsetting AlN's negative thermal coefficient of frequency (TCF) with silicon dioxides positive TCF [6], [7]. Tungsten vias to connect bottom metal with top metal are then created by first etching down into the oxide layer, then filling with tungsten, and finally planarizing the tungsten using CMP. By connecting to bottom metal with W, an underpass is created for sending RF signals into and out of the packaged area. Bottom metal is then deposited and patterned consisting of Ti/TiN/AlCu where the thickness can be varied as needed by device requirements with thicknesses of devices reported here of 20 nm/ 50 nm/ 100 nm. AlN is then RF sputter deposited to 750 nm thickness and annealed creating the piezoelectric transduction layer. Vias in the AlN to connect top metal to the W underpass are then etched open. Top metal is then deposited with typical metal layers of AlCu / TiN and thicknesses of 100 nm / 50 nm respectively. The top metal, defining the top resonator electrode, is then patterned with lithographic

resolution below 250 nm using an ASML and Nikon stepper. A thick 1∞m AlCu layer is then deposited and patterned for trace lines within the package. The resonator is re-patterned and etched through the top metal, AlN and bottom metal layer landing on the silicon release layer or oxide; this etch defines the sidewalls of the resonator. A contact pad layer is then deposited using a Ti/NiV/Au metallization stack with 50 nm/ 300 nm/ 100 nm. To create the bond ring, which will attach the lid wafer and the die wafer, a Ti/Pt/Au layer is deposited with 20 nm/ 100 nm/ 500 nm respectively. The resonators are then dry released at the wafer level by first patterning resist, to protect the Au layer, then removing the poly silicon layer under the AlN using a XeF_2 etch; without wafer level packaging the release step would be required to be performed after dicing the wafer at the die level to prevent stiction to the substrate, Fig. 1. Hence, WLP is seen as critical for the simultaneous release of these 900 MEMS die per wafer.
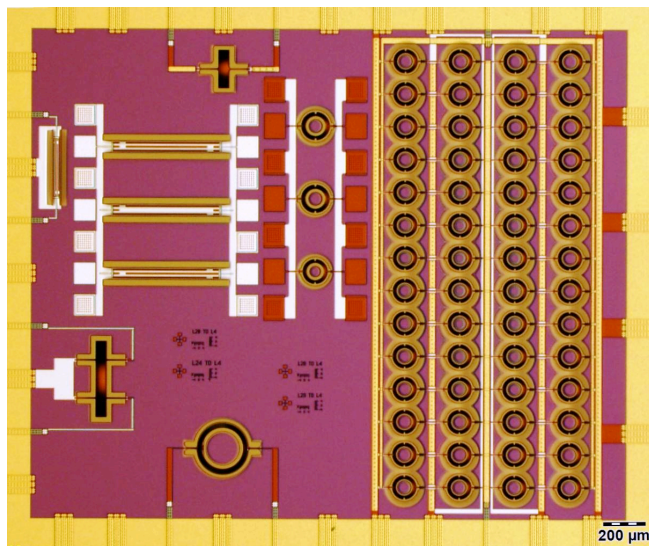

Figure 1: Optical image of released AlN resonators and RF filters before WLP.

The lid wafer is also created in the CMOS foundry from high resistivity silicon, 5 kOhm-cm, and three photolithographic masks. The utilization of high resistivity silicon reduces RF electrical loss and capacitive parasitics. A first etch patterns a 3 ∞m silicon ridge defining the bonding region. A second etch patterns a 100 ∞m trench above the external contact pads are; after bonding, a silicon back etch will land on the floor of this etch (with the etch progressing from the backside of the wafer) revealing the contact pads. Finally, the third etch creates a 20 ∞m deep area which serves as the device chamber. Perturbation of the second etch changes the thickness of the final encapsulation while perturbation of the third etch changes the volume of the device cavity. After the etching is completed, the wafer is thoroughly cleaned with solvents, Piranha etch and HF, and a 250 nm thermal silicon dioxide is grown. This oxide layer serves as a diffusion barrier during the wafer level bonding process, keeping the eutectic from interacting with the substrate and creating voids [8], [9]. Finally, a 136 nm thick amorphous silicon (a-Si) layer is deposited using 400 ºC

PECVD. A cross-section of a completed wafer is seen in Fig. 2. The silicon thickness is determined such that a 19% Au-Si eutectic can be created using the 500 nm Au bond ring on the device wafer for wafer level bonding [10].
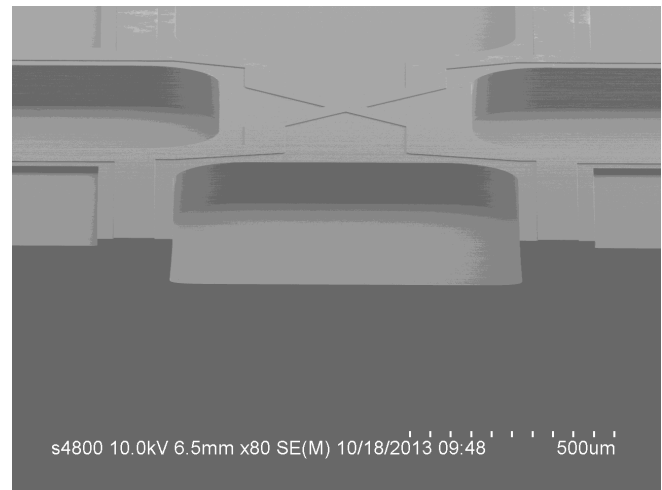

Figure 2: SEM cross-sectional image of the lid wafer. The 3 ∞m ridge serves as the bonding region, the 20 ∞m etch serves as the die cavity, and the 100 ∞m etch serves as the pad reveal.

With completion of the fabrication sequence, the lid wafer and device wafer are aligned and bonded in an EVG 520 bonder. The bonding sequence first the chamber to 10^{-6} Torr, heats the wafers to 110 ºC for 6-12 hours to bake out moisture, and then bonds the wafers at 400 ºC for 25 minutes under 3 to 5 kN of force. During cool down from the 400 ºC bond temperatures, the chamber is purged with N_2 gas to raise the chamber pressure to 1 psi such that the temperature variance is reduced between the top and bottom wafer. The bonded wafer is then inspected using an IR camera to ensure the eutectic formed a seal around the die, Fig. 3.
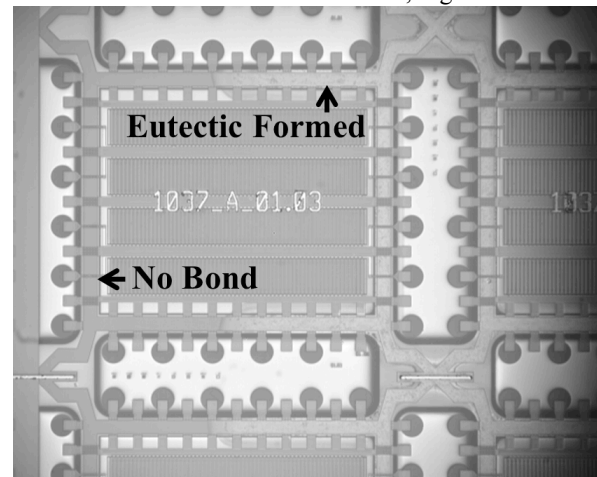

Figure 3: IR, thru wafer image of bonded wafers indicating where the eutectic was formed and where the bond did not occur.

Following bond, a plasma etch in an PlasmaTherm inductively coupled plasma reactive ion etcher (ICP RIE is

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performed, with 2000 W ICP power, 10 volts LF bias, 15 mTorr pressure and 100 sccm of SF_6 to etch 550 µm of silicon off the backside of the lid wafer. A plasma etch is preferred to back grinding of the wafer since no mechanical stress is applied to the bonded wafer stack and the fluorine etch leaves no residue. Due to the high selectivity to silicon dioxide, the fluorine etch can land hard on the oxide coating the base of the pad area in the lid. The result is a 100 µm thin silicon lid encapsulating the wafer level released AlN resonators, Fig 4. Analysis of the wafer shows all dies with bonded lids out of 900 die per wafer but with most of the outer dies only partially sealed. The roughness of the lid surface is due to the roughness of the single sided polished lid wafer and not currently thought to impact device performance.
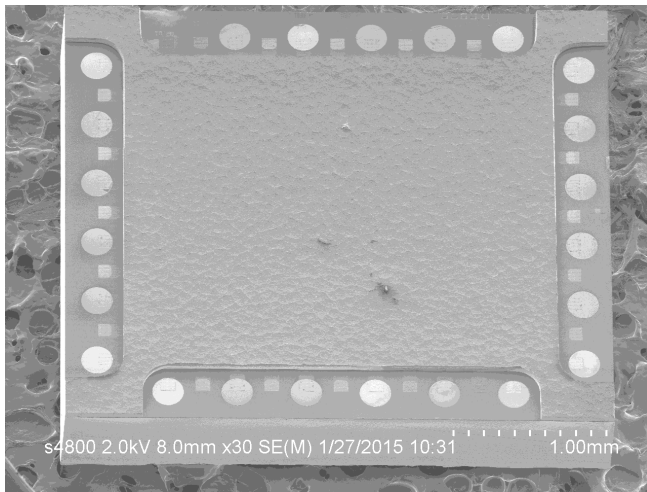

Figure 4: SEM image of a WLP AlN die after back etch and dicing.

Post Fabrication Processes

Upon completion of wafer level packaging, several post fabrication options can be combined in various sequences: wafer level automated RF testing, rapid thermal anneal (RTA) for resonator and filter frequency trimming, Laser Solder balling, and wafer dicing.
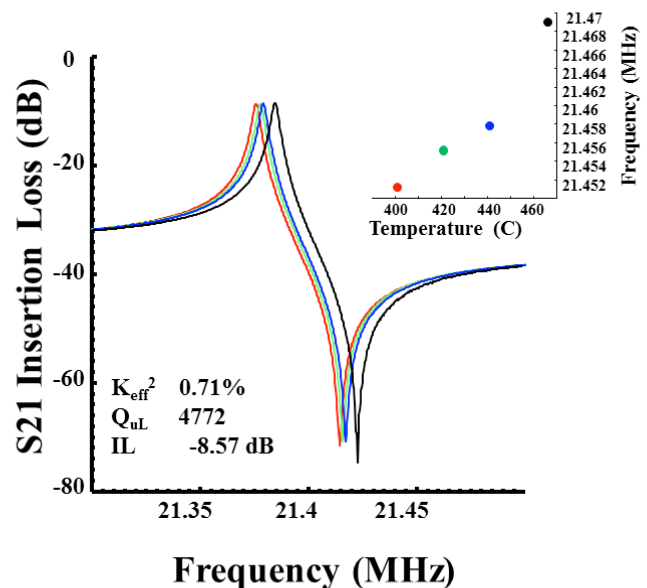
Using a Cascade PS-21 autoprober and Agilent E5071C network analyzer, the packaged resonators and filters are then tested to ensure device performance; since the testing can be done at the wafer level, device testing can be automated and performed inexpensively. All electronic tests reported here utilize this testing method.

Due to fabrication variance across wafer, it is typical to have a 2% frequency distribution in resonance frequency. Using a rapid thermal annealer (RTA), short temperature excursions of 5 minutes between 400 and 500 ºC, permit exact frequency trimming of both resonators and filters [11]. Deposited top and bottom metal contribute to the overall modulus and density of the resonator, while simultaneously serving to establish the electric field across the AlN piezoelectric required for acoustic wave transduction. The resonators and filters created here are Lamb-wave mode resonators in which the resonator frequency (f) is determined by lateral dimension (L) of the device and velocity of the sound wave (v) is controlled by the square root of resonator's film stack elastic modulus (E) and inverse square root of the density (ρ), Equation 1 [12]. The summation is taken over all the materials in the resonator stack and their thicknesses (t). By annealing the device, the metal stacks tend to reduce stress thereby increasing their elastic modulus while the AlN and oxide tend to remain constant. This stress reduction up shifts the resonator frequency and can be used as a method for post fabrication resonator trimming.

$$f = \frac{v}{2L} = \frac{1}{2L} * \sqrt{\frac{\sum E*t}{\sum \rho*t}} \qquad (1)$$

As example, the product wafer described here was tested, annealed, and then retested for RTA temperatures of 400, 420, 440, 465, and 475 ºC. The devices tested were 22 MHz and 500 MHz resonators and a 4 pole 500 MHz filter, Fig. 5 a,b,c respectively. The annealing was performed in 1 Torr of Ar purged vacuum for 5 minutes at the prescribed temperature. For the 22 MHz filter the frequency up shift was from about 0.1%, displayed here with the parallel resonance starting at 21.45 MHz after fabrication to 21.47 MHz after a 465 ºC anneal. The 500 MHz resonators upshifted only about ½ %, displayed here starting at 500.2 MHz and going to 502.6 MHz after a 475 ºC anneal. The filter upshifted from 500.7 MHz to 501.4 MHz after a 465 ºC anneal. In addition to frequency shift, resonators also tend to reduce in insertion loss from the annealing; an artifact most likely attributable to a change in the elastic modulus improving the Q and thereby reducing the motional impedance.

Figure 6: SEM image of a WLP AlN wafer after ball attach and dice. The lid is 100 um thick silicon and the balls are 250 ∝m $Pb_{90}Sn_{10}$.
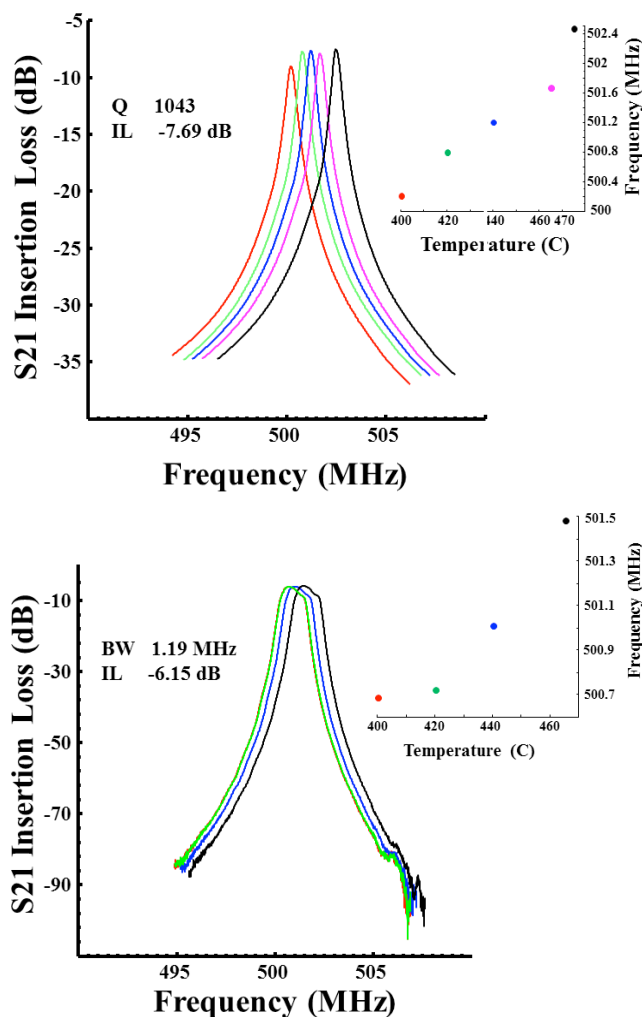

Figure 5: Transmission measurements of a) 22 MHz resonator, b) 500 MHz resonator, and c) a 500 MHz 4 pole filter after multiple anneals demonstrating frequency trimming. Insets shows the frequency up-shifting with each anneal temperature.

Previously described, the bond pad metallization consists of a metallization stack with 50 nm Ti / 300 nm NiV / 100 nm Au. The Ti layer serves as the adhesion layer, the NiV layer serves as diffusion barrier to Sn, and the Au layer reduces the surface oxidation of the NiV. $Pb_{90}Sn_{10}$ solder balls were chosen due to the low Sn content to reduce the formation of Ni/Sn intermetallics. The $Pb_{90}Sn_{10}$ solder balls are deposited using a PacTech SB2-SM laser solder jetter. The jetting capillary dispenses the 250 ∝m diameter solder balls from a height of 280 ∝m above the surface of the bond pads. A laser current of 5300 mA for a pulse width of 5 ms is used to melt the solder balls and a N_2 pressure of 60 mbar is used to dispense the solder balls onto the bond pads. Wafer scale jetting was performed at a deposition rate of 3 solder balls per second while populating the wafer, Fig. 6.
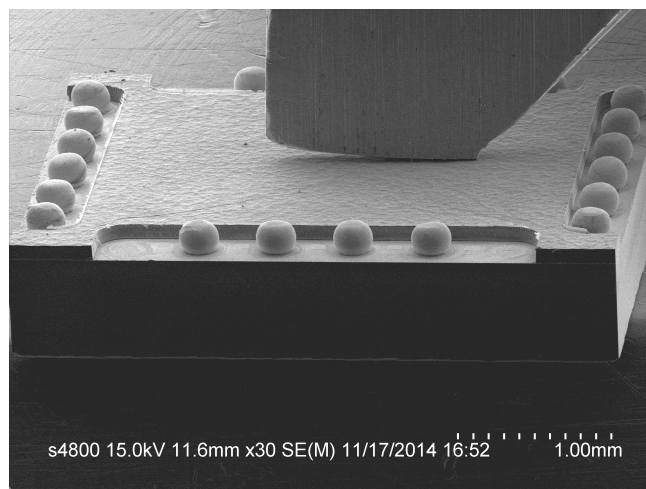
Finally, since a hermetic silicon lid encapsulates the released resonators, wafer level dicing is now possible and is used to singulate the die. Although during this process debris can be distributed across the wafer; subsequent cleaning etches can adequately re-clean the devices. We hypothesize that the debris mostly consists of Si and organics, such as resist, and utilize a two step etch with an O_2 plasma etch with 300 W bias power for 60 seconds and an SF_6 plasma etch for 60 seconds, Fig. 7.
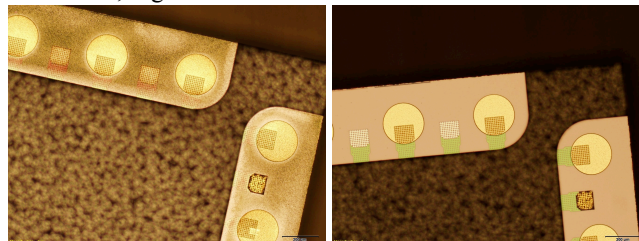

Figure 7: Left image shows Au contact pad after dicing and right image shows the same pad after plasma clean.

Although device testing, RTA trimming, solder balling, and dicing were discussed individually there is a heavy dependence on the sequence order. For example, while RTA trimming and solder balling can be performed at the wafer or die level, heat restrictions of the balling require that it should be performed after RTA anneals. Two standard sequences utilized are: 1) testing, dicing, plasma clean, RTA anneal, and balling or 2) testing, RTA anneal, plasma clean, balling, and dicing.

Fabrication Specifics

This section discusses observed phenomena occurring during the WLP process and fabrication which impacts yield. One phenomenon observed was metal induced lateral crystallization (MILC) [13]. During the bonding process, the Au bond line makes contact with the a-Si pad on the lid wafer. The desired effect is a diffusion of Si into the Au, creating a liquidous Au-Si eutectic. Upon cooling the wafers below 363

°C, the eutectic passes directly into a solid phase without creation of a dual solid and liquid phase in which Au or Si can aggregate out of solution. This event occurs for an optimal Si of 19% at. Due to the sputtering of a-Si on the lid wafer, a 25-minute bond at 400 °C also results in the a-Si laterally crystallizing and creating poly-silicon dendrites. During this phase transformation the well-adhered amorphous silicon becomes flaking poly-silicon potentially adding particle defects, Fig. 8. To limit this effect, the etch defining the lid cavity and contact pad opening on the lid wafer were adjusted to be slightly reentrant to reduce the coverage a-Si sputtering. This reduces the MILC rate to keep dendrites from forming in the main cavity.
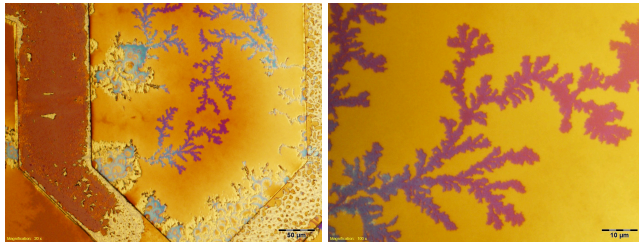

Figure 8: Left image shows the bond line with MILC of the sputtered a-Si creating particles; right image shows increased magnification of the dendritic growth. Scale bars are 50 and 10 μm for the left and right images.

The thickness of the metal stack has a profound effect upon the resonator. Not only does the metal stack shift the resonance by altering the acoustic velocity of the material, as predicted by Equation 1, but it also is observed to shift spurious modes (spurs) as well. Although much research continues in predicting the frequency of spurs, it is clear that they arise due to both piezo-electrical coupling and geometrically supported acoustic modes. If a spur has a frequency close to the main resonance, it can have multiple negative effects on the main resonance such as increasing insertion loss and providing poor band rejection/isolation. As an example of the profound effect on frequency, Fig. 9 shows a 22 MHz resonator with various thicknesses in the metal stack. These wafers were fabricated at the same time and die selected from the same area on the wafer, but with changes to the bottom and top metal thickness in TiN (25 or 50 nm) and AlCu (50 to 340 nm) holding the temperature compensating oxide and AlN constant. Although only 1 resonator from each wafer is displayed here, they were chosen, as representatives of the 300 die measured. The resonances were observed to shift almost 2 MHz over the various metal stacks, inset of Fig. 9, with spurs distributed observed across the frequency range, Fig. 9. More interesting is that the spurs are not the same size nor even have constant relative location with respect to the main resonance. This observation suggests that correct choice of the metal thickness can shift supported resonator modes and move spurs away from the frequency of choice. The metal thicknesses reported in section 2 were determined to be most optimal for the 22 MHz and the 500 MHz resonators described here.
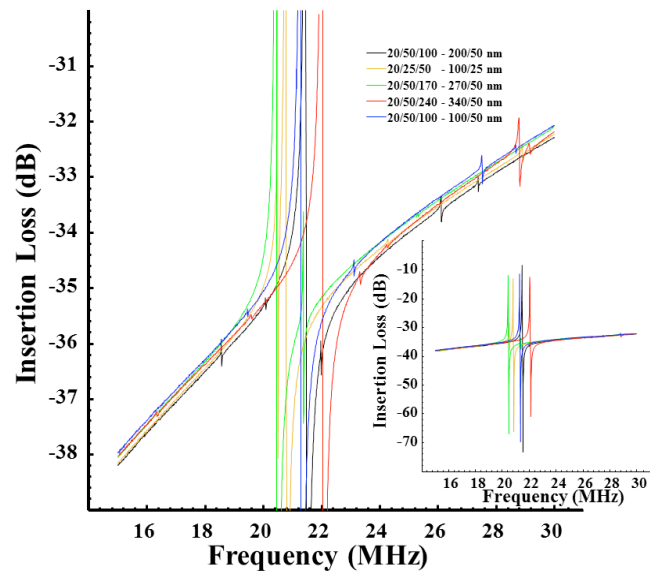

Figure 9: Resonator S_{21} performance for 22 MHz resonators with varying electrode metal thickness. Inset: wide range S_{21} performance.

Resonator and Filter Performance

Although individual devices have been reported here, Fig. 5a and Fig. 9, this section discusses wafer yield based on piezoelectric film and device performance. Two very important parameters for acoustic resonators are the coupling coefficient (k_{eff}^2) of the device and the quality factor (Q). Both parameters can be used to back out other resonator parameters and the combination of the two is widely utilized in the figure of merit for acoustic resonators and filters. Using the 22 MHz resonators, similar to Fig. 5a and Fig. 9, the k_{eff}^2 is determined by examination of the series resonance (f_s) and the parallel resonance (f_p), Equation 2.

$$k_{eff}^2 = \frac{f_p^2 - f_s^2}{f_p^2} \tag{2}$$

Out of the measured 60 die from this wafer, 54 working 22 MHz resonators yielded a mean k_{eff}^2 of 0.70%.

The Q factor is reported here as the unloaded Q factor and is determined by the series resonance at full width, half maximum. Since the 22 MHz resonators operate at lower frequency, the device is more susceptible to air dampening which lowers the Q, Fig. 10. Of the 60 devices, 6 were non-functional (no measurable resonance), 4 had spurs on resonance, 17 had higher Q values indicating they were under some level of vacuum, and 33 had Q factors indicating low vacuum or atmosphere. Of the 50 devices performing well the Q values spanned over 2000 based on both the device and vacuum level in the cavity. The mean insertion loss was -10.6 dB with a standard deviation of 1.3.
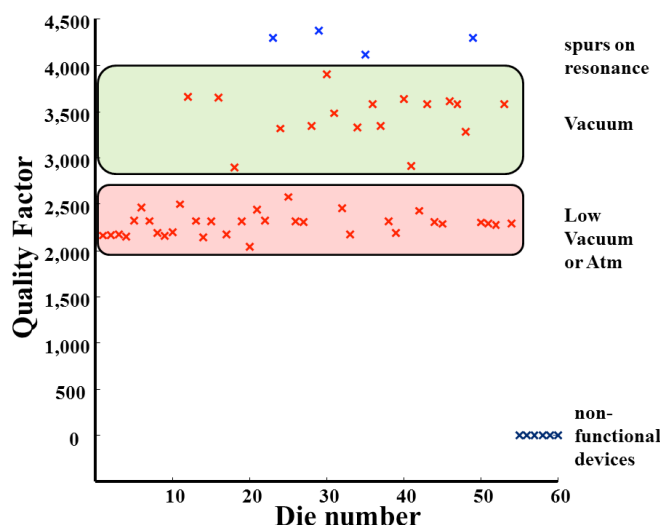
Figure 10: Wafer level data of Q factor using the 22 MHz resonator. Resonators demonstrating good performance and under WLP vacuum typically had Q's of 2800-4000 whereas packages at atmosphere but hermetic had Q's of 2000-2700.

The 500 MHz resonator is not affected by chamber gas pressure to the same extent as the lower resonant frequencies, Fig. 11. Of the 60 resonators, 15 had spurs preventing a minimum of 5 dB isolation outside of resonance, 5 resonators had unacceptable insertion loss (more than -10 dB), and 40 resonators performed well. Of the resonators performing well, the Q values spanned only 800 indicating a significantly less dependence on vacuum when compared with the 22 MHz results. The mean insertion loss was -7.5 dB with a standard deviation of 0.6 dB.
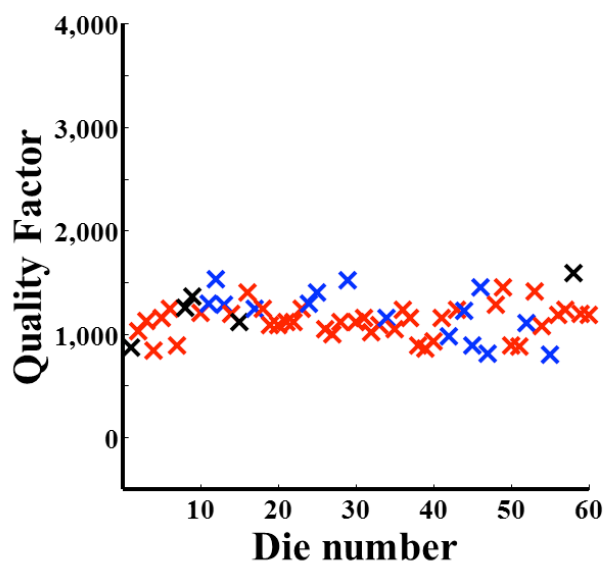

Figure 11: Wafer level data of Q factor using the 500 MHz resonators. Resonators demonstrating good performance, red, are compared here with poorly performing and non-functional resonators, blue and black respectively.

Conclusions

In this work, we have detailed a WLP process using silicon substrates for encapsulation of thin film AlN RF resonators and filters. The MEMs technology described here permits an inexpensive device release and packaging technique, at the wafer level, with hermetic silicon lids and solders balls for flip chip bonding. As part of the packaging efforts, this work describes the effects of metallization on resonant frequencies and frequency trimming while noting other phenomenon such as MILC.

By having a lid wafer fabricated separately from the device wafer, this technology becomes applicable for a wide range of device wafers. This greatly reduces costs by maintaining an inexpensive packaging technology in the same fabrication facility generating the device. Although the AlN film utilizing the d_{31} coupling, in the method described here, does not present piezoelectric coupling as high as $LiNbO_3$ or $LiTaO_3$ SAW resonator, it does have several advantages in that a 22 MHz filter can be packaged with a 500 MHz filter, a low impedance 22 MHz resonator can be realized in a small volume and a high Q factor can be obtained. Technology improvements in the piezoelectric film, could propel this method for acoustic RF Filters over that of SAW or BAWs [14].

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