## Salmoun Abolfathe

becture 7: Fault toberance and the threshold.

- 1) Analog rs Digital
- 3 concept computational complexity
- 3) the threshold thin
- 4) FTQC The threshold.

Il Analog comp

=> QC + Analog comp

Def/ Analog Comp

Input \_\_\_ output

 $\vec{X}(0) = \{x_0, \dots x_n\} \quad \vec{X}(T)$ 

 $\frac{d\vec{X}}{dt} = F(\vec{X})$ 

Assumptions

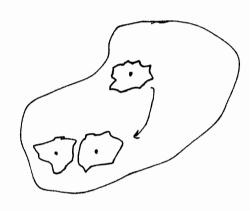
- O No noise in evolution
- 2) perfect measurment.

Thm/ Analog comp Reduces

in the presence of finite noise

or meas. error.

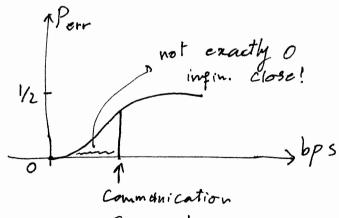
Idea



QC + noise ? Digital comp

II / computational capacity

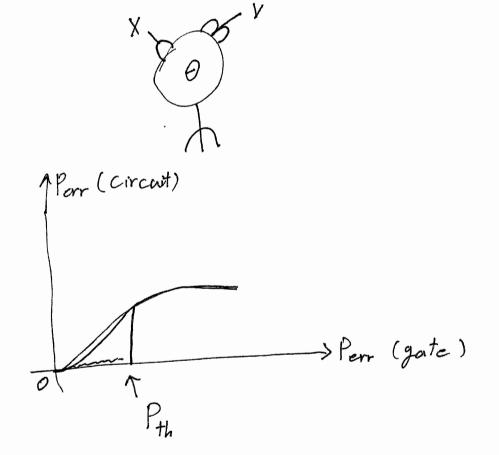
=> Communication (1940's Shannon)



Capacity.

=> 1956 Von Neamann

"Probabilistic logics and the synthesis of reliable organisms from unreliable components"



Observation

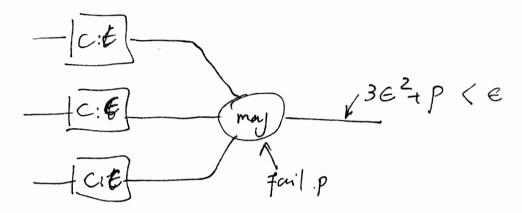
A circuit containing N crror-free gates

Can be simmulated w.p. error (E

Using O(MM) gates which fail w.p. error

P < P+h

Choose Pth ~ E/N



problems

- Inefficient # gates ~ 1/E

- Not a threshold. P+h~ indep of N, E

- avoid single points of failure

II/ The threshold thm.

A circuit with N error-free gates can be similated w.p. error  $\langle E$  using O(pdy(log NE).N) gates which fail up p as long  $P(P_{th}$ , where  $P_{th}$  is indep of N, E

## Proof Statch

Idea: compute on encoded data, never decode.

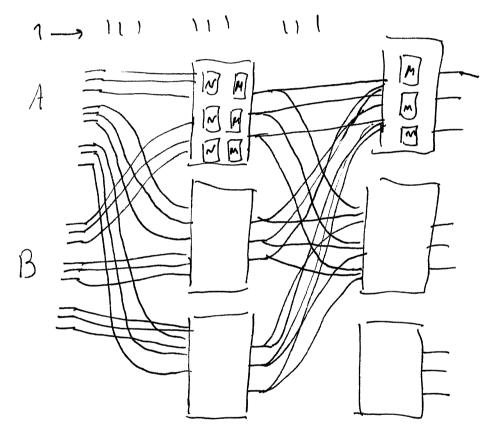
each fails w.p. ~p

output is wrong only if there are two or more failures

$$\sim \binom{8}{2} = 15$$
 possibilities  
Pfail  $\simeq 15$  P<sup>2</sup>

## Good if P< 1/15

level 2 encoding



$$P_{fail} \sim {6 \choose 2} (15p^2)^2$$

In general if C fault paths

$$CP_{fail} = (CP)^{2}$$
 $CP_{fail} = (CP)^{4}$ 
 $CP_{fail} = (CP)^{2k}$ 

$$P_{th} = 1/C \leftarrow 1 \text{ nobe} P. \text{ of } N, C$$

$$P_{th} = \left(\frac{P}{P_{th}}\right)^{2k}$$

$$P_{th} = \left(\frac{P}{P_{th}}\right)^{2k}$$

$$P_{th} = P_{th}$$

IV/ Fault Tolerance Criteria

def/ A procedure is FT if a single component failure causes at most one error in each encoded block of bits in the output.

good

| bad

| land

| land

| land

| land

| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land
| land

cost of FT

circuit size ~ dk & Foriginal circuit

d = size of FT procedure

what's k?

\(\left(\frac{P}{P\_{th}}\right)^{2k}\)\(\frac{E}{NP\_{th}}\)
\(2^{k}\log\left(\frac{P}{P\_{th}}\right)\)\(\log\left(\frac{P}{NP\_{th}}\right)\)
\(2^{k}\log\left(\frac{P}{NP\_{th}}\right)\)
\(2^{k}\log\left(\frac{P}{NP\_{th}}\right)\)
\(2^{k}\log\left(\frac{P}{NP\_{th}}\right)\)
\(2^{k}\log\left(\frac{P}{NP\_{th}}\right)\)

=) Circuit Size is

$$Nd^{k} \simeq \left( \frac{\log \frac{E}{NP_{th}}}{\log \frac{P}{P_{th}}} \right)^{\log d}$$
 $\frac{\log \frac{P}{P_{th}}}{\log \frac{P}{P_{th}}}$ 

- 1 ...

, etc., etc.

## I/ FTQC and threshold

Two principles

- 1) compute on encoded data
- 2) control/1.mit error propagation

> universal gate set?

CSS codes: {H,S, CNOT}

Clifford gates # univ. Qc.

Note: the Toffoli:

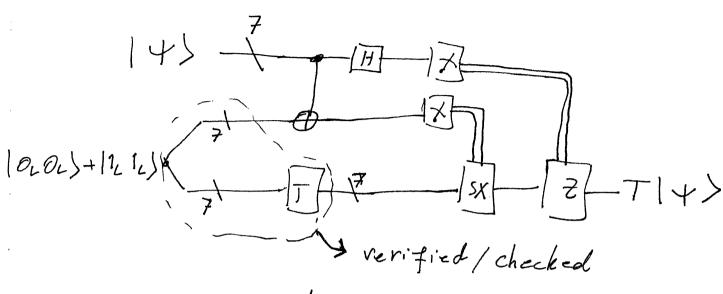
271/3

OL) + e 1/23 /1/2)

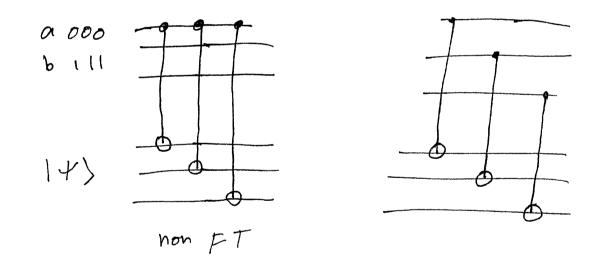
Lo univ. QC.

claim  $T = \begin{bmatrix} 1 & 0 \\ 0 & \sqrt{1} \end{bmatrix} \sim \sqrt{5} \sim \sqrt{4}\sqrt{2}$ 

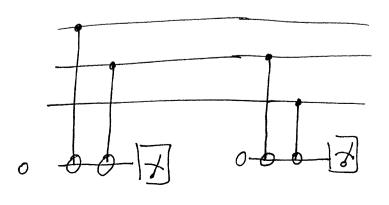
elifford gates meas. (2) and pre-prepared entangelment.

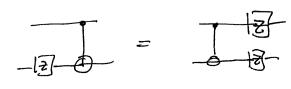


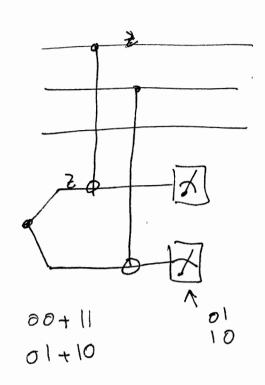
=> error propagation



Syndrome meas







Stean = 7-qubit code

72 gates

$$2\left(\frac{79}{2}\right) = 3081$$
 fault paths