DATA SHEET

4G bits DDR2 Mobile RAM™

LD2E5E304G

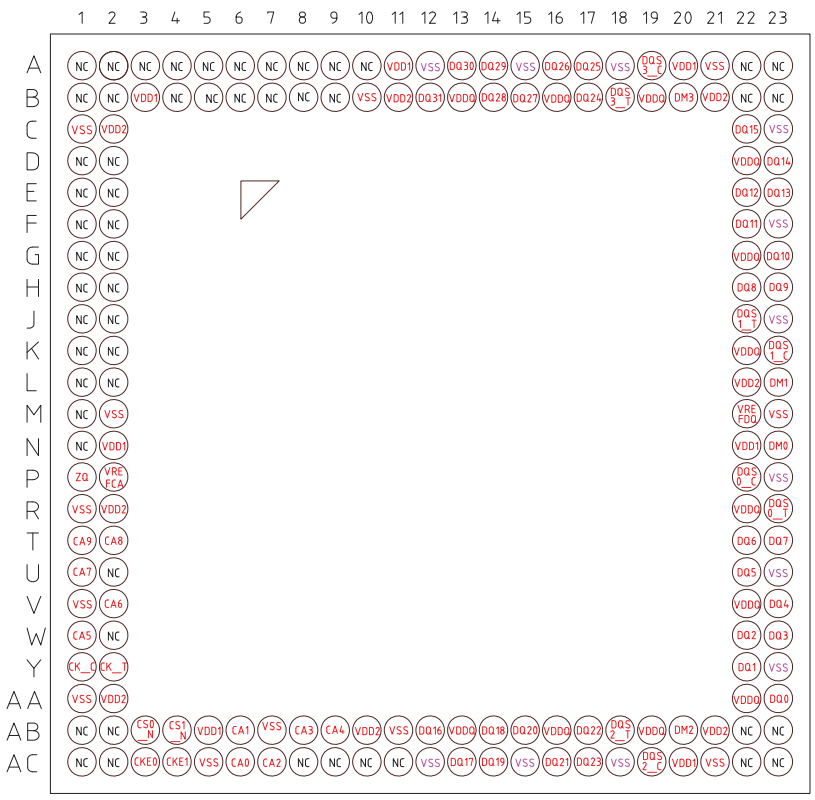
Specifications

- Density: 4G bits
- Organization
  - × 16 bits: 16M words × 16 bits × 8 banks
  - × 32 bits: 8M words × 32 bits × 8 banks
- Package: FBGA168ball,2 dies
- Power supply
  - VDD1 = 1.70V to 1.95V
  - VDD2, VDDQ = 1.14V to 1.30V
- Data rate: 1066Mbps max. (RL = 8)
- 2KB page size
  - Row address: R0 to R13
  - Column address: C0 to C9 (× 16 bits)
    C0 to C8 (× 32 bits)
- Eight internal banks for concurrent operation
- Interface: HSUL_12
- Burst lengths (BL): 4, 8, 16
- Burst type (BT)
  - Sequential (4, 8, 16)
  - Interleave (4, 8)
- Read latency (RL): 3, 4, 5, 6, 7, 8
- Precharge: auto precharge option for each burst access
- Programmable driver strength
- Refresh: auto-refresh, self-refresh
- Refresh cycles: 8192 cycles/32ms
  - Average refresh period: 3.9μs
- Operating junction temperature range
  - TJ = -30°C to +85°C

Features

- DLL is not implemented
- Low power consumption
- JEDEC LPDDR2-S4B compliance
- Per Bank Refresh
- Partial Array Self-Refresh (PASR)
  - Bank Masking
  - Segment Masking
- Auto Temperature Compensated Self-Refresh (ATCSR) by built-in temperature sensor
- Deep power-down mode
- Double-data-rate architecture; two data transfers per one clock cycle
- The high-speed data transfer is realized by the 4 bits prefetch pipelined architecture
- Differential clock inputs (CK and /CK)
- Bi-directional differential data strobe (DQS and /DQS)
- Commands entered on both rising and falling CK edge; data and data mask referenced to both edges of DQS
- Data mask (DM) for write data
- Burst termination by burst stop command
- Please contact your supplier to decide to use which data rate

Ball Assignment



Bottom side
(Top View)

REVISION HISTORY

REV	DESCRIPTION	RELEASED BY	DATE
A	New Issue		

APPROVALS		DATE
DRAWING		
CHECKED	------	------
APPROVED		

CUSTOMER DRAWING NO.: --------

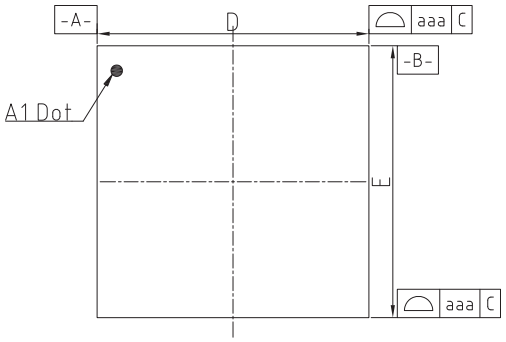
TITLE:
PIN ASSIGNMENT
for EMMC 12mm×12mm 168B

DWG. NO.: Rev. A

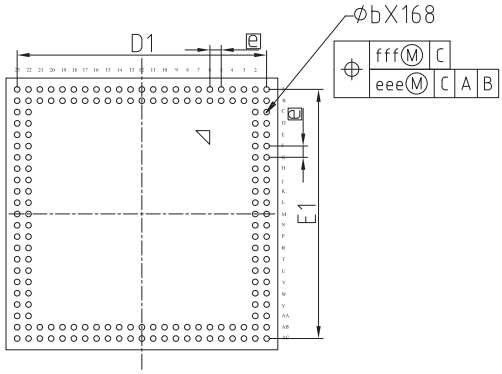
SIZE: Letter | SCALE: 1 : 1 | SHEET 1 of 1

Package Drawing

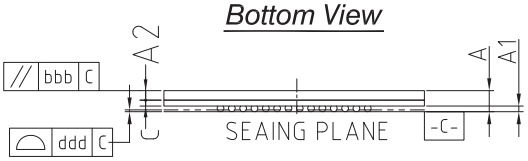
REVISION HISTORY			
REV.	DESCRIPTION	RELEASED BY	DATE
A	New Issue		



Top View



Bottom View



Side View

Symbol	Dimension in mm		
	Min	Nom	Max
A	---	---	1.00
A1	0.17	0.21	0.25
A2	0.51	0.53	0.54
c	0.15	0.18	0.21
ϕb	0.25	0.30	0.35
D	11.90	12.00	12.10
D1	---	11	---
E	11.90	12.00	12.10
E1	---	11	---
e	0.50 BSC		
aaa	0.15		
bbb	0.20		
ddd	0.20		
eee	0.15		
fff	0.10		
MD/ME	23/23		

NOTE:
1.CONTROLLING DIMENSION: MILLIMETER.
2.REFERANCE DOCUMENT:JEDEC MO-273
3.CONTROLLING DIMENSION : MILLIMETER

PROJECTION

DIMENSIONING
UNLESS OTHERWISE SPECIFIED
ALL DIMENSIONS ARE IN MM.
ALL PROJECTIONS ARE THIRD ORDER.

TOLERANCES:
LINEAR
X.X = ±0.1
X.XX =±0.05
X.XXX =±0.025
ANGULAR ±1°

APPROVALS		DATE
DRAWING		
CHECKED	---	---
APPROVED		
CUSTOMER		

CUSTOMER DRAWING NO.: --------

TITLE: PACKAGE OUTLINE DRAWING
168B BGA 12x12mm
T= 1.00mm max
SBT T=0.18mm

DWG. NO.: POD714 Rev. A

SIZE: Letter SCALE: 1:1 SHEET 1 of 1

Contents

1. Electrical Conditions

- All voltages are referenced to VSS (GND)
- Execute power-up and Initialization sequence before proper device operation is achieved.
- Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the DDR2 Mobile RAM Device must be powered down and then restarted through the specialized initialization sequence before normal operation can continue.

1.1 Absolute Maximum Ratings

Table 1 Absolute Maximum Ratings

Parameter	Symbol	min.	max.	Unit	Note
VDD1 supply voltage relative to VSS	VDD1	-0.4	2.3	V	2
VDD2 supply voltage relative to VSS	VDD2	-0.4	1.6	V	2
VDDQ supply voltage relative to VSSQ	VDDQ	-0.4	1.6	V	2, 3
Voltage on any ball relative to VSS	VIN, VOUT	-0.4	1.6	V	
Storage Temperature	TSTG	-55	125	°C	

Notes: 1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. See Power-Ramp section “Power-up, initialization and Power-Off” on page 56 for relationship between power supplies.
3. VREF ≤ 0.6 x VDDQ; however, VREF may be ≥ VDDQ provided that VREF ≤ 300mV.
4. Storage Temperature is the case surface temperature on the center/top side of the DDR2 Mobile RAM Device. For the measurement conditions, please refer to JESD51-2 standard.

Caution

Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

1.2 Recommended DC Operating Conditions

Table 2 Recommended DC Operating Conditions(TJ = -30°C to +85°C)

Parameter	Symbol	min.	typ.	max.	Unit
Core Power1	VDD1	1.70	1.80	1.95	V
Core Power2, Input Buffer Power	VDD2	1.14	1.20	1.30	V
I/O Buffer Power	VDDQ	1.14	1.20	1.30	V

1.3 AC and DC Input Measurement Levels

1.3.1 AC and DC Input Levels for Single-Ended CA and /CS Signals

Table 3 Single-Ended AC and DC Input Levels for CA and /CS Inputs

Parameter	Symbol	Speed	min.	max.	Unit	Note
AC input logic high	VIHCA(AC)	533 to 1066	VREF + 0.220	Note 2	V	1, 2
		400	VREF + 0.300			
AC input logic low	VILCA(AC)	533 to 1066	Note 2	VREF - 0.220	V	1, 2
		400		VREF - 0.300		
DC input logic high	VIHCA(DC)	533 to 1066	VREF + 0.130	VDD2	V	1
		400	VREF + 0.200			
DC input logic low	VILCA(DC)	533 to 1066	VSS	VREF - 0.130	V	1
		400		VREF - 0.200		
Reference Voltage for CA and /CS inputs	VREFCA(DC)		0.49 × VDD2	0.51 × VDD2	V	3, 4

Notes: 1. For CA and /CS input only pins. VREF = VREFCA(DC).
2. See “Overshoot and Undershoot Specifications” on page 17.
3. The ac peak noise on VREFCA may not allow VREFCA to deviate from VREFCA(DC) by more than ± 1% VDD2 (for reference: approx. ± 12 mV).
4. For reference: approx. VDD2/2 ± 12 mV.

1.3.2 AC and DC Input Levels for CKE

Table 4 Single-Ended AC and DC Input Levels for CKE

Parameter	Symbol	min.	max.	Unit	Note
CKE Input High Level	VIHCKE	0.8 × VDD2	Note 1	V	1
CKE Input Low Level	VILCKE	Note 1	0.2 × VDD2	V	1

Note: 1. See “Overshoot and Undershoot Specifications” on page 17.

1.3.3 AC and DC Input Levels for Single-Ended Data Signals

Table 5 Single-Ended AC and DC Input Levels for DQ and DM

Parameter	Symbol	Speed	min.	max.	Unit	Note
AC input logic high	VIHDQ(AC)	533 to 1066	VREF + 0.220	Note 2	V	1, 2
		400	VREF + 0.300			
AC input logic low	VILDQ(AC)	533 to 1066	Note 2	VREF - 0.220	V	1, 2
		400		VREF - 0.300		
DC input logic high	VIHDQ(DC)	533 to 1066	VREF + 0.130	VDDQ	V	1
		400	VREF + 0.200			
DC input logic low	VILDQ(DC)	533 to 1066	VSSQ	VREF - 0.130	V	1
		400		VREF - 0.200		
Reference Voltage for DQ, DM inputs	VREFDQ(DC)		0.49 × VDDQ	0.51 × VDDQ	V	3, 4

Notes: 1. For DQ input only pins. VREF = VREFDQ(DC).
2. See “Overshoot and Undershoot Specifications” on page 17.
3. The ac peak noise on VREFDQ may not allow VREFDQ to deviate from VREFDQ(DC) by more than ± 1% VDDQ (for reference: approx. ± 12 mV).
4. For reference: approx. VDDQ ± 12 mV.

1.4 VREF Tolerances

The dc-tolerance limits and ac-noise limits for the reference voltages VREFCA and VREFDQ are illustrated in Figure 1. It shows a valid reference voltage VREF(t) as a function of time. (VREF stands for VREFCA and VREFDQ likewise).

VDD stands for VDD2 for VREFCA and VDDQ for VREFDQ. VREF(DC) is the linear average of VREF(t) over a very long period of time (e.g. 1 sec) and is specified as a fraction of the linear average of VDDQ or VDD2 also over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirements in Table 3. Furthermore VREF(t) may temporarily deviate from VREF(DC) by no more than ± 1% VDD. VREF(t) cannot track noise on VDDQ or VDD2 if this would send VREF outside these specification.

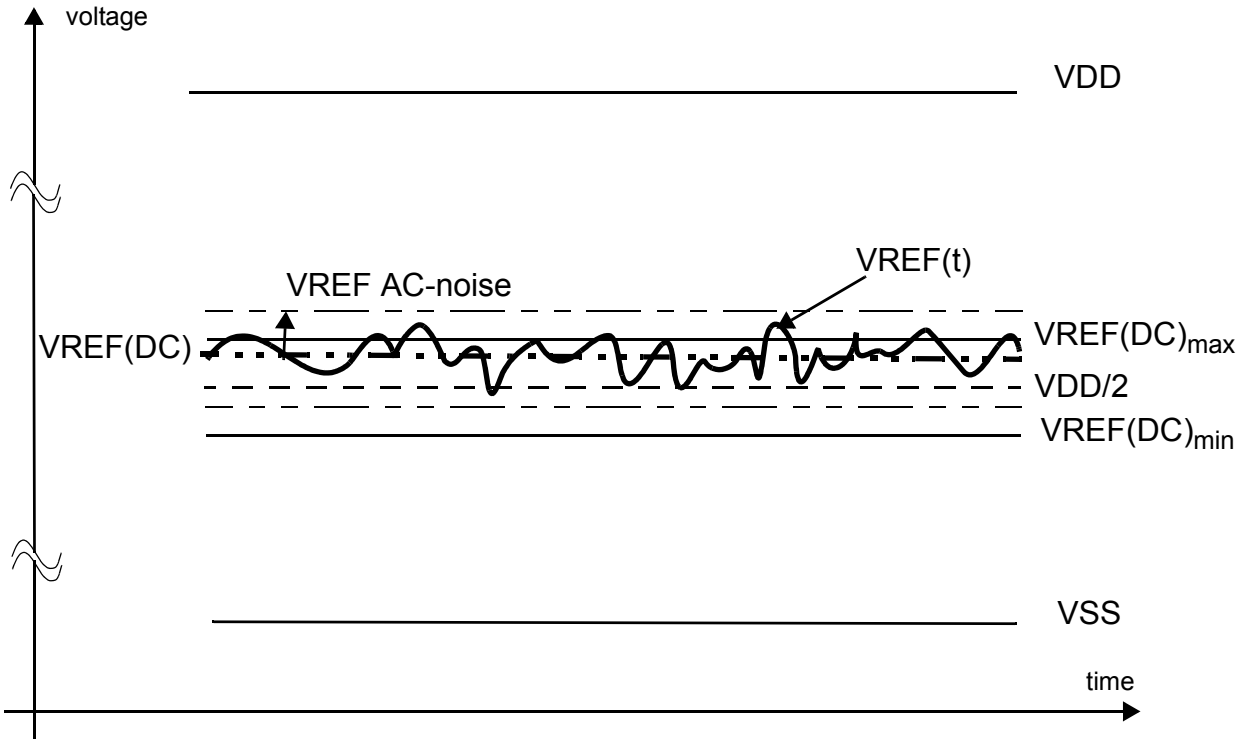


Figure 1 — Illustration of VREF(DC) tolerance and VREF AC-noise limits

The voltage levels for setup and hold time measurements VIH(AC), VIH(DC), VIL(AC) and VIL(DC) are dependent on VREF.

“VREF “ shall be understood as VREF(DC), as defined in Figure 1.

This clarifies that dc-variations of VREF affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. Devices will function correctly with appropriate timing deratings with VREF outside these specified levels so long as VREF is maintained between 0.44 × VDDQ (or VDD2) and 0.56 × VDDQ (or VDD2) and so long as the controller achieves the required single-ended AC and DC input levels from instantaneous VREF (see the “Single-Ended AC and DC Input Levels for CA and /CS Inputs” on page 5 and “Single-Ended AC and DC Input Levels for DQ and DM” on page 5.) Therefore, system timing and voltage budgets need to account for VREF deviations outside of this range.

This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with VREF AC-noise. Timing and voltage effects due to AC-noise on VREF up to the specified limit (± 1% of VDD) are included in DRAM timings and their associated deratings.

1.5 Input Signal

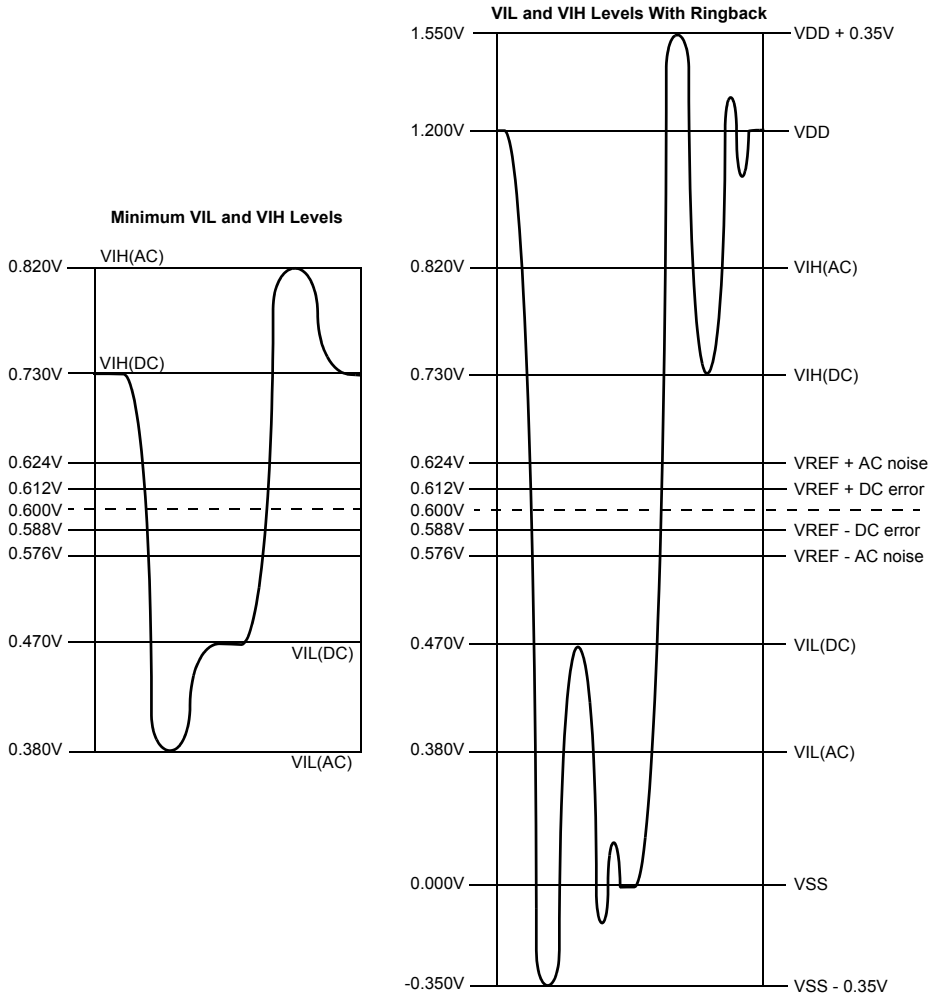


Figure 2 — DDR2 Mobile RAM-533 to DDR2 Mobile RAM-1066 Input Signal

Notes: 1. Numbers reflect nominal values.
2. For CA0 – CA9, CK, /CK and /CS, VDD stands for VDD2. For DQ, DM, DQS, and /DQS, VDD stands for VDDQ.
3. For CA0 – CA9, CK, /CK and /CS, VSS stands for VSS. For DQ, DM, DQS, and /DQS, VSS stands for VSSQ.

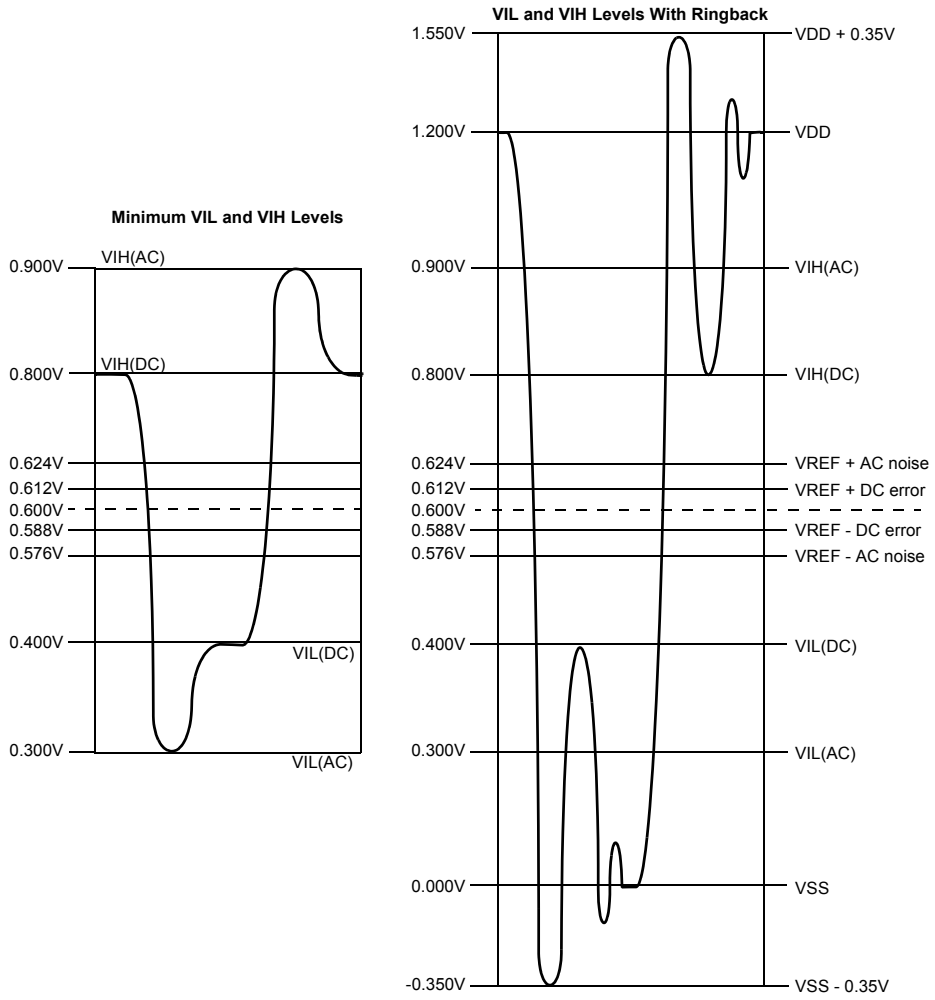


Figure 3 — DDR2 Mobile RAM-400 Input Signal

Notes: 1. Numbers reflect nominal values.
2. For CA0 – CA9, CK, /CK and /CS, VDD stands for VDD2. For DQ, DM, DQS, and /DQS, VDD stands for VDDQ.
3. For CA0 – CA9, CK, /CK and /CS, VSS stands for VSS. For DQ, DM, DQS, and /DQS, VSS stands for VSSQ.

1.6 AC and DC Logic Input Levels for Differential Signals

1.6.1 Differential signal definition

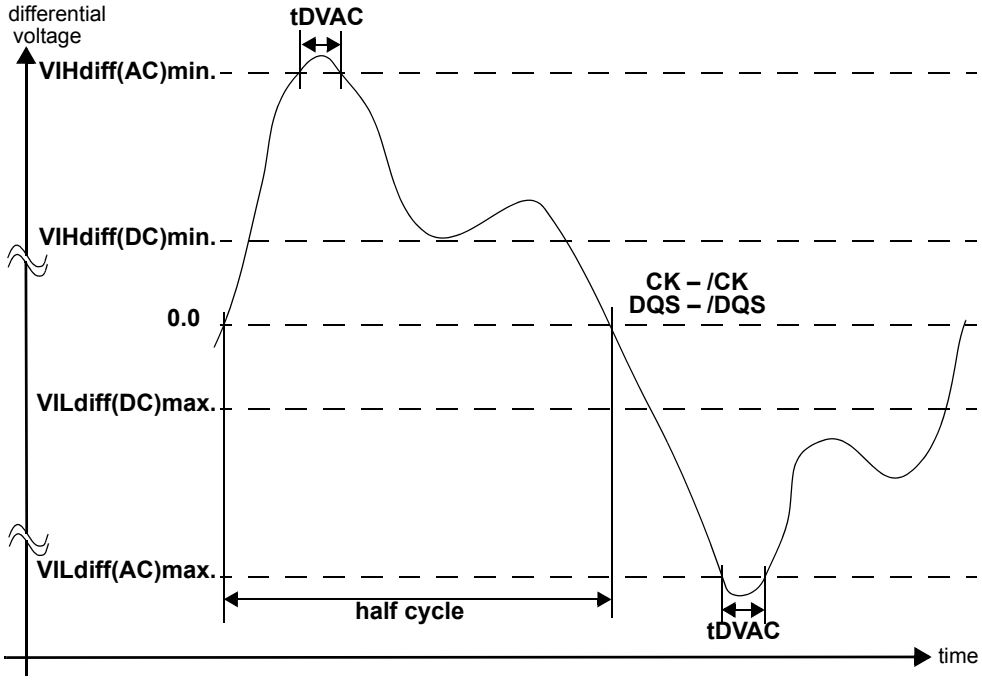


Figure 4 — Definition of differential ac-swing and "time above AC-level" tDVAC

1.6.2 Differential swing requirements for clock (CK – /CK) and strobe (DQS – /DQS)

Table 6 Differential AC and DC Input Levels

Parameter	Symbol	min.	max.	Unit	Note
Differential input high	VIHdiff(DC)	2 × (VIH(DC) - VREF)	Note 3	V	1
Differential input low	VILdiff(DC)	Note 3	2 × (VIL(DC) - VREF)	V	1
Differential input high AC	VIHdiff(AC)	2 × (VIH(AC) - VREF)	Note 3	V	2
Differential input low AC	VILdiff(AC)	Note 3	2 × (VIL(AC) - VREF)	V	2

Notes: 1. Used to define a differential signal slew-rate.
2. For CK – /CK use VIH/VIL(AC) of CA and VREFCA; for DQS – /DQS, use VIH/VIL(AC) of DQs and VREFDQ; if a reduced AC-high or AC-low level is used for a signal group, then the reduced level applies also here.
3. These values are not defined, however the single-ended signals CK, /CK, DQS, and /DQS need to be within the respective limits (VIH(DC) max, VIL(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to "Overshoot and Undershoot Specifications" on page 17.
4. For CK and /CK, VREF = VREFCA(DC). For DQS and /DQS, VREF = VREFDQ(DC).

Table 7 Allowed time before ringback (tDVAC) for CK – /CK and DQS – /DQS

Slew Rate [V/ns]	tDVAC [ps] @ |VIH/Ldiff(AC)| = 440mV	tDVAC [ps] @ |VIH/Ldiff(AC)| = 600mV
	min.	min.
> 4.0	175	75
4.0	170	57
3.0	167	50
2.0	163	38
1.8	162	34
1.6	161	29
1.4	159	22
1.2	155	13
1.0	150	0
< 1.0	150	0

1.6.3 Single-ended requirements for differential signals

Each individual component of a differential signal (CK, DQS, /CK, or /DQS) has also to comply with certain requirements for single-ended signals.

CK and /CK shall meet VSEH(AC)min / VSEL(AC)max in every half-cycle.

DQS, /DQS shall meet VSEH(AC)min / VSEL(AC)max in every half-cycle preceeding and following a valid transition.

Note that the applicable AC-levels for CA and DQ's are different per speed-bin.

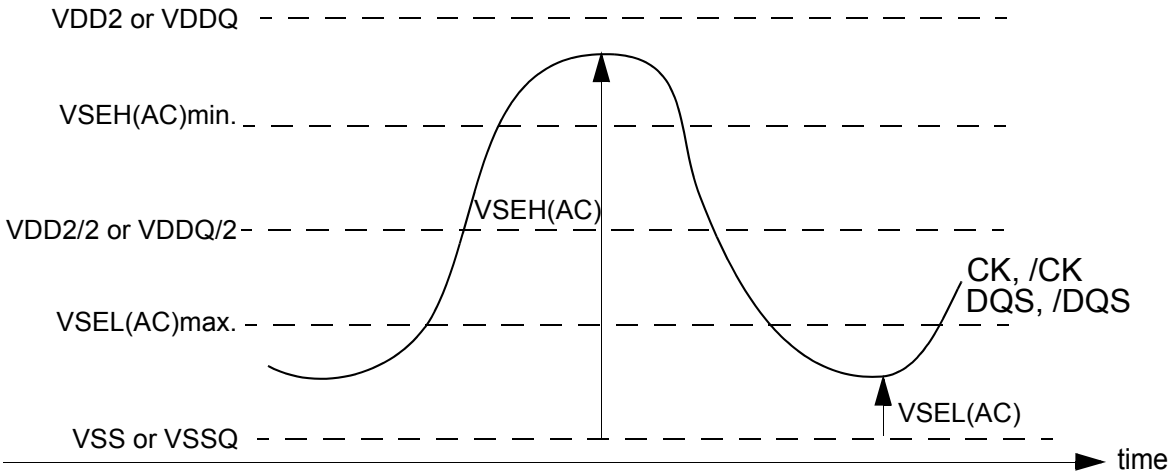


Figure 5 — Single-ended requirement for differential signals.

Note that while CA and DQ signal requirements are with respect to VREF, the single-ended components of differential signals have a requirement with respect to VDDQ/2 for DQS, /DQS and VDD2/2 for CK, /CK; this is nominally the same. The transition of single-ended signals through the AC-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach VSEL(AC)max, VSEH(AC)min has no bearing on timing, but adds a restriction on the common mode charateristics of these signals.

The signal ended requirements for CK, /CK, DQS and /DQS are found in tables 3 and 5, respectively.

Table 8 Single-ended levels for CK, DQS, /CK, /DQS

Parameter	Symbol	Speed	min.	max.	Unit	Note
Single-ended high-level for strobes	VSEH(AC)	533 to 1066	(VDDQ / 2) + 0.220	Note 3	V	1, 2
		400	(VDDQ / 2) + 0.300			
Single-ended high-level for CK, /CK		533 to 1066	(VDD2 / 2) + 0.220	Note 3	V	1, 2
		400	(VDD2 / 2) + 0.300			
Single-ended low-level for strobes	VSEL(AC)	533 to 1066	Note 3	(VDDQ / 2) - 0.220	V	1, 2
		400		(VDDQ / 2) - 0.300		
Single-ended low-level for CK, /CK		533 to 1066	Note 3	(VDD2 / 2) - 0.220	V	1, 2
		400		(VDD2 / 2) - 0.300		

Notes: 1. For CK, /CK use VSEH/VSEL(AC) of CA; for strobes (DQS0, /DQS0, DQS1, /DQS1, DQS2, /DQS2, DQS3, /DQS3) use VIH/VIL(AC) of DQs.

2. VIH(AC)/VIL(AC) for DQs is based on VREFDQ; VSEH(AC)/VSEL(AC) for CA is based on VREFCA; if a reduced AC-high or AC-low level is used for a signal group, then the reduced level applies also here

3. These values are not defined, however the single-ended signals CK, /CK, DQS0, /DQS0, DQS1, /DQS1, DQS2, /DQS2, DQS3, /DQS3 need to be within the respective limits (VIH(DC) max, VIL(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to "Overshoot and Undershoot Specifications" on page 17.

1.7 Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK, /CK and DQS, /DQS) must meet the requirements in Table 8. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signals to the midlevel between of VDD and VSS.

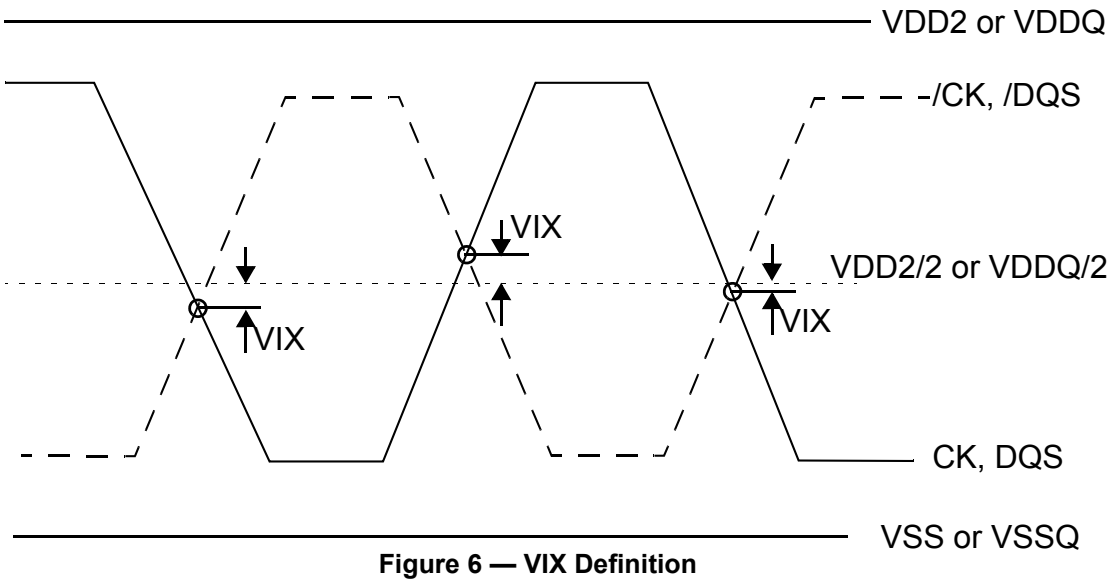


Figure 6 — VIX Definition

Table 9 Cross point voltage for differential input signals (CK, DQS)

Parameter	Symbol	min.	max.	Unit	Note
Differential Input Cross Point Voltage relative to VDD2/2 for CK, /CK	VIXCA	-120	120	mV	1, 2
Differential Input Cross Point Voltage relative to VDDQ/2 for DQS, /DQS	VIXDQ	-120	120	mV	1, 2

Notes: 1. The typical value of VIX(AC) is expected to be about 0.5 × VDD of the transmitting device, and VIX(AC) is expected to track variations in VDD. VIX(AC) indicates the voltage at which differential input signals must cross.
2. For CK and /CK, VREF = VREFCA(DC). For DQS and /DQS, VREF = VREFDQ(DC).

1.8 Slew Rate Definitions for Single-Ended Input Signals

See “CA and /CS Setup, Hold and Derating” on page 37 for single-ended slew rate definitions for address and command signals.

See “Data Setup, Hold and Slew Rate Derating” on page 44 for single-ended slew rate definitions for data signals.

1.9 Slew Rate Definitions for Differential Input Signals

Input slew rate for differential signals (CK, /CK and DQS, /DQS) are defined and measured as shown in Table 10 and Figure 7.

Table 10 Differential Input Slew Rate Definition

Description	Measured		Defined by
	from	to	
Differential input slew rate for rising edge (CK – /CK and DQS – /DQS).	VILdiffmax	VIHdiffmin	[VIHdiffmin - VILdiffmax] / DeltaTRdiff
Differential input slew rate for falling edge (CK – /CK and DQS – /DQS).	VIHdiffmin	VILdiffmax	[VIHdiffmin - VILdiffmax] / DeltaTFdiff

Note: 1. The differential signal (i.e. CK – /CK and DQS – /DQS) must be linear between these thresholds.

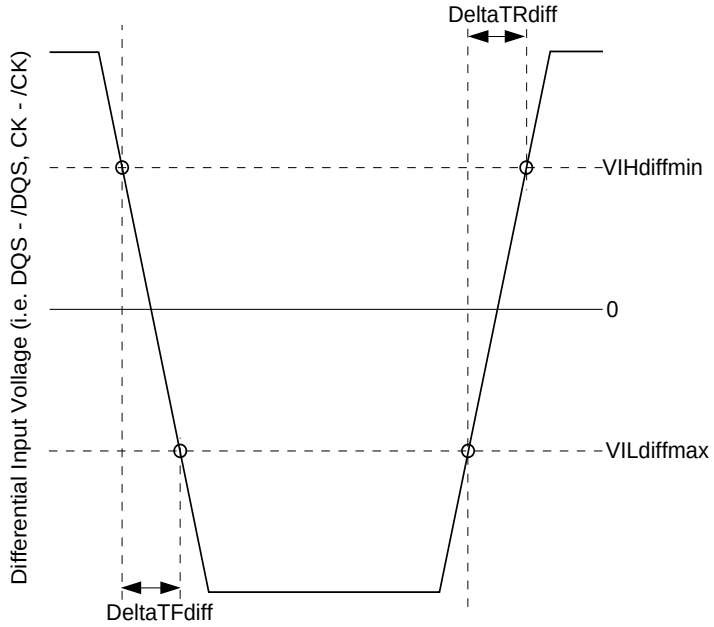


Figure 7 — Differential Input Slew Rate Definition for DQS, /DQS and CK, /CK

1.10 AC and DC Output Measurement Levels

1.10.1 Single Ended AC and DC Output Levels

Table 11 shows the output levels used for measurements of single ended signals.

Table 11 Single-ended AC and DC Output Levels

Parameter	Symbol		Value	Unit	Note
DC output high measurement level (for IV curve linearity)	VOH(DC)		0.9 × VDDQ	V	1
DC output low measurement level (for IV curve linearity)	VOL(DC)		0.1 × VDDQ	V	2
AC output high measurement level (for output slew rate)	VOH(AC)		VREFDQ + 0.12	V	
AC output low measurement level (for output slew rate)	VOL(AC)		VREFDQ - 0.12	V	
Output Leakage current (DQ, DM, DQS, /DQS) (DQ, DQS, /DQS are disabled; 0V ≤ VOUT ≤ VDDQ)	IOZ	min.	-5	µA	
		max.	5	µA	
Delta RON between pull-up and pull-down for DQ/DM	MMPUPD	min.	-15	%	
		max.	15	%	

Notes: 1. IOH = -0.1mA.
2. IOL = 0.1mA.

1.10.2 Differential AC and DC Output Levels

Table 12 shows the output levels used for measurements of differential signals.

Table 12 Differential AC and DC Output Levels

Parameter	Symbol	Value	Unit	Note
AC differential output high measurement level (for output SR)	VOHdiff(AC)	+0.2 × VDDQ	V	
AC differential output low measurement level (for output SR)	VOLdiff(AC)	-0.2 × VDDQ	V	

1.10.3 Single Ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC) for single ended signals as shown in Table 13 and Figure 8.

Table 13 Single-ended Output Slew Rate Definition

Description	Measured		Defined by
	from	to	
Single-ended output slew rate for rising edge	VOL(AC)	VOH(AC)	[VOH(AC) - VOL(AC)] / DeltaTRse
Single-ended output slew rate for falling edge	VOH(AC)	VOL(AC)	[VOH(AC) - VOL(AC)] / DeltaTFse

Note: 1. Output slew rate is verified by design and characterization, and may not be subject to production test.

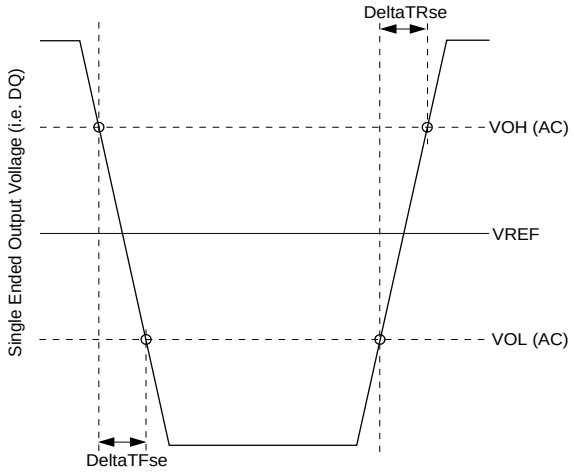


Figure 8 — Single Ended Output Slew Rate Definition

Table 14 Output Slew Rate (single-ended)

Parameter	Symbol	min.	max.	Unit
Single-ended Output Slew Rate (RON = 40Ω ± 30%)	SRQse	1.5	3.5	V/ns
Single-ended Output Slew Rate (RON = 60Ω ± 30%)	SRQse	1.0	2.5	V/ns
Output slew-rate matching Ratio (Pull-up to Pull-down)		0.7	1.4	

Remark: SR: Slew Rate, Q: Query Output (like in DQ, which stands for Data-in, Query-Output), se: Single-ended Signals

Notes: 1. Measured with output reference load.
2. The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pulldown drivers due to process variation.
3. The output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC).
4. Slew rates are measured under normal SSO conditions, with 1/2 of DQ signals per data byte driving logic high and 1/2 of DQ signals per data byte driving logic low.

1.11 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOLdiff(AC) and VOHdiff(AC) for differential signals as shown in Table 15 and Figure 9.

Table 15 Differential Output Slew Rate Definition

Description	Measured		Defined by
	from	to	
Differential output slew rate for rising edge	VOLdiff(AC)	VOHdiff(AC)	[VOHdiff(AC) - VOLdiff(AC)] / DeltaTRdiff
Differential output slew rate for falling edge	VOHdiff(AC)	VOLdiff(AC)	[VOHdiff(AC) - VOLdiff(AC)] / DeltaTFdiff

Note: 1. Output slew rate is verified by design and characterization, and may not be subject to production test.

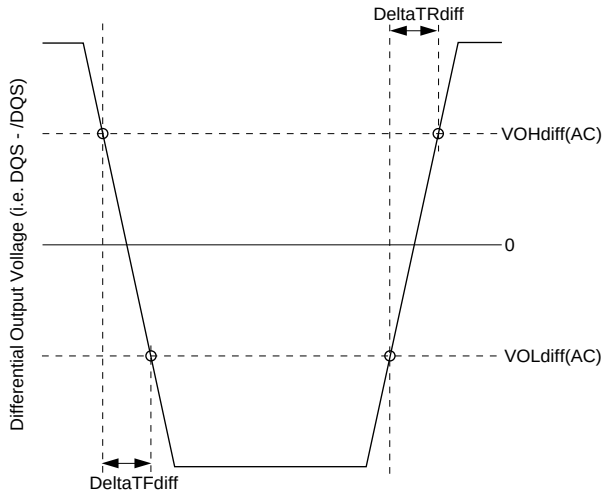


Figure 9 — Differential Output Slew Rate Definition

Table 16 Differential Output Slew Rate

Parameter	Symbol	min.	max.	Unit
Differential Output Slew Rate (RON = 40Ω ± 30%)	SRQdiff	3.0	7.0	V/ns
Differential Output Slew Rate (RON = 60Ω ± 30%)	SRQdiff	2.0	5.0	V/ns

Remark: SR: Slew Rate, Q: Query Output (like in DQ, which stands for Data-in, Query-Output), diff: Differential Signals

Notes: 1. Measured with output reference load.
2. The output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC).
3. Slew rates are measured under normal SSO conditions, with 1/2 of DQ signals per data byte driving logic high and 1/2 of DQ signals per data byte driving logic low.

1.12 Overshoot and Undershoot Specifications

Table 17 AC Overshoot/Undershoot Specification

Parameter		1066	800	667	533	400	Unit
Maximum peak amplitude allowed for overshoot area.	max.	0.35					V
Maximum peak amplitude allowed for undershoot area.	max.	0.35					V
Maximum overshoot area above VDD[*1].	max.	0.15	0.20	0.24	0.30	0.40	V-ns
Maximum undershoot area below VSS[*2]	max.	0.15	0.20	0.24	0.30	0.40	V-ns

Notes: 1. For CA0 – CA9, CK, /CK, /CS, and CKE, VDD stands for VDD2. For DQ, DM, DQS, and /DQS, VDD stands for VDDQ.
2. For CA0 – CA9, CK, /CK, /CS, and CKE, VSS stands for VSS. For DQ, DM, DQS, and /DQS, VSS stands for VSSQ.
3. Values are referenced from actual VDDQ, VDD2, VSSQ, and VSS levels.

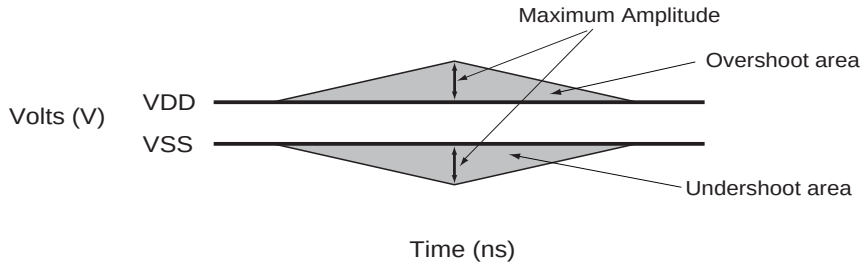


Figure 10 — Overshoot and Undershoot Definition

1.13 RONPU and RONPD Resistor Definition

$$RONPU = \frac{(VDDQ - Vout)}{ABS(Iout)}$$

Note 1: This is under the condition that RONPD is turned off

$$RONPD = \frac{Vout}{ABS(Iout)}$$

Note 1: This is under the condition that RONPU is turned off

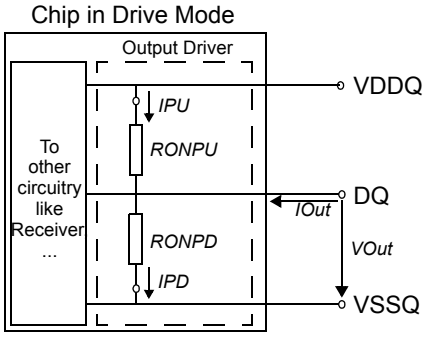


Figure 11 — Output Driver: Definition of Voltages and Currents

1.13.1 RONPU and RONPD Characteristics with ZQ Calibration

Output driver impedance RON is defined by the value of the external reference resistor RZQ. Nominal RZQ is 240Ω.

Table 18 Output Driver DC Electrical Characteristics with ZQ Calibration

RONNOM	Resistor	Vout	min.	nom.	max.	Unit	Note
34.3Ω	RON34PD	0.5 × VDDQ	0.85	1.00	1.15	RZQ/7	1, 2, 3, 4
	RON34PU	0.5 × VDDQ	0.85	1.00	1.15	RZQ/7	1, 2, 3, 4
40.0Ω	RON40PD	0.5 × VDDQ	0.85	1.00	1.15	RZQ/6	1, 2, 3, 4
	RON40PU	0.5 × VDDQ	0.85	1.00	1.15	RZQ/6	1, 2, 3, 4
48.0Ω	RON48PD	0.5 × VDDQ	0.85	1.00	1.15	RZQ/5	1, 2, 3, 4
	RON48PU	0.5 × VDDQ	0.85	1.00	1.15	RZQ/5	1, 2, 3, 4
60.0Ω	RON60PD	0.5 × VDDQ	0.85	1.00	1.15	RZQ/4	1, 2, 3, 4
	RON60PU	0.5 × VDDQ	0.85	1.00	1.15	RZQ/4	1, 2, 3, 4
80.0Ω	RON80PD	0.5 × VDDQ	0.85	1.00	1.15	RZQ/3	1, 2, 3, 4
	RON80PU	0.5 × VDDQ	0.85	1.00	1.15	RZQ/3	1, 2, 3, 4
120.0Ω (optional)	RON120PD	0.5 × VDDQ	0.85	1.00	1.15	RZQ/2	1, 2, 3, 4
	RON120PU	0.5 × VDDQ	0.85	1.00	1.15	RZQ/2	1, 2, 3, 4
Mismatch between pull-up and pull-down	MMPUPD		-15.00		+15.00	%	1, 2, 3, 4, 5

Notes: 1. Across entire operating temperature range, after calibration.
2. RZQ = 240Ω.
3. The tolerance limits are specified after calibration with fixed voltage and temperature. For behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
4. Pull-down and pull-up output driver impedances are recommended to be calibrated at 0.5 × VDDQ.
5. Mesaurement definition for mismatch between pull-up and pull-down, MMPUPD: Measure RONPU and RONPD, both at 0.5 × VDDQ:

$$\text{MMPUPD} = \frac{\text{RONPU} - \text{RONPD}}{\text{RONNOM}} \times 100$$

For example, with MMPUPD max.= 15% and RONPD = 0.85, RONPU must be less than 1.0.

1.13.2 Output Driver Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to the Tables shown below.

Table 19 Output Driver Sensitivity Definition

Resistor	Vout	min.	max.	Unit	Note
RONPD	0.5 × VDDQ	85 - (dRONdT × |ΔT|) - (dRONdV × |ΔV|)	115 + (dRONdT × |ΔT|) + (dRONdV × |ΔV|)	%	1, 2
RONPU					

Notes: 1. ΔT = T - T(@ calibration), ΔV = V - V(@ calibration)
2. dRONdT and dRONdV are not subject to production test but are verified by design and characterization

Table 20 Output Driver Temperature and Voltage Sensitivity

Parameter	Symbol	min.	max.	Unit	Note
RON Temperature Sensitivity	dRONdT	0	0.75	%/°C	
RON Voltage Sensitivity	dRONdV	0	0.20	%/mV	

1.13.3 RONPU and RONPD Characteristics without ZQ Calibration

Output driver impedance RON is defined by design and characterization as default setting.

Table 21 Output Driver DC Electrical Characteristics without ZQ Calibration

RONNOM	Resistor	Vout	min.	nom.	max.	Unit	Note
34.3Ω	RON34PD	0.5 × VDDQ	24	34.3	44.6	Ω	1
	RON34PU	0.5 × VDDQ	24	34.3	44.6	Ω	1
40.0Ω	RON40PD	0.5 × VDDQ	28	40	52	Ω	1
	RON40PU	0.5 × VDDQ	28	40	52	Ω	1
48.0Ω	RON48PD	0.5 × VDDQ	33.6	48	62.4	Ω	1
	RON48PU	0.5 × VDDQ	33.6	48	62.4	Ω	1
60.0Ω	RON60PD	0.5 × VDDQ	42	60	78	Ω	1
	RON60PU	0.5 × VDDQ	42	60	78	Ω	1
80.0Ω	RON80PD	0.5 × VDDQ	56	80	104	Ω	1
	RON80PU	0.5 × VDDQ	56	80	104	Ω	1
120.0Ω (optional)	RON120PD	0.5 × VDDQ	84	120	156	Ω	1
	RON120PU	0.5 × VDDQ	84	120	156	Ω	1

Note: 1. Across entire operating temperature range, without calibration.

2. Electrical Specifications

2.1 IDD Measurement Conditions

The following definitions are used within the IDD measurement tables:

LOW: VIN ≤ VIL(DC) max.

HIGH: VIN ≥ VIH(DC) min.

STABLE: Inputs are stable at a HIGH or LOW level

SWITCHING: See Table 22, 23 and 24.

Table 22 Definition of Switching for CA Input Signals

Switching for CA								
	CK (RISING) / /CK (FALLING)	CK (FALLING) / /CK (RISING)	CK (RISING) / /CK (FALLING)	CK (FALLING) / /CK (RISING)	CK (RISING) / /CK (FALLING)	CK (FALLING) / /CK (RISING)	CK (RISING) / /CK (FALLING)	CK (FALLING) / /CK (RISING)
Cycle	N		N + 1		N + 2		N + 3	
/CS	HIGH		HIGH		HIGH		HIGH	
CA0	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA1	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA2	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA3	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA4	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA5	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA6	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA7	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA8	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA9	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH

Notes: 1. /CS must always be driven HIGH.
2. 50% of CA bus is changing between HIGH and LOW once per clock for the CA bus.
3. The above pattern (N, N + 1, N + 2, N + 3...) is used continuously during IDD measurement for IDD values that require SWITCHING on the CA bus.

Table 23 Definition of Switching for IDD4R

Clock	CKE	/CS	Clock Cycle Number	Command	CA0 – CA2	CA3 – CA9	All DQ
Rising	HIGH	LOW	N	Read_Rising	HLH	LHLHLHL	L
Falling	HIGH	LOW	N	Read_Falling	LLL	LLLLLLL	L
Rising	HIGH	HIGH	N + 1	NOP	LLL	LLLLLLL	H
Falling	HIGH	HIGH	N + 1	NOP	HLH	HLHLLHL	L
Rising	HIGH	LOW	N + 2	Read_Rising	HLH	HLHLLHL	H
Falling	HIGH	LOW	N + 2	Read_Falling	LLL	HHHHHHH	H
Rising	HIGH	HIGH	N + 3	NOP	LLL	HHHHHHH	H
Falling	HIGH	HIGH	N + 3	NOP	HLH	LHLHLHL	L

Notes: 1. Data strobe (DQS) is changing between HIGH and LOW every clock cycle.
2. The above pattern (N, N + 1...) is used continuously during IDD measurement for IDD4R.

Table 24 Definition of Switching for IDD4W

Clock	CKE	/CS	Clock Cycle Number	Command	CA0 – CA2	CA3 – CA9	All DQ
Rising	HIGH	LOW	N	Write_Rising	HLL	LHLHLHL	L
Falling	HIGH	LOW	N	Write_Falling	LLL	LLLLLLL	L
Rising	HIGH	HIGH	N + 1	NOP	LLL	LLLLLLL	H
Falling	HIGH	HIGH	N + 1	NOP	HLH	HLHLLHL	L
Rising	HIGH	LOW	N + 2	Write_Rising	HLL	HLHLLHL	H
Falling	HIGH	LOW	N + 2	Write_Falling	LLL	HHHHHHH	H
Rising	HIGH	HIGH	N + 3	NOP	LLL	HHHHHHH	H
Falling	HIGH	HIGH	N + 3	NOP	HLH	LHLHLHL	L

Notes: 1. Data strobe (DQS) is changing between HIGH and LOW every clock cycle.
2. Data masking (DM) must always be driven LOW.
3. The above pattern (N, N + 1...) is used continuously during IDD measurement for IDD4W.

2.2 DC Characteristics 1

(TJ = -30°C to +85°C, VDD1 = 1.70V to 1.95V, VDD2, VDDQ = 1.14V to 1.30V)

Table 25 IDD Specification Parameters and Operating Conditions

Symbol	Power Supply	1066	800	667	533	400	Unit	Parameter/Condition
		max.	max.	max.	max.	max.		
IDD0_1	VDD1	12	12	12	12	12	mA	**Operating one bank active-pecharge current:** tCK = tCK(avg)min; tRC = tRCmin; CKE is HIGH; /CS is HIGH between valid commands; CA bus inputs are SWITCHING; Data bus inputs are STABLE
IDD0_2	VDD2	60	60	60	60	60	mA	
IDD0_IN	VDDQ	1.0	1.0	1.0	1.0	1.0	mA	
IDD2P_1	VDD1	1.2	1.2	1.2	1.2	1.2	mA	**Idle power-down standby current:** tCK = tCK(avg)min; CKE is LOW; /CS is HIGH; All banks idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE
IDD2P_2	VDD2	2.0	2.0	2.0	2.0	2.0	mA	
IDD2P_IN	VDDQ	0.1	0.1	0.1	0.1	0.1	mA	
IDD2PS_1	VDD1	1.2	1.2	1.2	1.2	1.2	mA	**Idle power-down standby current with clock stop:** CK = LOW, /CK = HIGH; CKE is LOW; /CS is HIGH; All banks idle; CA bus inputs are STABLE; Data bus inputs are STABLE
IDD2PS_2	VDD2	0.8	0.8	0.8	0.8	0.8	mA	
IDD2PS_IN	VDDQ	0.1	0.1	0.1	0.1	0.1	mA	
IDD2N_1	VDD1	1.5	1.5	1.5	1.5	1.5	mA	**Idle non power-down standby current:** tCK = tCK(avg)min; CKE is HIGH; /CS is HIGH; All banks idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE
IDD2N_2	VDD2	28	28	24	20	16	mA	
IDD2N_IN	VDDQ	1.0	1.0	1.0	1.0	1.0	mA	
IDD2NS_1	VDD1	1.4	1.4	1.4	1.4	1.4	mA	**Idle non power-down standby current with clock stop:** CK = LOW, /CK = HIGH; CKE is HIGH; /CS is HIGH; All banks idle; CA bus inputs are STABLE; Data bus inputs are STABLE
IDD2NS_2	VDD2	9.0	9.0	9.0	9.0	9.0	mA	
IDD2NS_IN	VDDQ	1.0	1.0	1.0	1.0	1.0	mA	
IDD3P_1	VDD1	2.6	2.6	2.6	2.6	2.6	mA	**Active power-down standby current:** tCK = tCK(avg)min; CKE is LOW; /CS is HIGH; One bank active; CA bus inputs are SWITCHING; Data bus inputs are STABLE
IDD3P_2	VDD2	3.2	3.0	2.8	2.6	2.4	mA	
IDD3P_IN	VDDQ	0.5	0.5	0.5	0.5	0.5	mA	
IDD3PS_1	VDD1	2.2	2.2	2.2	2.2	2.2	mA	**Active power-down standby current with clock stop:** CK = LOW, /CK = HIGH; CKE is LOW; /CS is HIGH; One bank active; CA bus inputs are STABLE; Data bus inputs are STABLE
IDD3PS_2	VDD2	2.7	2.7	2.7	2.7	2.7	mA	
IDD3PS_IN	VDDQ	0.5	0.5	0.5	0.5	0.5	mA	
IDD3N_1	VDD1	4.5	4.5	4.5	4.5	4.5	mA	**Active non power-down standby current:** tCK = tCK(avg)min; CKE is HIGH; /CS is HIGH; One bank active; CA bus inputs are SWITCHING; Data bus inputs are STABLE
IDD3N_2	VDD2	32	30	26	22	18	mA	
IDD3N_IN	VDDQ	1.0	1.0	1.0	1.0	1.0	mA	
IDD3NS_1	VDD1	4.0	4.0	4.0	4.0	4.0	mA	**Active non power-down standby current with clock stop:** CK = LOW, /CK = HIGH; CKE is HIGH; /CS is HIGH; One bank active; CA bus inputs are STABLE; Data bus inputs are STABLE
IDD3NS_2	VDD2	11	11	11	11	11	mA	
IDD3NS_IN	VDDQ	1.0	1.0	1.0	1.0	1.0	mA	

Table 25 IDD Specification Parameters and Operating Conditions (cont'd)

Symbol	Power Supply	1066	800	667	533	400	Unit	Parameter/Condition
		max.	max.	max.	max.	max.		
IDD4R_1	VDD1	5.0	5.0	4.5	4.0	3.5	mA	**Operating burst read current:** tCK = tCK(avg)min; /CS is HIGH between valid commands; One bank active; BL = 4; RL = RLmin; CA bus inputs are SWITCHING; 50% data change each burst transfer; Values in parenthesis are for x16 bits;
IDD4R_2	VDD2	150 (120)	120 (110)	110 (100)	100 (90)	90 (80)	mA	
IDD4W_1	VDD1	5.0	5.0	5.0	5.0	5.0	mA	**Operating burst write current:** tCK = tCK(avg)min; /CS is HIGH between valid commands; One bank active; BL = 4; WL = WLmin; CA bus inputs are SWITCHING; 50% data change each burst transfer; Values in parenthesis are for x16 bits;
IDD4W_2	VDD2	170 (130)	130 (110)	120 (100)	110 (90)	100 (80)	mA	
IDD4W_IN	VDDQ	1.0	1.0	1.0	1.0	1.0	mA	
IDD5_1	VDD1	28	28	28	28	28	mA	**All Bank Auto Refresh Burst current:** tCK = tCK(avg)min; CKE is HIGH between valid commands; tRC = tRFCabmin; Burst refresh; CA bus inputs are SWITCHING; Data bus inputs are STABLE;
IDD5_2	VDD2	120	120	120	120	120	mA	
IDD5_IN	VDDQ	1.0	1.0	1.0	1.0	1.0	mA	
IDD5AB_1	VDD1	2.0	2.0	2.0	2.0	2.0	mA	**All Bank Auto Refresh Average current:** tCK = tCK(avg)min; CKE is HIGH between valid commands; tRC = tREFI; CA bus inputs are SWITCHING; Data bus inputs are STABLE;
IDD5AB_2	VDD2	30	30	26	22	18	mA	
IDD5AB_IN	VDDQ	1.0	1.0	1.0	1.0	1.0	mA	
IDD5PB_1	VDD1	2.0	2.0	2.0	2.0	2.0	mA	**Per Bank Auto Refresh Average current:** tCK = tCK(avg)min; CKE is HIGH between valid commands; tRC = tREFI/8; CA bus inputs are SWITCHING; Data bus inputs are STABLE;
IDD5PB_2	VDD2	30	30	26	22	18	mA	
IDD5PB_IN	VDDQ	1.0	1.0	1.0	1.0	1.0	mA	
IDD8_1	VDD1	8.0	8.0	8.0	8.0	8.0	µA	**Deep Power-Down current:** CK = LOW, /CK = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE;
IDD8_2	VDD2	3.0	3.0	3.0	3.0	3.0	µA	
IDD8_IN	VDDQ	6.0	6.0	6.0	6.0	6.0	µA	

Notes: 1. IDD values published are the maximum of the distribution of the arithmetic mean.
2. IDD current specifications are tested after the device is properly initialized.

Table 26 IDD6 Full and Partial Array Self-Refresh Current

Parameter		Symbol	typ.	max.	Unit	Condition
Self-Refresh Current -30°C ≤ TJ ≤ +45°C	Full Array	IDD6_1	—	500	µA	CK = LOW, /CK = HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE;
		IDD6_2	—	450	µA	
		IDD6_IN	—	10	µA	
	1/2 Array	IDD6_1	—	330	µA	
		IDD6_2	—	300	µA	
		IDD6_IN	—	10	µA	
	1/4 Array	IDD6_1	—	280	µA	
		IDD6_2	—	210	µA	
		IDD6_IN	—	10	µA	
	1/8 Array	IDD6_1	—	250	µA	
		IDD6_2	—	180	µA	
		IDD6_IN	—	10	µA	
Self-Refresh Current +45°C < TJ ≤ +85°C	Full Array	IDD6_1	—	1200	µA	
		IDD6_2	—	900	µA	
		IDD6_IN	—	10	µA	
	1/2 Array	IDD6_1	—	900	µA	
		IDD6_2	—	600	µA	
		IDD6_IN	—	10	µA	
	1/4 Array	IDD6_1	—	630	µA	
		IDD6_2	—	450	µA	
		IDD6_IN	—	10	µA	
	1/8 Array	IDD6_1	—	500	µA	
		IDD6_2	—	350	µA	
		IDD6_IN	—	10	µA	

Note: 1. IDD values published are the maximum of the distribution of the arithmetic mean.

2.3 DC Characteristics 2

(TJ = -30°C to +85°C, VDD1 = 1.70V to 1.95V, VDD2, VDDQ = 1.14V to 1.30V)

Table 27 Electrical Characteristics and Operating Conditions

Symbol	min.	max.	Unit	Parameter/Condition	Note
IL	-2	+2	µA	**Input leakage current:** For CA, CKE, /CS, CK, /CK Any input 0V ≤ VIN ≤ VDD2 (All other pins not under test = 0V)	2
IVREF	-1	+1	µA	**VREF supply leakage current:** VREFDQ = VDDQ/2 or VREFCA = VDD2/2 (All other pins not under test = 0V)	1

Notes: 1. The minimum limit requirement is for testing purposes. The leakage current on VREFCA and VREFDQ pins should be minimal.

2. Although DM is for input only, the DM leakage shall match the DQ and DQS, /DQS output leakage specification.

2.4 Pin Capacitance

(TA = +25°C, VDD1 = 1.70V to 1.95V, VDD2, VDDCA, VDDQ = 1.14V to 1.30V)

Table 28 Input/output capacitance

Parameter	Symbol	min.	max.	Unit	Note
Input capacitance, CK and /CK	CCK	1.0	2.0	pF	1, 2
Input capacitance delta, CK and /CK	CDCK	0	0.2	pF	1, 2, 3
Input capacitance, all other input-only pins	CI	1.0	2.0	pF	1, 2, 4
Input capacitance delta, all other input-only pins	CDI	-0.4	0.4	pF	1, 2, 5
Input/output capacitance, DQ, DM, DQS, /DQS	CIO	1.25	2.5	pF	1, 2, 6, 7
Input/output capacitance delta, DQS, /DQS	CDDQS	0	0.25	pF	1, 2, 7, 8
Input/output capacitance delta, DQ, DM	CDIO	-0.5	0.5	pF	1, 2, 7, 9
Input/output capacitance ZQ Pin	CZQ	0	2.5	pF	1, 2

Notes: 1. This parameter applies to die device only (does not include package capacitance).
2. This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA) with VDD1, VDD2, VDDQ, VSS, VSSQ applied and all other pins floating.
3. Absolute value of CCK – C/CK.
4. CI applies to /CS, CKE, CA0 – CA9.
5. CDI = CI - 0.5 × (CCK + C/CK)
6. DM loading matches DQ and DQS.
7. MR3 I/O configuration DS OP3-OP0 = 0001B (34.3 Ω typical)
8. Absolute value of CDQS and C/DQS.
9. CDIO = CIO - 0.5 × (CDQS + C/DQS) in byte-lane.

2.5 Clock Specification

The jitter specified is a random jitter meeting a Gaussian distribution. Input clocks violating the min/max values may result in malfunction of the DDR2 Mobile RAM device.

2.5.1 Definition for tCK(avg) and nCK

tCK(avg) is calculated as the average clock period across any consecutive 200 cycle window, where each clock period is calculated from rising edge to rising edge.

$$tCK(avg) = \left(\sum_{j=1}^{N} tCK_j \right) / N$$

$$where \qquad N = 200$$

Unit 'tCK(avg)' represents the actual clock average tCK(avg) of the input clock under operation. Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges.

tCK(avg) may change by up to +/-1% within a 100 clock cycle window, provided that all jitter and timing specs are met.

2.5.2 Definition for tCK(abs)

tCK(abs) is defined as the absolute clock period, as measured from one rising edge to the next consecutive rising edge. tCK(abs) is not subject to production test.

2.5.3 Definition for tCH(avg) and tCL(avg)

tCH(avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

$$tCH(avg) = \left(\sum_{j=1}^{N} tCH_j \right) / (N \times tCK(avg))$$

$$where \qquad N = 200$$

tCL(avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$tCL(avg) = \left(\sum_{j=1}^{N} tCL_j \right) / (N \times tCK(avg))$$

$$where \qquad N = 200$$

2.5.4 Definition for tJIT(per)

tJIT(per) is the single period jitter defined as the largest deviation of any signal tCK from tCK(avg).
tJIT(per) = Min/max of {tCKi - tCK(avg) where i = 1 to 200}.
tJIT(per),act is the actual clock jitter for a given system.
tJIT(per),allowed is the specified allowed clock period jitter.
tJIT(per) is not subject to production test.

2.5.5 Definition for tJIT(cc)

tJIT(cc) is defined as the absolute difference in clock period between two consecutive clock cycles.
tJIT(cc) = Max of |{tCKi +1 - tCKi}|.
tJIT(cc) defines the cycle to cycle jitter.
tJIT(cc) is not subject to production test.

2.5.6 Definition for tERR(nper)

tERR(nper) is defined as the cumulative error across n multiple consecutive cycles from tCK(avg).
tERR(nper), act is the actual clock jitter over n cycles for a given system.
tERR(nper), allowed is the specified allowed clock period jitter over n cycles.
tERR(nper) is not subject to production test.

$$tERR(nper) = \left(\sum_{j=i}^{i+n-1} tCK_j \right) - n \times tCK(avg)$$

tERR(nper),min can be calculated by the formula shown below:

$$tERR(nper), min = (1 + 0.68LN(n)) \times tJIT(per), min$$

tERR(nper),max can be calculated by the formula shown below:

$$tERR(nper), max = (1 + 0.68LN(n)) \times tJIT(per), max$$

Using these equations, tERR(nper) tables can be generated for each tJIT(per),act value.

2.5.7 Definition for duty cycle jitter tJIT(duty)

tJIT(duty) is defined with absolute and average specification of tCH / tCL.

$$tJIT(duty), min = MIN((tCH(abs), min - tCH(avg), min), (tCL(abs), min - tCL(avg), min)) \times tCK(avg)$$
$$tJIT(duty), max = MAX((tCH(abs), max - tCH(avg), max), (tCL(abs), max - tCL(avg), max)) \times tCK(avg)$$

2.5.8 Definition for tCK(abs), tCH(abs) and tCL(abs)

These parameters are specified per their average values, however it is understood that the following relationship between the average timing and the absolute instantaneous timing holds at all times.

Table 29 Definition for tCK(abs), tCH(abs), and tCL(abs)

Parameter	Symbol	Min	Unit
Absolute Clock Period	tCK(abs)	tCK(avg),min + tJIT(per),min	ps
Absolute Clock HIGH Pulse Width	tCH(abs)	tCH(avg),min + tJIT(duty),min / tCK(avg)min	tCK(avg)
Absolute Clock LOW Pulse Width	tCL(abs)	tCL(avg),min + tJIT(duty),min / tCK(avg)min	tCK(avg)

Notes: 1. tCK(avg),min is expressed is ps for this table.
2. tJIT(duty),min is a negative value.

2.6 Period Clock Jitter

DDR2 Mobile RAM devices can tolerate some clock period jitter without core timing parameter de-rating. This section describes device timing requirements in the presence of clock period jitter (tJIT(per)) in excess of the values found in Table 30 on page 31 and how to determine cycle time de-rating and clock cycle de-rating.

2.6.1 Clock period jitter effects on core timing parameters (tRCD, tRP, tRTP, tWR, tWRA, tWTR, tRC, tRAS, tRRD, tFAW)

Core timing parameters extend across multiple clock cycles. Period clock jitter will impact these parameters when measured in numbers of clock cycles. When the device is operated with clock jitter within the specification limits, the DDR2 Mobile RAM device is characterized and verified to support tnPARAM = RU{tPARAM / tCK(avg)}.

When the device is operated with clock jitter outside specification limits, the number of clocks or tCK(avg) may need to be increased based on the values for each core timing parameter.

2.6.1.1 Cycle time de-rating for core timing parameters

For a given number of clocks (tnPARAM), for each core timing parameter, average clock period (tCK(avg)) and actual cumulative period error (tERR(tnPARAM),act) in excess of the allowed cumulative period error (tERR(tnPARAM),allowed), the equation below calculates the amount of cycle time de-rating (in ns) required if the equation results in a positive value for a core timing parameter (tCORE).

$$CycleTimeDerating = MAX\left\{\left(\frac{tPARAM + tERR(tnPARAM),act - tERR(tnPARAM),allowed}{tnPARAM} - tCK(avg)\right), 0\right\}$$

A cycle time derating analysis should be conducted for each core timing parameter. The amount of cycle time derating required is the maximum of the cycle time de-ratings determined for each individual core timing parameter.

2.6.1.2 Clock Cycle de-rating for core timing parameters

For a given number of clocks (tnPARAM) for each core timing parameter, clock cycle de-rating should be specified with amount of period jitter (tJIT(per)).

For a given number of clocks (tnPARAM), for each core timing parameter, average clock period (tCK(avg)) and actual cumulative period error (tERR(tnPARAM),act) in excess of the allowed cumulative period error (tERR(tnPARAM),allowed), the equation below calculates the clock cycle derating (in clocks) required if the equation results in a positive value for a core timing parameter (tCORE).

$$ClockCycleDerating = RU\left\{\frac{tPARAM + tERR(tnPARAM),act - tERR(tnPARAM),allowed}{tCK(avg)}\right\} - tnPARAM$$

A clock cycle de-rating analysis should be conducted for each core timing parameter.

2.6.2 Clock jitter effects on Command/Address timing parameters (tIS, tIH, tISCKE, tIHCKE, tISb, tIHb, tISCKEb, tIHCKEb)

These parameters are measured from a command/address signal (CKE, CS, CA0 – CA9) transition edge to its respective clock signal (CK, /CK) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), as the setup and hold are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values shall be met.

2.6.3 Clock jitter effects on Read timing parameters

2.6.3.1 tRPRE

When the device is operated with input clock jitter, tRPRE needs to be de-rated by the actual period jitter (tJIT(per),act,max) of the input clock in excess of the period jitter (tJIT(per),allowed,max). Output de-ratings are relative to the input clock.

$$tRPRE(min, derated) = 0.9 - \left(\frac{tJIT(per), act,max - tJIT(per),allowed,max}{tCK(avg)} \right)$$

For example,

if the measured jitter into a DDR2 Mobile RAM-800 device has tCK(avg) = 2500 ps, tJIT(per),act,min = -172 ps and tJIT(per),act,max= + 193 ps, then

tRPRE,min,derated = 0.9 - (tJIT(per),act,max - tJIT(per),allowed,max)/tCK(avg) = 0.9 - (193 - 100)/2500= 0.8628 tCK(avg)

2.6.3.2 tLZ(DQ), tHZ(DQ), tDQSCK, tLZ(DQS), tHZ(DQS)

These parameters are measured from a specific clock edge to a data signal (DMn, DQm.: n=0,1,2,3. m=0 –31) transition and will be met with respect to that clock edge. Therefore, they are not affected by the amount of clock jitter applied (i.e. tJIT(per).

2.6.3.3 tQSH, tQSL

These parameters are affected by duty cycle jitter which is represented by tCH(abs)min and tCL(abs)min. Therefore tQSH(abs)min and tQSL(abs)min can be specified with tCH(abs)min and tCL(abs)min.

tQSH(abs)min = tCH(abs)min - 0.05

tQSL(abs)min = tCL(abs)min - 0.05

These parameters determine absolute Data-Valid window at the DDR2 Mobile RAM device pin.

Absolute min data-valid window @ DDR2 Mobile RAM device pin =

min { (tQSH(abs)min × tCK(avg)min - tDQSQmax - tQHSmax) , (tQSL(abs)min × tCK(avg)min - tDQSQmax - tQHSmax) }

This minimum data-valid window shall be met at the target frequency regardless of clock jitter.

2.6.3.4 tRPST

tRPST is affected by duty cycle jitter which is represented by tCL(abs). Therefore tRPST(abs)min can be specified by tCL(abs)min.

tRPST(abs)min = tCL(abs)min - 0.05 = tQSL(abs)min

2.6.4 Clock jitter effects on Write timing parameters

2.6.4.1 tDS, tDH

These parameters are measured from a data signal (DMn, DQm.: n=0,1,2,3. m=0 –31) transition edge to its respective data strobe signal (DQSn, /DQSn : n=0,1,2,3) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), as the setup and hold are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values shall be met.

2.6.4.2 tDSS, tDSH

These parameters are measured from a data strobe signal (DQSx, /DQSx) crossing to its respective clock signal (CK, /CK) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), as the setup and hold are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values shall be met.

2.6.4.3 tDQSS

This parameter is measured from a data strobe signal (DQSx, /DQSx) crossing to the subsequent clock signal (CK, /CK) crossing. When the device is operated with input clock jitter, this parameter needs to be de-rated by the actual tJIT(per),act of the input clock in excess of the period jitter tJIT(per),allowed.

$$tDQSS(min, derated) = 0.75 - \frac{tJIT(per), act,min - tJIT(per),allowed,min}{tCK(avg)}$$

$$tDQSS(max, derated) = 1.25 - \frac{tJIT(per), act,max - tJIT(per),allowed,max}{tCK(avg)}$$

For example,

if the measured jitter into a LPDDR2-800 device has tCK(avg)= 2500 ps, tJIT(per),act,min= -172 ps and tJIT(per),act,max= + 193 ps, then

tDQSS,(min,derated) = 0.75 -(tJIT(per),act,min - tJIT(per),allowed,min)/tCK(avg) = 0.75 - (-172 + 100) /2500 = 0.7788 tCK(avg)

and

tDQSS,(max,derated) = 1.25 - (tJIT(per),act,max - tJIT(per),allowed,max)/tCK(avg) = 1.25 - (193 - 100) /2500 = 1.2128 tCK(avg)

2.7 AC Characteristics

(TJ = -30°C to +85°C, VDD1 = 1.70V to 1.95V, VDD2, VDDQ = 1.14V to 1.30V)

Table 30 AC Characteristics Table*6

Parameter	Symbol	min. max.	min. tCK*9	1066	800	667	533	400	Unit
Max. Frequency*4			—	533	400	333	266	200	MHz
Clock Timing									
Average Clock Period	tCK(avg)	min.	—	1.875	2.5	3	3.75	5	ns
		max.	—	100					ns
Average high pulse width	tCH(avg)	min.	—	0.45					tCK(avg)
		max.	—	0.55					
Average low pulse width	tCL(avg)	min.	—	0.45					tCK(avg)
		max.	—	0.55					
Absolute Clock Period	tCK(abs)	min.	—	tCK(avg)(min.) + tJIT(per)(min.)					ps
Absolute clock HIGH pulse width (with allowed jitter)	tCH(abs), allowed	min.	—	0.43					tCK(avg)
		max.	—	0.57					
Absolute clock LOW pulse width (with allowed jitter)	tCL(abs), allowed	min.	—	0.43					tCK(avg)
		max.	—	0.57					
Clock Period Jitter (with allowed jitter)	tJIT(per), allowed	min.	—	-90	-100	-110	-120	-140	ps
		max.	—	90	100	110	120	140	
Maximum Clock Jitter between two consecutive clock cycles (with allowed jitter)	tJIT(cc), allowed	max.	—	180	200	220	240	280	ps
Duty cycle Jitter (with allowed jitter)	tJIT(duty), allowed	min.	—	min((tCH(abs),min - tCH(avg),min), (tCL(abs),min - tCL(avg),min)) × tCK(avg)					ps
		max.	—	max((tCH(abs),max - tCH(avg),max), (tCL(abs),max - tCL(avg),max)) × tCK(avg)					
Cumulative error across 2 cycles	tERR(2per), allowed	min.	—	-132	-147	-162	-177	-206	ps
		max.	—	132	147	162	177	206	
Cumulative error across 3 cycles	tERR(3per), allowed	min.	—	-157	-175	-192	-210	-245	ps
		max.	—	157	175	192	210	245	
Cumulative error across 4 cycles	tERR(4per), allowed	min.	—	-175	-194	-214	-233	-272	ps
		max.	—	175	194	214	233	272	
Cumulative error across 5 cycles	tERR(5per), allowed	min.	—	-188	-209	-230	-251	-293	ps
		max.	—	188	209	230	251	293	
Cumulative error across 6 cycles	tERR(6per), allowed	min.	—	-200	-222	-244	-266	-311	ps
		max.	—	200	222	244	266	311	
Cumulative error across 7 cycles	tERR(7per), allowed	min.	—	-209	-232	-256	-279	-325	ps
		max.	—	209	232	256	279	325	

Table 30 AC Characteristics Table*6 (cont'd)

Parameter	Symbol	min. max.	min. tCK*9	1066	800	667	533	400	Unit
Cumulative error across 8 cycles	tERR(8per), allowed	min.	—	-217	-241	-266	-290	-338	ps
		max.	—	217	241	266	290	338	
Cumulative error across 9 cycles	tERR(9per), allowed	min.	—	-224	-249	-274	-299	-349	ps
		max.	—	224	249	274	299	349	
Cumulative error across 10 cycles	tERR(10per), allowed	min.	—	-231	-257	-282	-308	-359	ps
		max.	—	231	257	282	308	359	
Cumulative error across 11 cycles	tERR(11per), allowed	min.	—	-237	-263	-289	-316	-368	ps
		max.	—	237	263	289	316	368	
Cumulative error across 12 cycles	tERR(12per), allowed	min.	—	-242	-269	-296	-323	-377	ps
		max.	—	242	269	296	323	377	
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR(nper), allowed	min.	—	tERR(nper),allowed,min. = (1 + 0.68ln(n)) × tJIT(per),allowed,min.					ps
		max.	—	tERR(nper),allowed,max. = (1 + 0.68ln(n)) × tJIT(per),allowed,max.					
Read Parameters									
DQS output access time from CK, /CK	tDQSCK	min.	—	2500					ps
		max.	—	5500					
DQSCK Delta Short*15	tDQSCKDS	max.	—	330	450	540	670	900	ps
DQSCK Delta Medium*16	tDQSCKDM	max.	—	680	900	1050	1350	1800	ps
DQSCK Delta Long*17	tDQSCKDL	max.	—	920	1200	1400	1800	2400	ps
DQS – DQ skew	tDQSQ	max.	—	200	240	280	340	400	ps
Data hold skew factor	tQHS	max.	—	230	280	340	400	480	ps
DQS Output High Pulse Width	tQSH	min.	—	tCH(abs) - 0.05					tCK(avg)
DQS Output Low Pulse Width	tQSL	min.	—	tCL(abs) - 0.05					tCK(avg)
Data Half Period	tQHP	min.	—	min(tQSH, tQSL)					tCK(avg)
DQ / DQS output hold time from DQS	tQH	min.	—	tQHP - tQHS					ps
Read preamble*12,*13	tRPRE	min.	—	0.9					tCK(avg)
Read postamble*12,*14	tRPST	min.	—	tCL(abs) - 0.05					tCK(avg)
DQS low-Z from clock*12	tLZ(DQS)	min.	—	tDQSCK(min.) - 300					ps
DQ low-Z from clock*12	tLZ(DQ)	min.	—	tDQSCK(min.) - (1.4 × tQHS(max.))					ps
DQS high-Z from clock*12	tHZ(DQS)	max.	—	tDQSCK(max.) - 100					ps
DQ high-Z from clock*12	tHZ(DQ)	max.	—	tDQSCK(max.) + (1.4 × tDQSQ(max.))					ps

Table 30 AC Characteristics Table*6 (cont'd)

Parameter	Symbol	min. max.	min. tCK*9	1066	800	667	533	400	Unit
Write Parameters*11									
DQ and DM input hold time (VREF based)	tDH	min.	—	210	270	350	430	480	ps
DQ and DM input setup time (VREF based)	tDS	min.	—	210	270	350	430	480	ps
DQ and DM input pulse width	tDIPW	min.	—	0.35					tCK(avg)
Write command to 1st DQS latching transition	tDQSS	min.	—	0.75					tCK(avg)
		max.	—	1.25					
DQS input high-level width	tDQSH	min.	—	0.4					tCK(avg)
DQS input low-level width	tDQSL	min.	—	0.4					tCK(avg)
DQS falling edge to CK setup time	tDSS	min.	—	0.2					tCK(avg)
DQS falling edge hold time from CK	tDSH	min.	—	0.2					tCK(avg)
Write postamble	tWPST	min.	—	0.4					tCK(avg)
Write preamble	tWPRE	min.	—	0.35					tCK(avg)
CKE Input Parameters									
CKE min. pulse width (high and low pulse width)	tCKE	min.	3	3					tCK(avg)
CKE input setup time	tISCKE*2	min.	—	0.25					tCK(avg)
CKE input hold time	tIHCKE*3	min.	—	0.25					tCK(avg)
Command Address Input Parameters*11									
Address and control input setup time (VREF based)	tIS*1	min.	—	220	290	370	460	600	ps
Address and control input hold time (VREF based)	tIH*1	min.	—	220	290	370	460	600	ps
Address and control input pulse width	tIPW	min.	—	0.40					tCK(avg)
Boot Parameters (10 MHz – 55 MHz)*5,*7,*8									
Clock Cycle Time	tCKb	max.	—	100					ns
		min.	—	18					
CKE Input Setup Time	tISCKEb	min.	—	2.5					ns
CKE Input Hold Time	tIHCKEb	min.	—	2.5					ns
Address & Control Input Setup Time	tISb	min.	—	1150					ps
Address & Control Input Hold Time	tIHb	min.	—	1150					ps
DQS Output Data Access Time from CK, /CK	tDQSCKb	min.	—	2.0					ns
		max.	—	10.0					
Data Strobe Edge to Ouput Data Edge tDQSQb - 1.2	tDQSQb	max.	—	1.2					ns
Data Hold Skew Factor	tQHSb	max.	—	1.2					ns
Mode Register Parameters									
Mode Register Write command period	tMRW	min.	5	5					tCK(avg)
Mode Register Read command period	tMRR	min.	2	2					tCK(avg)

Table 30 AC Characteristics Table*6 (cont'd)

Parameter	Symbol	min. max.	min. tCK*9	1066	800	667	533	400	Unit
DDR2 Mobile RAM Core Parameters*9									
Read Latency	RL	min.	3	8	6	5	4	3	tCK(avg)
Write Latency	WL	min.	1	4	3	2	2	1	tCK(avg)
ACTIVE to ACTIVE command period	tRC	min.	—	tRAS + tRPab (with all-bank Precharge) tRAS + tRPpb (with per-bank Precharge)					ns
CKE min. pulse width during Self-Refresh (low pulse width during Self-Refresh)	tCKESR	min.	3	15					ns
Self-refresh exit to next valid command delay	tXSR	min.	2	tRFCab + 10					ns
Exit power down to next valid command delay	tXP	min.	2	7.5					ns
CAS to CAS delay	tCCD	min.	2	2					tCK(avg)
Internal Read to Precharge command delay	tRTP	min.	2	7.5					ns
RAS to CAS Delay	tRCD	min.	3	18					ns
Row Precharge Time (single bank)	tRPpb	min.	3	18					ns
Row Precharge Time (all banks)	tRPab	min.	3	21					ns
Row Active Time	tRAS	min.	3	42					ns
		max.	—	70					µs
Write Recovery Time	tWR	min.	3	15					ns
Internal Write to Read Command Delay	tWTR	min.	2	7.5				10	ns
Active bank A to Active bank B	tRRD	min.	2	10					ns
Four Bank Activate Window	tFAW	min.	8	50					ns
Minimum Deep Power Down Time	tDPD	min.	—	500					µs
DDR2 Mobile RAM Refresh Requirement Parameters									
Refresh Window	tREFW	max.	—	32					ms
Required number of REFRESH commands	R	min.	—	8192					
Average time between REFRESH commands (for reference only)	tREFI	max.	—	3.9					µs
	tREFIpb	max.	—	0.4875					µs
Refresh Cycle time	tRFCab	min.	—	130					ns
Per Bank Refresh Cycle time	tRFCpb	min.	—	60					ns
Burst Refresh Window = 4 × 8 × tRFCab	tREFBW	min.	—	4.16					µs
ZQ Calibration Parameters*9									
Initialization Calibration Time	tZQINIT	min.	—	1					µs
Long Calibration Time	tZQCL	min.	6	360					ns
Short Calibration Time	tZQCS	min.	6	90					ns
Calibration Reset Time	tZQRESET	min.	3	50					ns

Notes: 1. Input set-up/hold time for signal(CA0 – CA9, /CS).

2. CKE input setup time is measured from CKE reaching high/low voltage level to CK, /CK crossing.
3. CKE input hold time is measured from CK, /CK crossing to CKE reaching high/low voltage level.
4. Frequency values are for reference only. Clock cycle time (tCK) shall be used to determine device capabilities.
5. To guarantee device operation before the DDR2 Mobile RAM Device is configured a number of AC boot timing parameters are defined in the Table 30 on page 31. Boot parameter symbols have the letter b appended, e.g. tCK during boot is tCKb.
6. Frequency values are for reference only. Clock cycle time (tCK or tCKb) shall be used to determine device capabilities.
7. The DDR2 Mobile RAM will set some Mode register default values upon receiving a RESET (MRW) command as specified in “Mode Register Definition” on page 60.
8. The output skew parameters are measured with Ron default settings into the reference load.
9. These parameters should be satisfied with both specification, analog (ns) value and min. tCK.
10. All AC timings assume an input slew rate of 1V/ns.
11. Read, Write, and Input Setup and Hold values are referenced to VREF.
12. For low-to-high and high-to-low transitions the timing reference will be at the point when the signal crosses VTT. tHZ and tLZ transitions occur in the same access time (with respect to clock) as valid data transitions. These parameters are not referenced to a specific voltage level but to the time when the device output is no longer driving (for tRPST, tHZ(DQS) and tHZ(DQ)), or begins driving (for tRPRE, tLZ(DQS), tLZ(DQ)). Figure 12 shows a method to calculate the point when device is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.

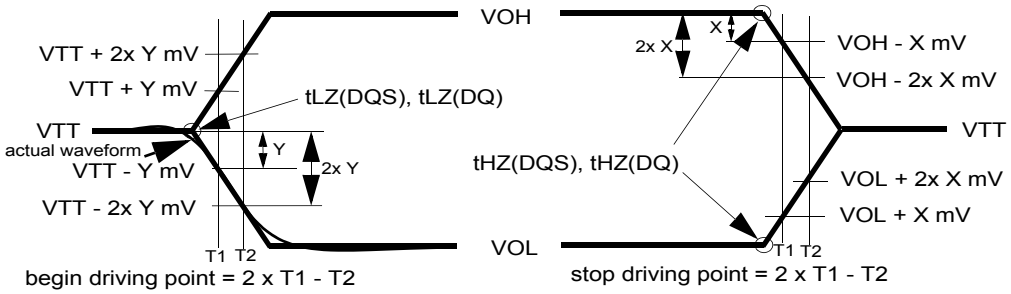


Figure 12 — tLZ and tHZ Method for Calculating Transition and Endpoints

The parameters tLZ(DQS), tLZ(DQ), tHZ(DQS), and tHZ(DQ) are defined as single-ended. The timing parameters tRPRE and tRPST are determined from the differential signal DQS-/DQS.

13. Measured from the start driving of DQS – /DQS to the start driving the first rising strobe edge.
14. Measured from the from start driving the last falling strobe edge to the stop driving DQS – /DQS.
15. tDQSCKDS is the absolute value of the difference between any two tDQSCK measurements (within a byte lane) within a contiguous sequence of bursts within a 160ns rolling window. tDQSCKDS is not tested and is guaranteed by design. Temperature drift in the system is < 10°C/s. Values do not include clock jitter.
16. tDQSCKDM is the absolute value of the difference between any two tDQSCK measurements (within a byte lane) within a 1.6µs rolling window. tDQSCKDM is not tested and is guaranteed by design. Temperature drift in the system is < 10°C/s. Values do not include clock jitter.
17. tDQSCKDL is the absolute value of the difference between any two tDQSCK measurements (within a byte lane) within a 32ms rolling window. tDQSCKDL is not tested and is guaranteed by design. Temperature drift in the system is < 10°C/s. Values do not include clock jitter.

2.7.1 HSUL_12 Driver Output Timing Reference Load

These 'Timing Reference Loads' are not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

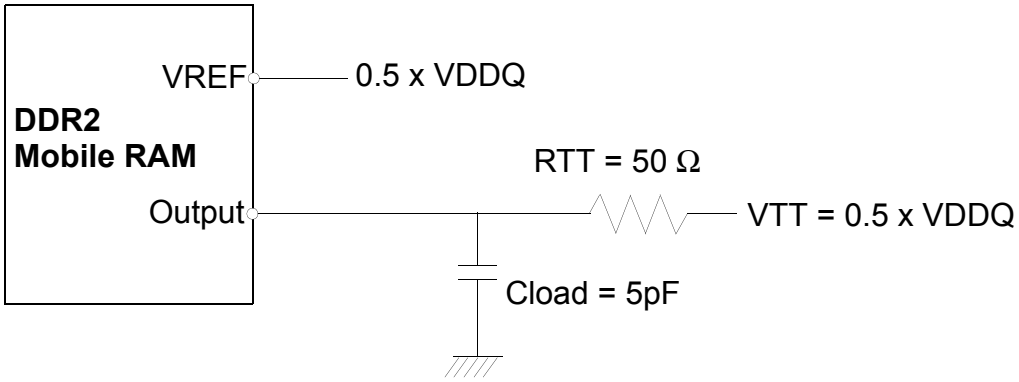


Figure 13 — HSUL_12 Driver Output Reference Load for Timing and Slew Rate

Note: 1. All output timing parameter values (like tDQSCK, tDQSQ, tQHS, tHZ, tRPRE etc) are reported with respect to this reference load. This reference load is also used to report slew rate.

2.8 CA and /CS Setup, Hold and Derating

For all input signals (CA and /CS) the total tIS (setup time) and tIH (hold time) required is calculated by adding the data sheet tIS(base) andtIH(base) value (see Table 31) to the ΔtIS and ΔtIH derating value (see Table 32 and Table 33) respectively. Example: tIS (total setup time) = tIS(base) + ΔtIS

Setup (tIS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(DC) and the first crossing of VIH(AC)min. Setup (tIS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VREF(DC) and the first crossing of VIL(AC)max. If the actual signal is always earlier than the nominal slew rate line between shaded 'VREF(DC) to AC region', use nominal slew rate for derating value (see Figure 14). If the actual signal is later than the nominal slew rate line anywhere between shaded 'VREF(DC) to AC region', the slew rate of a tangent line to the actual signal from the AC level to DC level is used for derating value (see Figure 16).

Hold (tIH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(DC)max and the first crossing of VREF(DC). Hold (tIH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(DC)min and the first crossing of VREF(DC). If the actual signal is always later than the nominal slew rate line between shaded 'DC to VREF(DC) region', use nominal slew rate for derating value (see Figure 15). If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'DC to VREF(DC) region', the slew rate of a tangent line to the actual signal from the DC level to VREF(DC) level is used for derating value (see Figure 17). For a valid transition the input signal has to remain above/below VIH/IL(AC) for some time tVAC (see Table 34). Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached VIH/IL(AC) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach VIH/IL(AC).

For slew rates in between the values listed in Table 31, the derating values may obtained by linear interpolation.
These values are typically not subject to production test. They are verified by design and characterization.

Table 31 CA and /CS Setup and Hold Base-Values for 1V/ns

Unit [ps]	1066	800	667	533	400	Reference
tIS(base)	0	70	150	240	—	VIH/L(AC)=VREF(DC) ± 220mV
	—	—	—	—	300	VIH/L(AC)=VREF(DC) ± 300mV
tIH(base)	90	160	240	330	—	VIH/L(DC)=VREF(DC) ± 130mV
	—	—	—	—	400	VIH/L(DC)=VREF(DC) ± 200mV

Note: 1. AC/DC referenced for 1V/ns CA and /CS slew rate and 2 V/ns differential CK – /CK slew rate.

Table 32 Derating values DDR2 Mobile RAM tIS/tIH - AC/DC based AC220

ΔtIS, ΔtIH derating in [ps] AC/DC based [a] AC220 Threshold -> VIH(AC)=VREF(DC)+220mV, VIL(AC)=VREF(DC)-220mV DC130 Threshold -> VIH(DC)=VREF(DC)+130mV, VIL(DC)=VREF(DC)-130mV																	
		CK,/CK Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CA, /CS Slew rate V/ns	2.0	110	65	110	65	110	65										
	1.5	74	43	74	43	74	43	89	59								
	1.0	0	0	0	0	0	0	16	16	32	32						
	0.9			-3	-5	-3	-5	13	11	29	27	45	43				
	0.8					-8	-13	8	3	24	19	40	35	56	55		
	0.7							2	-6	18	10	34	26	50	46	66	78
	0.6									10	-3	26	13	42	33	58	65
	0.5											4	-4	20	16	36	48
	0.4													-7	2	17	34

a. Cell contents blanked are defined as ‘not supported’.

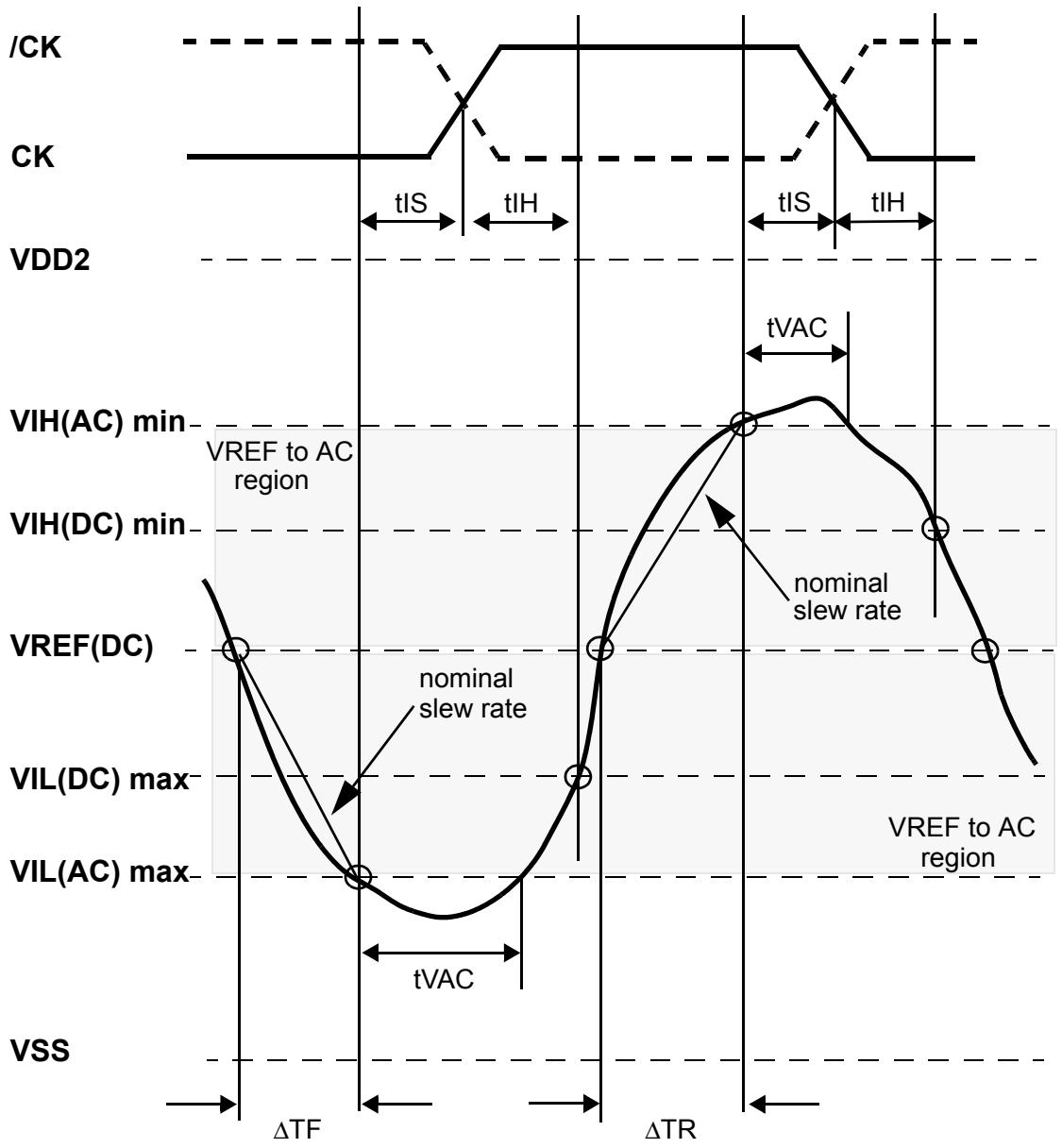
Table 33 Derating values DDR2 Mobile RAM tIS/tIH - AC/DC based AC300

ΔtIS, ΔtIH derating in [ps] AC/DC based [a] AC300 Threshold -> VIH(AC)=VREF(DC)+300mV, VIL(AC)=VREF(DC)-300mV DC200 Threshold -> VIH(DC)=VREF(DC)+200mV, VIL(DC)=VREF(DC)-200mV																	
		CK,/CK Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CA, /CS Slew rate V/ns	2.0	150	100	150	100	150	100										
	1.5	100	67	100	67	100	67	116	83								
	1.0	0	0	0	0	0	0	16	16	32	32						
	0.9			-4	-8	-4	-8	12	8	28	24	44	40				
	0.8					-12	-20	4	-4	20	12	36	28	52	48		
	0.7							-3	-18	13	-2	29	14	45	34	61	66
	0.6									2	-21	18	-5	34	15	50	47
	0.5											-12	-32	4	-12	20	20
	0.4													-35	-40	-11	-8

a. Cell contents blanked are defined as ‘not supported’.

Table 34 Required time tVAC above VIH(AC) {below VIL(AC)} for valid transition

Slew Rate [V/ns]	tVAC @ 300mV [ps]		tVAC @ 220mV [ps]	
	min.	max.	min.	max.
> 2.0	75	—	175	—
2.0	57	—	170	—
1.5	50	—	167	—
1.0	38	—	163	—
0.9	34	—	162	—
0.8	29	—	161	—
0.7	22	—	159	—
0.6	13	—	155	—
0.5	0	—	150	—
< 0.5	0	—	150	—



$$\text{Setup Slew Rate Falling Signal} = \frac{\text{VREF(DC)} - \text{VIL(AC)max}}{\Delta TF}$$

$$\text{Setup Slew Rate Rising Signal} = \frac{\text{VIH(AC)min} - \text{VREF(DC)}}{\Delta TR}$$

Figure 14 — Illustration of nominal slew rate and tVAC for setup time tIS for CA and /CS with respect to clock.

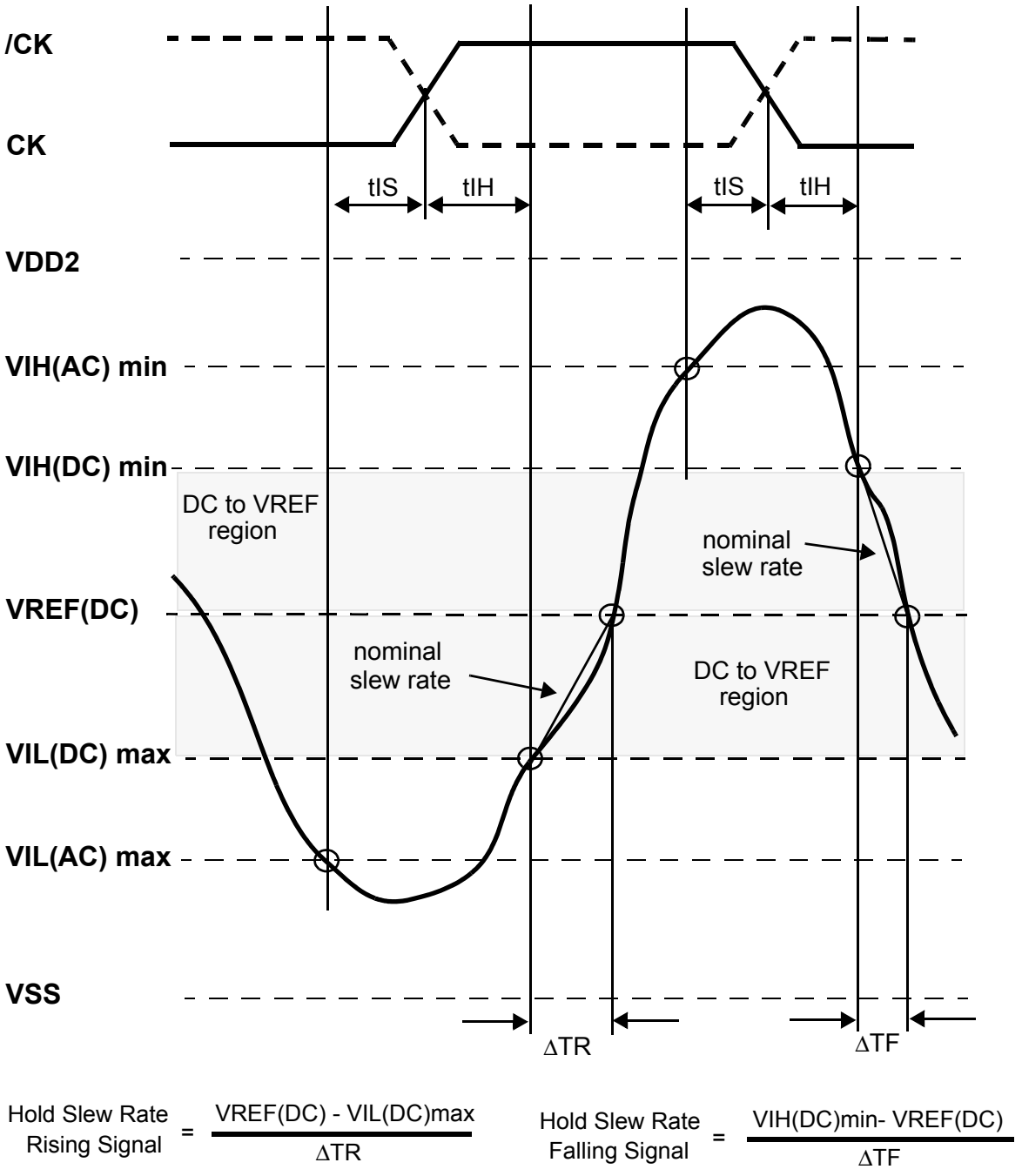


Figure 15 — Illustration of nominal slew rate for hold time tIH for CA and /CS with respect to clock

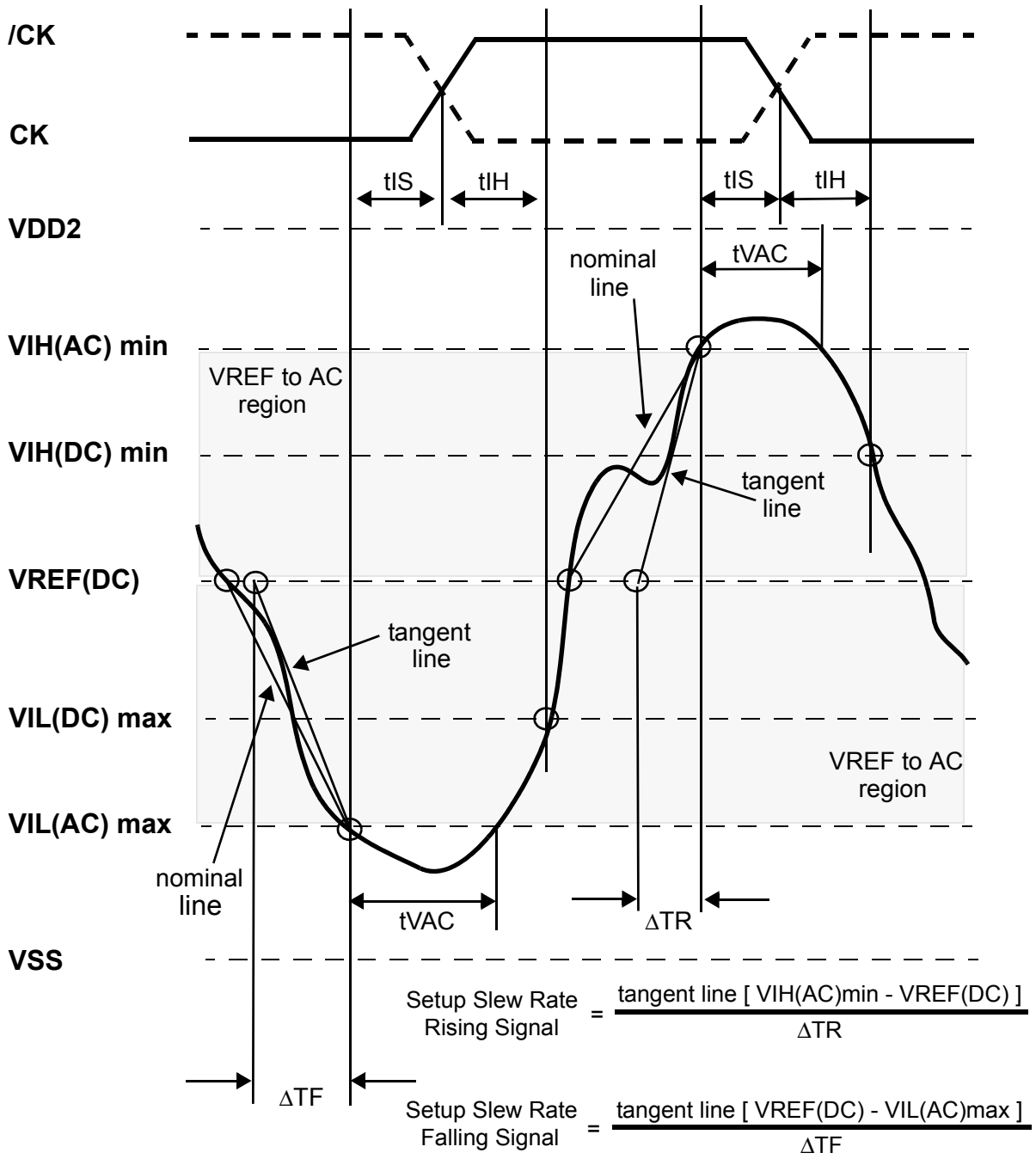
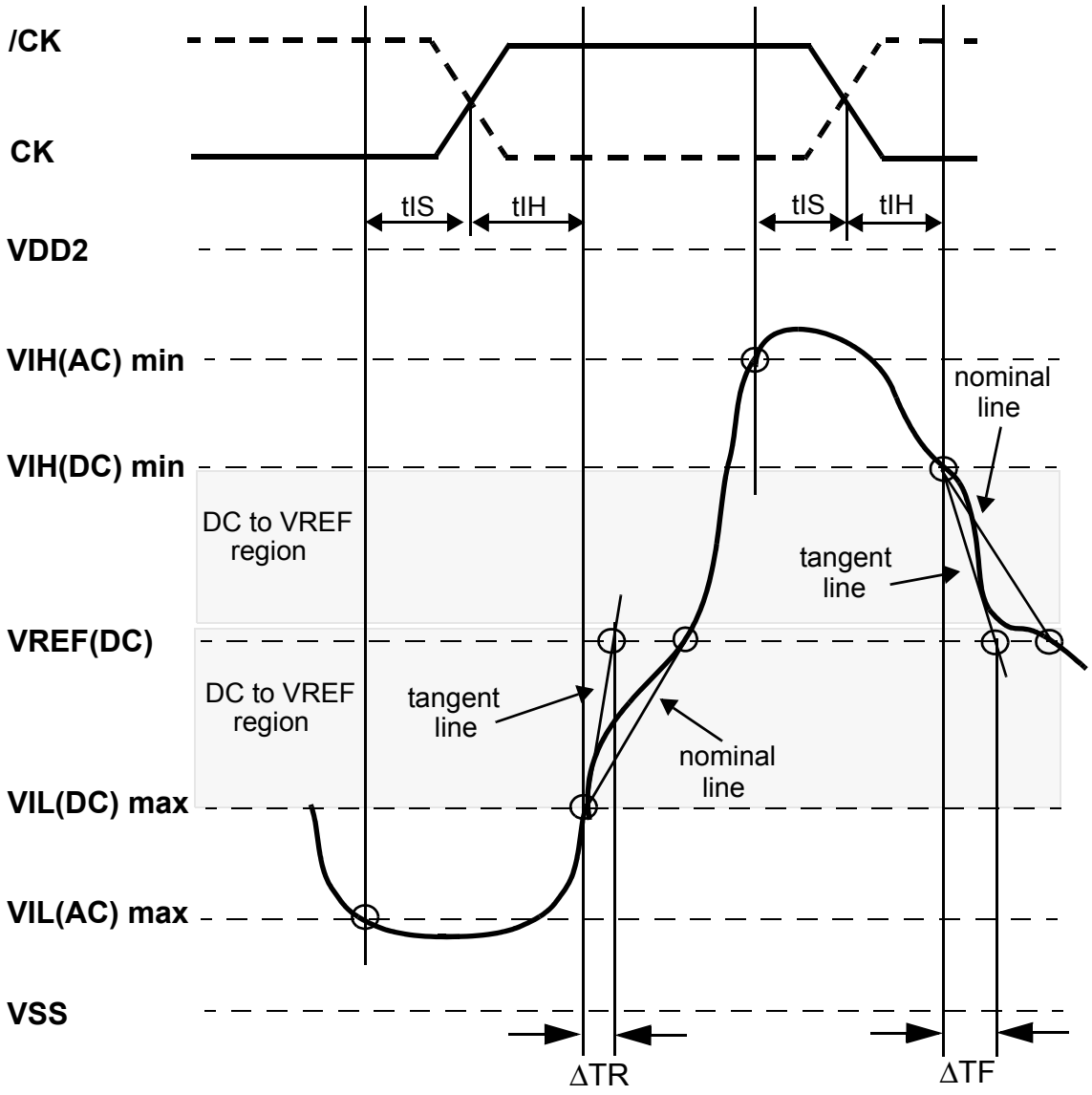


Figure 16 — Illustration of tangent line for setup time tIS for CA and /CS with respect to clock



$$\text{Hold Slew Rate Rising Signal} = \frac{\text{tangent line [VREF(DC) - VIL(DC)max]}}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{\text{tangent line [VIH(DC)min - VREF(DC)]}}{\Delta TF}$$

Figure 17 — Illustration of tangent line for hold time tIH for CA and /CS with respect to clock

2.9 Data Setup, Hold and Slew Rate Derating

For all input signals the total tDS (setup time) and tDH (hold time) required is calculated by adding the data sheet tDS(base) and tDH(base) value (see Table 35) to the ΔtDS and ΔtDH (see Table 36 and Table 37) derating value respectively. Example: tDS (total setup time) = tDS(base) + ΔtDS.

Setup (tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(DC) and the first crossing of VIH(AC)min. Setup (tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VREF(DC) and the first crossing of VIL(AC)max (see Figure 18). If the actual signal is always earlier than the nominal slew rate line between shaded 'VREF(DC) to ac region', use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between shaded 'VREF(DC) to AC region', the slew rate of a tangent line to the actual signal from the AC level to DC level is used for derating value (see Figure 20).

Hold (tDH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(DC)max and the first crossing of VREF(DC). Hold (tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(DC)min and the first crossing of VREF(DC) (see Figure 19). If the actual signal is always later than the nominal slew rate line between shaded 'DC level to VREF(DC) region', use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'DC to VREF(DC) region', the slew rate of a tangent line to the actual signal from the DC level to VREF(DC) level is used for derating value (see Figure 21).

For a valid transition the input signal has to remain above/below VIH/IL(AC) for some time tVAC (see Table 38).

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached VIH/IL(AC) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach VIH/IL(AC).

For slew rates in between the values listed in the tables the derating values may obtained by linear interpolation.

These values are typically not subject to production test. They are verified by design and characterization.

Table 35 Data Setup and Hold Base-Values

Unit [ps]	1066	800	667	533	400	Reference
tDS(base)	-10	50	130	210	—	VIH/L(AC)=VREF(DC) ± 220mV
	—	—	—	—	180	VIH/L(AC)=VREF(DC) ± 300mV
tDH(base)	80	140	220	300	—	VIH/L(DC)=VREF(DC) ± 130mV
	—	—	—	—	280	VIH/L(DC)=VREF(DC) ± 200mV

Note: 1. AC/DC referenced for 1V/ns DQ slew rate and 2 V/ns differential DQS – /DQS slew rate.

Table 36 Derating values DDR2 Mobile RAM tDS/tDH - AC/DC based AC220

ΔtDS, ΔDH derating in [ps] AC/DC based [a] AC220 Threshold -> VIH(AC)=VREF(DC)+220mV, VIL(AC)=VREF(DC)-220mV DC130 Threshold -> VIH(DC)=VREF(DC)+130mV, VIL(DC)=VREF(DC)-130mV																	
		DQS, /DQS Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew rate V/ns	2.0	110	65	110	65	110	65										
	1.5	74	43	73	43	73	43	89	59								
	1.0	0	0	0	0	0	0	16	16	32	32						
	0.9			-3	-5	-3	-5	13	11	29	27	45	43				
	0.8					-8	-13	8	3	24	19	40	35	56	55		
	0.7							2	-6	18	10	34	26	50	46	66	78
	0.6									10	-3	26	13	42	33	58	65
	0.5											4	-4	20	16	36	48
	0.4													-7	2	17	34

a. Cell contents blanked are defined as ‘not supported’.

Table 37 Derating values DDR2 Mobile RAM tDS/tDH - AC/DC based AC300

ΔtDS, ΔDH derating in [ps] AC/DC based [a] AC300 Threshold -> VIH(AC)=VREF(DC)+300mV, VIL(AC)=VREF(DC)-300mV DC200 Threshold -> VIH(DC)=VREF(DC)+200mV, VIL(DC)=VREF(DC)-200mV																	
		DQS, /DQS Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew rate V/ns	2.0	150	100	150	100	150	100										
	1.5	100	67	100	67	100	67	116	83								
	1.0	0	0	0	0	0	0	16	16	32	32						
	0.9			-4	-8	-4	-8	12	8	28	24	44	40				
	0.8					-12	-20	4	-4	20	12	36	28	52	48		
	0.7							-3	-18	13	-2	29	14	45	34	61	66
	0.6									2	-21	18	-5	34	15	50	47
	0.5											-12	-32	4	-12	20	20
	0.4													-35	-40	-11	-8

a. Cell contents blanked are defined as ‘not supported’.

Table 38 Required time tVAC above VIH(AC) {below VIL(AC)} for valid transition

Slew Rate [V/ns]	tVAC @ 300mV [ps]		tVAC @ 220mV [ps]	
	min.	max.	min.	max.
> 2.0	75	—	175	—
2.0	57	—	170	—
1.5	50	—	167	—
1.0	38	—	163	—
0.9	34	—	162	—
0.8	29	—	161	—
0.7	22	—	159	—
0.6	13	—	155	—
0.5	0	—	150	—
< 0.5	0	—	150	—

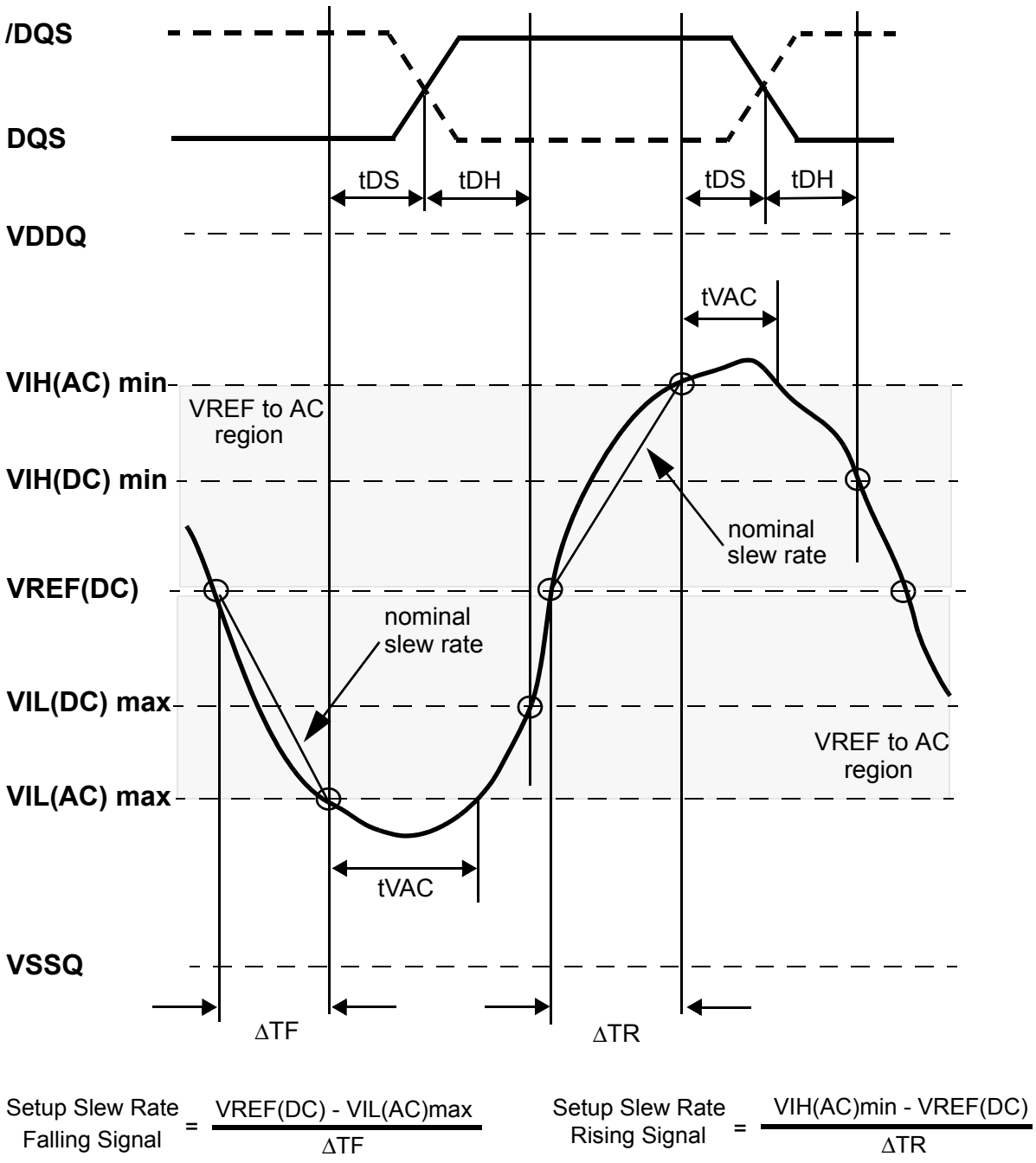
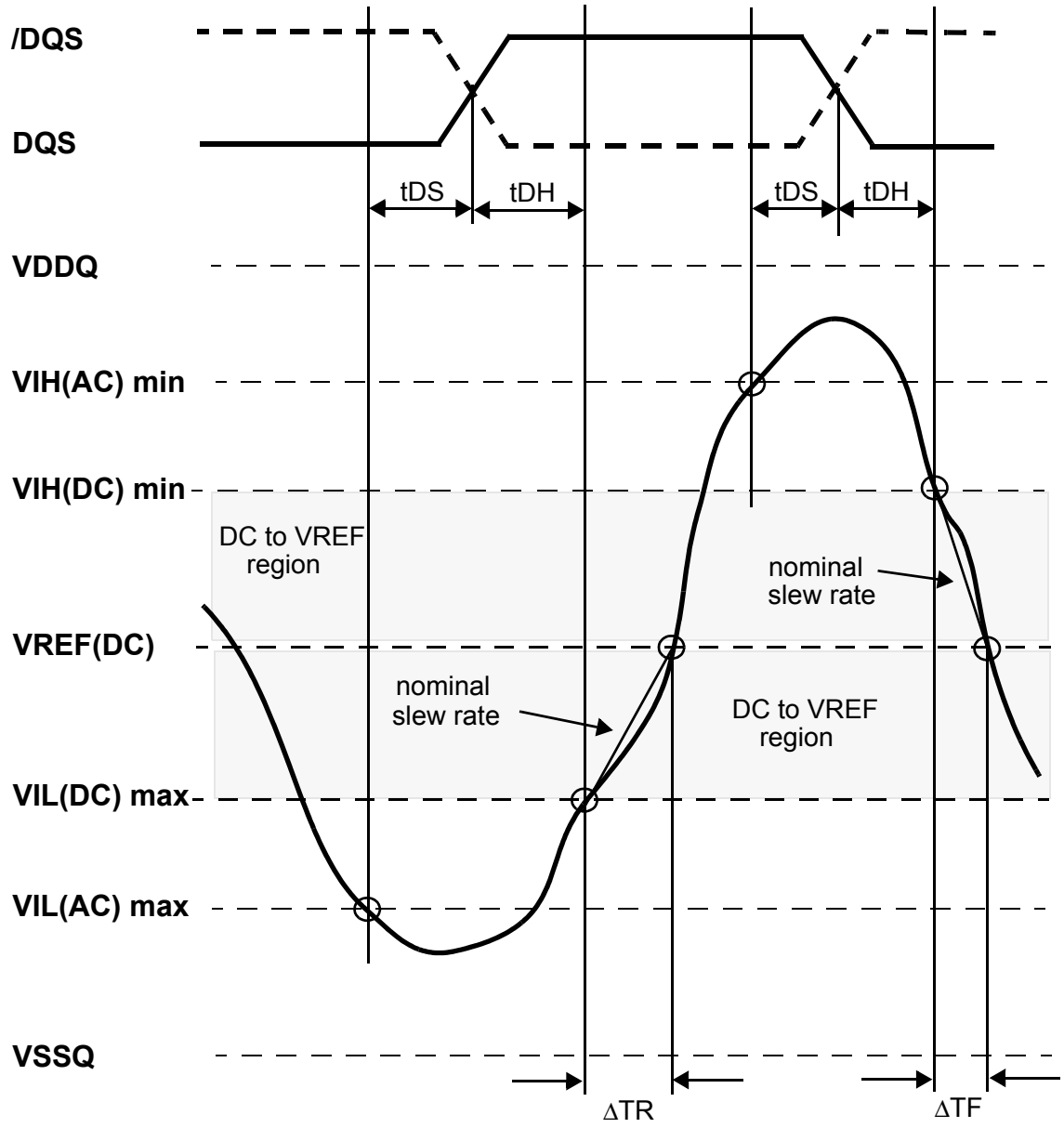


Figure 18 — Illustration of nominal slew rate and tVAC for setup time tDS for DQ with respect to strobe



$$\text{Hold Slew Rate Rising Signal} = \frac{\text{VREF(DC) - VIL(DC)max}}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{\text{VIH(DC)min - VREF(DC)}}{\Delta TF}$$

Figure 19 — Illustration of nominal slew rate for hold time tDH for DQ with respect to strobe

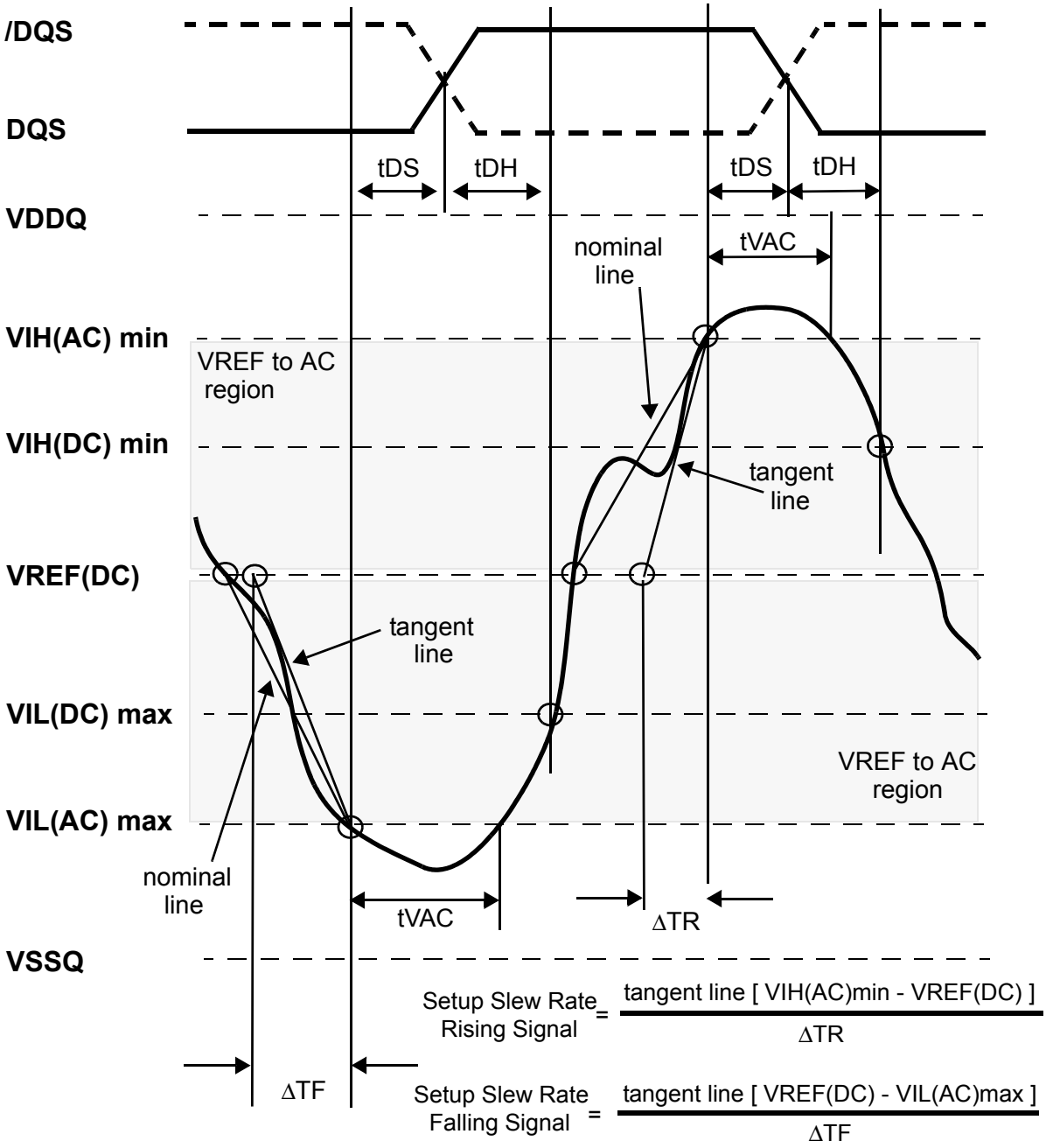
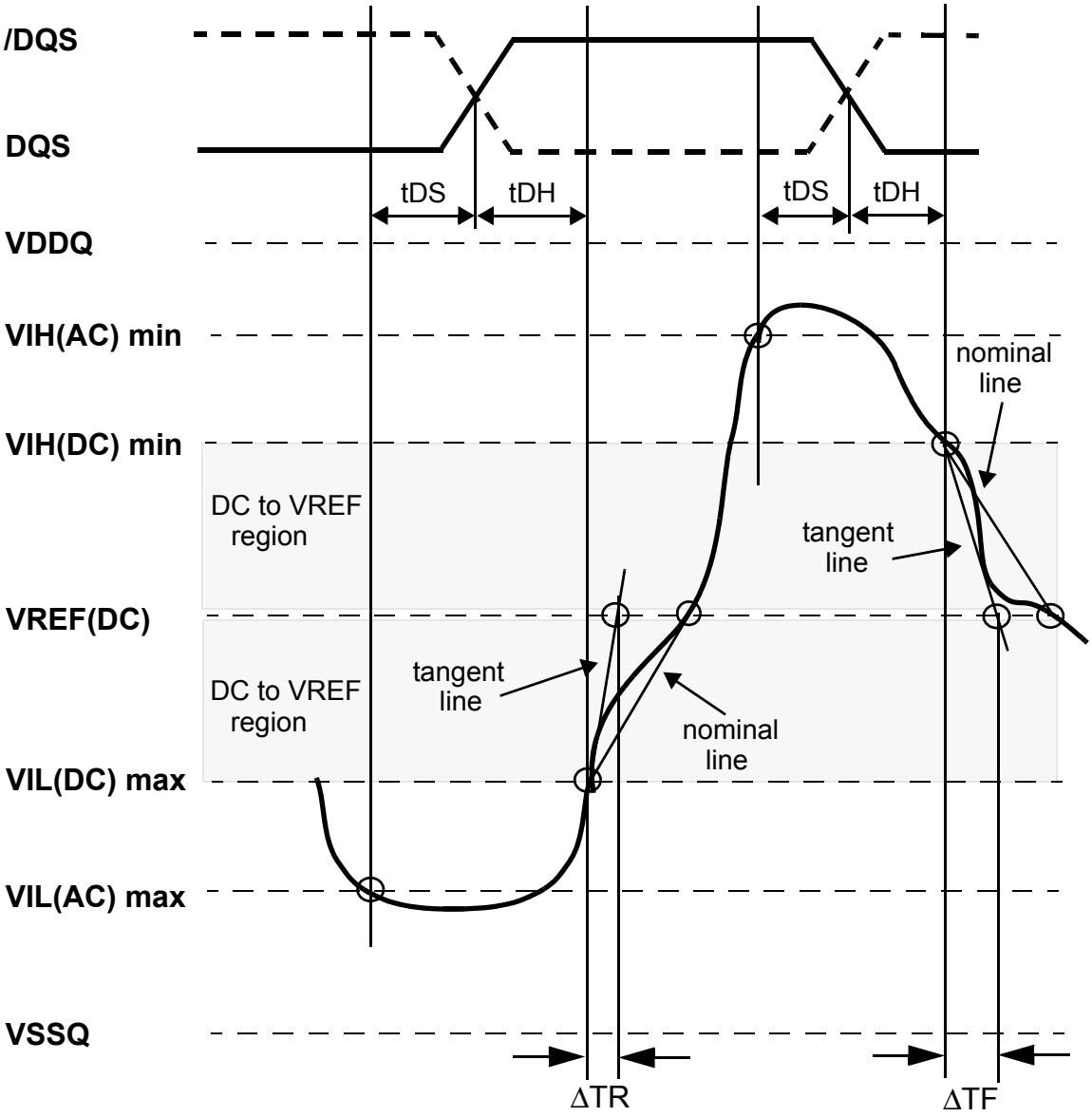


Figure 20 — Illustration of tangent line for setup time tDS for DQ with respect to strobe



$$\text{Hold Slew Rate Rising Signal} = \frac{\text{tangent line [VREF(DC) - VIL(DC)max]}}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{\text{tangent line [VIH(DC)min - VREF(DC)]}}{\Delta TF}$$

Figure 21 — Illustration of tangent line for hold time tDH for DQ with respect to strobe

3. Pin Function

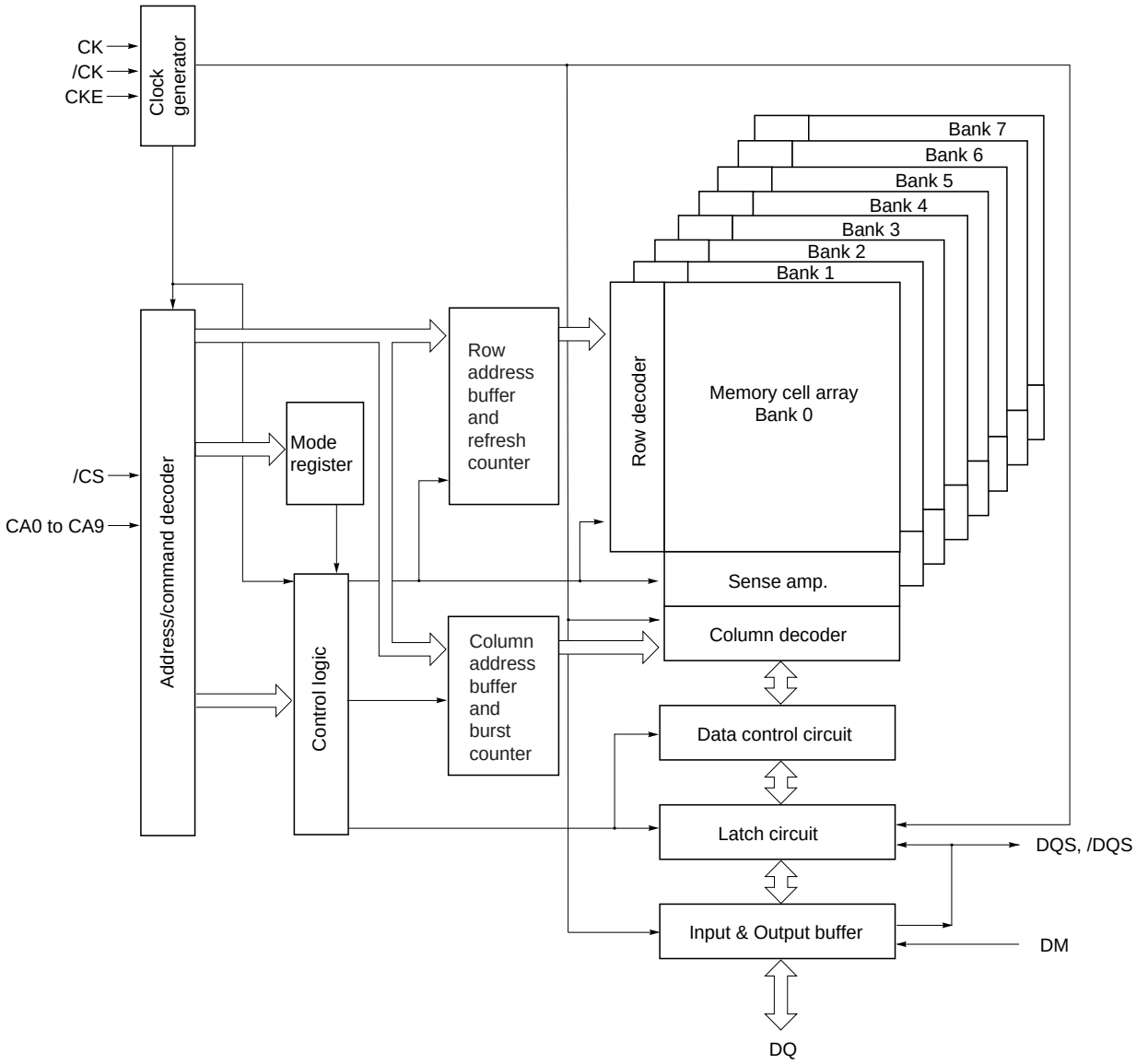
Table 39 Pad Definition and Description

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>CK, /CK</td><td>Input</td><td>Clock:
CK and /CK are differential clock inputs. All Double Data Rate (DDR) CA inputs are sampled on both positive and negative edge of CK. Single Data Rate (SDR) inputs, /CS and CKE, are sampled at the positive Clock edge.
Clock is defined as the differential pair, CK and /CK. The positive Clock edge is defined by the crosspoint of a rising CK and a falling /CK. The negative Clock edge is defined by the crosspoint of a falling CK and a rising /CK.</td></tr>
<tr><td>CKE</td><td>Input</td><td>Clock Enable:
CKE HIGH activates and CKE LOW deactivates internal clock signals and therefore device input buffers and output drivers. Power savings modes are entered and exited through CKE transitions.
CKE is considered part of the command code. See Command Truth Table on page 54 for command code descriptions. CKE is sampled at the positive Clock edge.</td></tr>
<tr><td>/CS</td><td>Input</td><td>Chip Select:
/CS is considered part of the command code. See Command Truth Table on page 54 for command code descriptions. /CS is sampled at the positive Clock edge.</td></tr>
<tr><td>CA0 – CA9</td><td>Input</td><td>DDR Command/Address Inputs:
Uni-directional command/address bus inputs.
CA is considered part of the command code. See Command Truth Table on page 54 for command code descriptions.</td></tr>
<tr><td>DQ0 – DQ31</td><td>I/O</td><td>Data Inputs/Output: Bi-directional data bus
x32 : DQ0 – DQ31 , x16 : DQ0 – DQ15</td></tr>
<tr><td>DQS0 – DQS3,
/DQS0 – /DQS3</td><td>I/O</td><td>Data Strobe (Bi-directional, Differential):
The data strobe is bi-directional (used for read and write data) and differential (DQS and /DQS). It is output with read data and input with write data. DQS is edge-aligned to read data and centered with write data.

The following is corresponding table between DQ and DQS, /DQS
<table>
<tr><th colspan="2">×32</th><th colspan="2">×16</th></tr>
<tr><th>DQ</th><th>DQS, /DQS</th><th>DQ</th><th>DQS, /DQS</th></tr>
<tr><td>DQ0-7</td><td>DQS0, /DQS0</td><td>DQ0-7</td><td>DQS0, /DQS0</td></tr>
<tr><td>DQ8-15</td><td>DQS1, /DQS1</td><td>DQ8-15</td><td>DQS1, /DQS1</td></tr>
<tr><td>DQ16-23</td><td>DQS2, /DQS2</td><td>—</td><td>—</td></tr>
<tr><td>DQ24-31</td><td>DQS3, /DQS3</td><td>—</td><td>—</td></tr>
</table></td></tr>
<tr><td>DM0 – DM3</td><td>Input</td><td>Input Data Mask:
DM is the input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM is for input only, the DM loading shall match the DQ and DQS (or /DQS).

The following is corresponding table between DQ and DM
<table>
<tr><th colspan="2">×32</th><th colspan="2">×16</th></tr>
<tr><th>DQ</th><th>DM</th><th>DQ</th><th>DM</th></tr>
<tr><td>DQ0-7</td><td>DM0</td><td>DQ0-7</td><td>DM0</td></tr>
<tr><td>DQ8-15</td><td>DM1</td><td>DQ8-15</td><td>DM1</td></tr>
<tr><td>DQ16-23</td><td>DM2</td><td>—</td><td>—</td></tr>
<tr><td>DQ24-31</td><td>DM3</td><td>—</td><td>—</td></tr>
</table></td></tr>
<tr><td>VDD1</td><td>Supply</td><td>Core Power Supply 1</td></tr>
<tr><td>VDD2</td><td>Supply</td><td>Core Power Supply 2</td></tr>
<tr><td>VDDQ</td><td>Supply</td><td>I/O Power Supply</td></tr>
<tr><td>VREFCA</td><td>Supply</td><td>Reference Voltage for CA Input Receiver</td></tr>
<tr><td>VREFDQ</td><td>Supply</td><td>Reference Voltage for DQ Input Receiver</td></tr>
<tr><td>VSS</td><td>Supply</td><td>Ground</td></tr>
<tr><td>VSSQ</td><td>Supply</td><td>I/O Ground</td></tr>
<tr><td>ZQ</td><td>I/O</td><td>Reference Pin for Output Drive Strength Calibration</td></tr>
</table>

4. Block Diagram



5. Simplified State Diagram

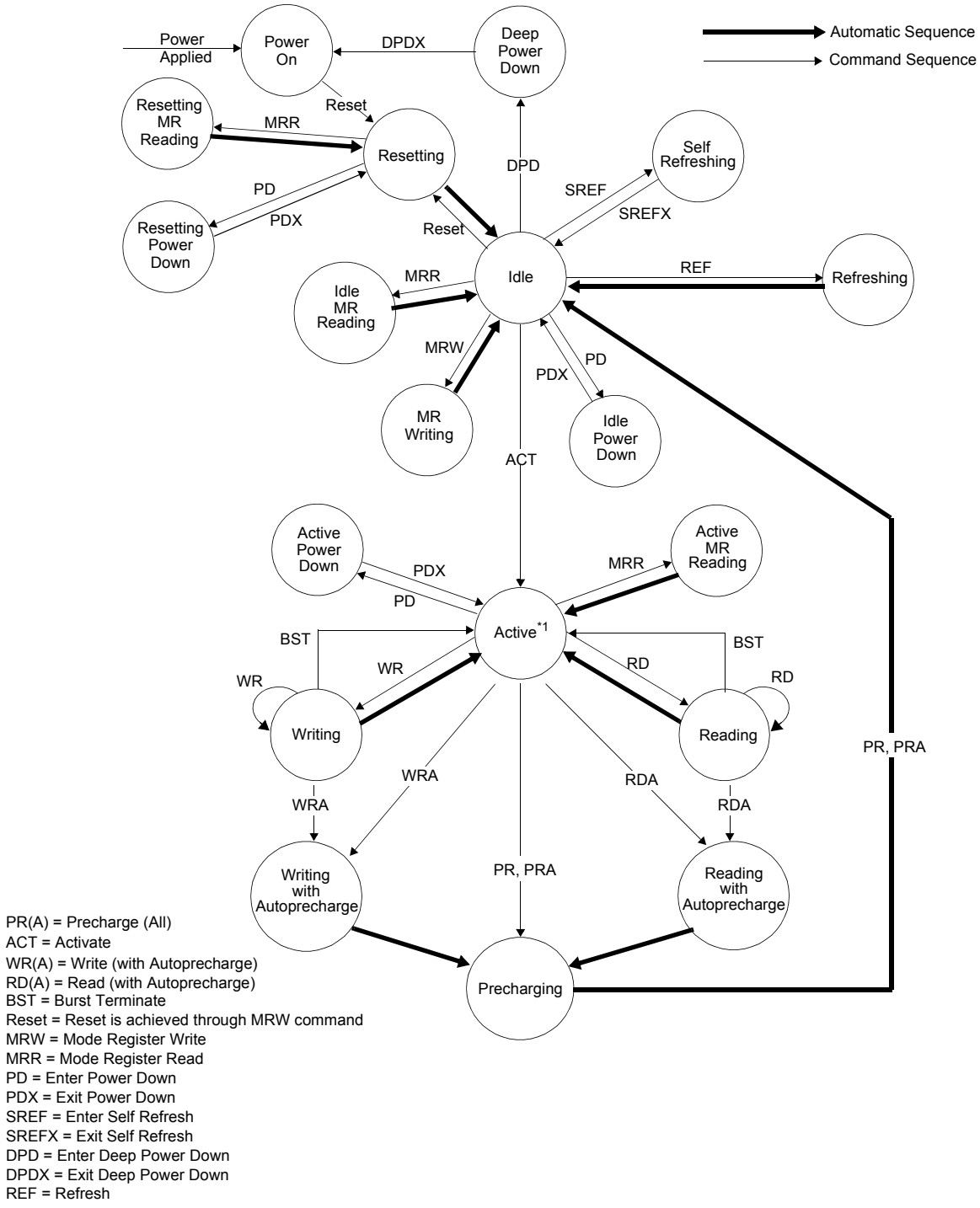


Figure 22 — Simplified Bus Interface State Diagram

Note 1: For DDR2 Mobile RAM in the Idle state, all banks are precharged.

6. Truth tables

Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the DDR2 Mobile RAM Device must be powered down and then restarted through the specified initialization sequence before normal operation can continue.

Table 40 provides the command truth table.

Table 40 Command Truth Table

Command	SDR Command Pins			DDR CA pins (10)										
	CKE		/CS	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	CK EDGE
	CK(n-1)	CK(n)												
MRW	H	H	L	L	L	L	L	MA0	MA1	MA2	MA3	MA4	MA5	↑
				MA6	MA7	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	↓
MRR	H	H	L	L	L	L	H	MA0	MA1	MA2	MA3	MA4	MA5	↑
				MA6	MA7	X								↓
Refresh (per bank)	H	H	L	L	L	H	L	X						↑
				X										↓
Refresh (all bank)	H	H	L	L	L	H	H	X						↑
				X										↓
Enter Self-Refresh	H	L	L	L	L	H	X							↑
				X										↓
Activate (bank)	H	H	L	L	H	R8	R9	R10	R11	R12	BA0	BA1	BA2	↑
				R0	R1	R2	R3	R4	R5	R6	R7	R13	RFU	↓
Write (bank)	H	H	L	H	L	L	RFU	RFU	C1	C2	BA0	BA1	BA2	↑
				AP*3	C3	C4	C5	C6	C7	C8	C9	RFU	RFU	↓
Read (bank)	H	H	L	H	L	H	RFU	RFU	C1	C2	BA0	BA1	BA2	↑
				AP*3	C3	C4	C5	C6	C7	C8	C9	RFU	RFU	↓
Precharge (bank)	H	H	L	H	H	L	H	AB	X	X	BA0	BA1	BA2	↑
				X	X	X	X	X	X	X	X	X	X	↓
BST	H	H	L	H	H	L	L	X						↑
				X										↓
Enter Deep Power Down	H	L	L	H	H	L	X							↑
				X										↓
NOP	H	H	L	H	H	H	X							↑
				X										↓
Maintain PD, SREF, DPD (NOP)	L	L	L	H	H	H	X							↑
				X										↓

Table 40 Command Truth Table

Command	SDR Command Pins			DDR CA pins (10)										
	CKE		/CS	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	CK EDGE
	CK(n-1)	CK(n)												
NOP	H	H	H	X										
				X										
Maintain PD, SREF, DPD (NOP)	L	L	H	X										
				X										
Enter Power Down	H	L	H	X										
				X										
Exit PD, SREF, DPD	L	H	H	X										
				X										

Notes: 1. All commands are defined by states of /CS, CA0, CA1, CA2, CA3, and CKE at the rising edge of the clock.
2. Bank addresses determine which bank is to be operated upon.
3. AP “high” during a READ or WRITE command indicates that an auto-precharge will occur to the bank associated with the READ or WRITE command.
4. “X” means “H or L (but a defined logic level)”
5. Self-refresh exit and Deep Power Down exit are asynchronous.
6. VREF must be between 0 and VDDQ during Self-Refresh and Deep Power Down operation.
7. CAxr refers to command/address bit “x” on the rising edge of clock.
8. CAxf refers to command/address bit “x” on the falling edge of clock.
9. /CS and CKE are sampled at the rising edge of clock.
10. The least-significant column address C0 is not transmitted on the CA bus, and is implied to be zero.
11. RFU needs to input “H” or “L“ (but a defined logic level).

7. Power-up, initialization and Power-Off

DDR2 Mobile RAM Devices must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation.

7.1 Power Ramp and Device Initialization

The following sequence shall be used to power-up an DDR2 Mobile RAM Device. Unless specified otherwise, these steps are mandatory.

1. Power Ramp

   While applying power (after Ta), CKE shall be held at a logic low level (≤ 0.2 × VDD2), all other inputs shall be between VILmin and VIHmax. The DDR2 Mobile RAM Device will only guarantee that outputs are in a high impedance state while CKE is held low.
   On or before the completion of the power ramp (Tb) CKE must be held low.
   DQ, DM, DQS and /DQS voltage levels must be between VSSQ and VDDQ during voltage ramp time to avoid latch-up. CK, /CK, /CS and CA inputs levels must be between VSS and VDD2 during voltage ramp up to avoid latch-up.

   The following conditions apply:

   Ta is the point where any power supply first reaches 300mV.

   After Ta is reached, VDD1 must be greater than VDD2 - 200mV.

   After Ta is reached, VDD1 and VDD2 must be greater than VDDQ - 200mV.

   After Ta is reached, VREF must always be less than all other supply voltages.

   The voltage difference between any of VSS and VSSQ pins may not exceed 100mV.

   The above conditions apply between Ta and power-off (controlled or uncontrolled).

   Tb is the point when all supply and reference voltages are within their respective min/max operating conditions.

   For supply and reference voltage operating conditions, See Table 2 on page 4.

   Power ramp duration tINIT0 (Tb - Ta) must be no greater than 20ms.

   Note: VDD2 is not present in some systems. Rules related to VDD2 in those cases do not apply.

2. CKE and clock
   Beginning at Tb, CKE must remain low for at least tINIT1 = 100 ns, after which it may be asserted high. Clock must be stable at least tINIT2 = 5 x tCK prior to the first low to high transition of CKE (Tc). CKE, /CS and CA inputs must observe setup and hold time (tIS, tIH) requirements with respect to the first rising clock edge (as well as to the subsequent falling and rising edges).

   The clock period shall be within the range defined for tCKb (18 ns to 100 ns), if any Mode Register Reads are performed. Mode Register Writes can be sent at normal clock operating frequencies so long as all AC Timings are met.. Furthermore, some AC parameters (e.g. tDQSCK) may have relaxed timings (e.g. tDQSCKb) before the system is appropriately configured.

   While keeping CKE high, issue NOP commands for at least tINIT3 = 200 μs. (Td).

3. Reset command
   After tINIT3 is satisfied, a MRW(Reset) command shall be issued (Td). The memory controller may optionally issue a Precharge-All command prior to the MRW Reset command. Wait for at least tINIT4 = 1 μs while keeping CKE asserted and issuing NOP commands.

4. Mode Registers Reads and Device Auto-Initialization (DAI) polling:
   After tINIT4 is satisfied (Te) only MRR commands and power-down entry/exit commands are allowed.
   Therefore, after Te, CKE may go low in accordance to Power-Down entry and exit specification.
   The MRR command may be used to poll the DAI-bit to acknowledge when Device Auto-Initialization is complete or the memory controller shall wait a minimum of tINIT5 before proceeding.
   As the memory output buffers are not properly configured yet, some AC parameters may have relaxed timings before the system is appropriately configured.
   After the DAI-bit (MR#0, “DAI”) is set to zero “DAI complete“ by the memory device, the device is in idle state (Tf). The state of the DAI status bit can be determined by an MRR command to MR#0.

   The DDR2 Mobile RAM will set the DAI-bit no later than tINIT5 (10 µs) after the Reset command.
   The memory controller shall wait a minimum of tINIT5 or until the DAI-bit is set before proceeding.
   After the DAI-Bit is set, it is recommended to determine the device type and other device characteristics by issuing MRR commands (MR0 “Device Information” etc.).

5. ZQ Calibration:
   After tINIT5 (Tf), an MRW ZQ Initialization Calibration command may be issued to the memory (see MR#10). This command is used to calibrate output drivers (RON) over process, voltage, and temperature. In system in which more than one DDR2 Mobile RAM Device exists on the same bus, the controller must not overlap ZQ Calibration commands. The device is ready for normal operation after tZQINIT.

6. Normal Operation:
   After tZQINIT (Tg), MRW commands may be used to properly configure the memory, for example the output buffer driver strength, latencies etc. Specifically, MR1, MR2, and MR3 shall be set to configure the memory for the target frequency and memory configuration.
   The DDR2 Mobile RAM Device will now be in IDLE state and ready for any valid command.
   After Tg, the clock frequency may be changed according to the clock frequency change procedure described in section “Input clock stop and frequency change during CKE low events” of “DDR2 Mobile RAM General Functionality and Electrical Condition” datasheet (E1354E).

Table 41 Timing Parameters for initialization

Symbol	min.	max.	Unit	Comment
tINIT0	—	20	ms	Maximum Power Ramp Time
tINIT1	100	—	ns	Minimum CKE low time after completion of power ramp
tINIT2	5	—	tCK	Minimum stable clock before first CKE high
tINIT3	200	—	µs	Minimum Idle time after first CKE assertion
tINIT4	1	—	µs	Minimum Idle time after Reset command
tINIT5	—	10	µs	Maximum duration of Device Auto-Initialization
tZQINIT	1	—	µs	ZQ Initial Calibration
tCKb	18	100	ns	Clock cycle time during boot

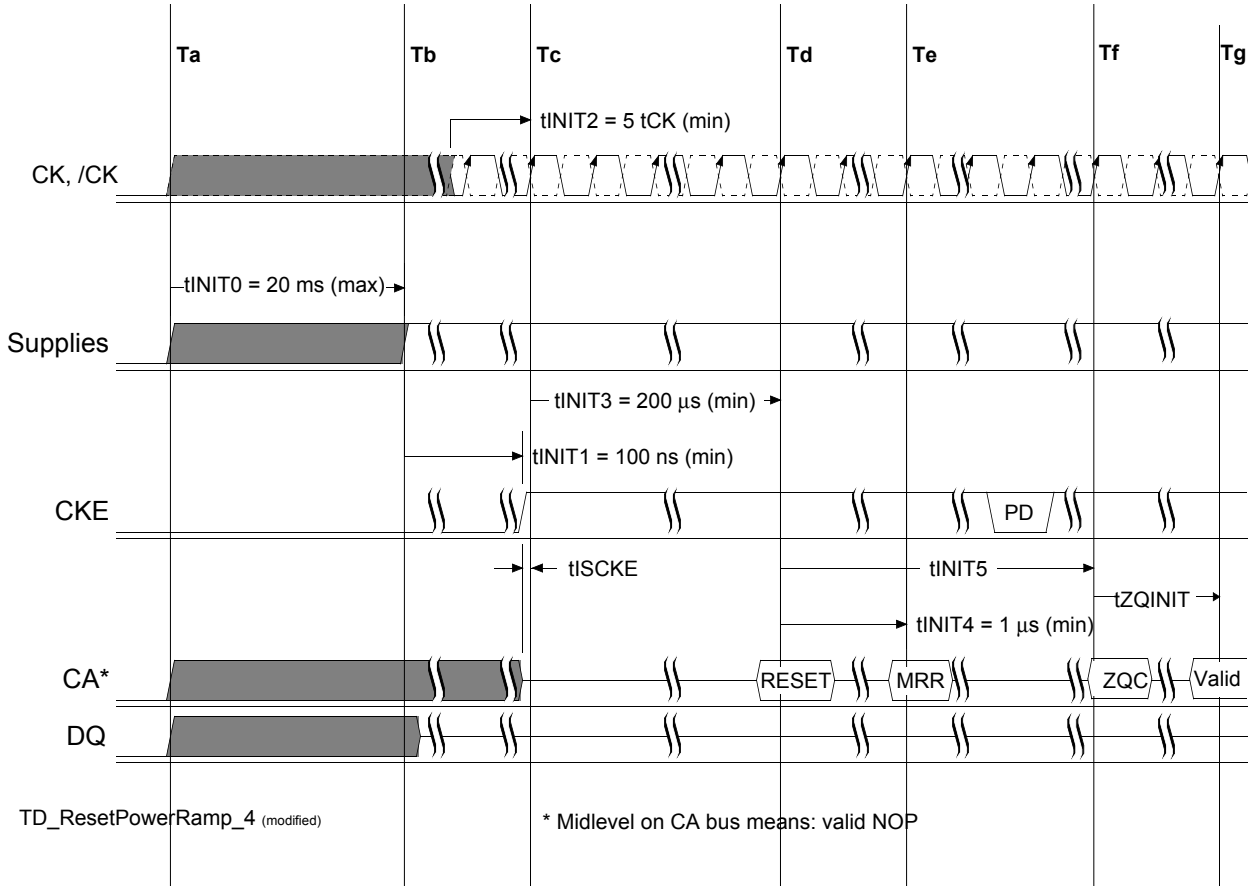


Figure 23 — Power Ramp and Initialization Sequence

7.1.1 Initialization after Reset (without Power Ramp):

If the RESET command is issued outside the power-up initialization sequence, the reinitialization procedure shall begin with step 3 (Td).

7.1.2 Power-Off Sequence

The following sequence shall be used to power-off the DDR2 Mobile RAM Device. Unless specified otherwise, these steps are mandatory.

While removing power, CKE shall be held at a logic low level (≤ 0.2 × VDD2), all other inputs shall be between VILmin and VIHmax. The DDR2 Mobile RAM Device will only guarantee that outputs are in a high impedance state while CKE is held low.

DQ, DM, DQS and /DQS voltage levels must be between VSSQ and VDDQ during power-off sequence to avoid latch-up.

CK, /CK, /CS and CA input levels must be between VSS and VDD2 during power-off sequence to avoid latch-up.

Tx is the point where any power supply decreases under its minimum value specified in the DC operating condition table.

Tz is the point where all power supplies are below 300mV. After Tz, the device is powered off.

The time between Tx and Tz (tPOFF) shall be less than 2s.

The following conditions apply:

Between Tx and Tz, VDD1 must be greater than VDD2 - 200mV.

Between Tx and Tz, VDD1 and VDD2 must be greater than VDDQ - 200mV.

Between Tx and Tz, VREF must always be less than all other supply voltages.

The voltage difference between any of VSS and VSSQ pins may not exceed 100mV.

For supply and reference voltage operating conditions, See Table 2 on page 4.

Table 42 Timing Parameters for Power-Off

Symbol	min.	max.	Unit	Comment
tPOFF	—	2	s	Maximum Power-Off ramp time

7.1.3 Uncontrolled Power-Off Sequence

The following sequence shall be used to power-off the DDR2 Mobile RAM Device under uncontrolled condition. Unless specified otherwise, these steps are mandatory.

Tx is the point where any power supply decreases under its minimum value specified in the DC operating condition table. After turning off all power supplies, any power supply current capacity must be zero.

Tz is the point where all power supply first reaches 300mV. After Tz, the device is powered off.

The time between Tx and Tz (tPOFF) shall be less than 2s. The relative level between supply voltages are uncontrolled during this period.

VDD1 and VDD2 shall decrease with a slope lower than 0.5V/usec between Tx and Tz.

Uncontrolled power-off sequence can be applied only up to 400 times in the life of the device.

8. Mode Register Definition

Table 43 shows the mode registers for DDR2 Mobile RAM.
Each register is denoted as “R” if it can be read but not written and “W” if it can be written but not read. Mode Register Read command shall be used to read a register. Mode Register Write command shall be used to write a register.

Table 43 Mode Register Assignment

MR#	MA <7:0>	Function	Acc-ess	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	Link
0	00H	Device Info.	R	(RFU)			RZQI		(RFU)	DI	DAI	MR#0
1	01H	Device Feature 1	W	nWR (for AP)			WC	BT	BL			MR#1
2	02H	Device Feature 2	W	(RFU)				RL & WL				MR#2
3	03H	I/O Config-1	W	(RFU)				DS				MR#3
4	04H	Refresh Rate	R	TUF	(RFU)				Refresh Rate			MR#4
5	05H	Basic Config-1	R	Manufacturer ID								MR#5
6	06H	Basic Config-2	R	Revision ID1 (Die Revision)								MR#6
7	07H	Basic Config-3	R	Revision ID2 (RFU)								MR#7
8	08H	Basic Config-4	R	I/O width		Density				Type		MR#8
9	09H	Test Mode	W	Vendor-Specific Test Mode								
10	0AH	IO Calibration	W	Calibration Code								MR#10
11:15	0BH~0FH	(Reserved)		(RFU)								
16	10H	PASR_Bank	W	Bank Mask								MR#16
17	11H	PASR_Seg	W	Segment Mask								MR#17
18:19	12H~13H	(Reserved)		(RFU)								
32	20H	DQ Calibration Pattern A	R	See “DQ Calibration” of “DDR2 Mobile RAM General Functionality and Electrical Condition” datasheet (E1354E).								MR#32
33:39	21H~27H	(Do Not Use)										
40	28H	DQ Calibration Pattern B	R	See “DQ Calibration” of “DDR2 Mobile RAM General Functionality and Electrical Condition” datasheet (E1354E).								MR#40
41:47	29H~2FH	(Do Not Use)										
48:62	30H~3EH	(Reserved)		(RFU)								
63	3FH	Reset	W	X								MR#63
64:126	40H~7EH	(Reserved)		(RFU)								
127	7FH	(Do Not Use)										
128:190	80H~BEH	(Reserved)		(RFU)								
191	BFH	(Do Not Use)										
192:254	C0H~FEH	(Reserved)		(RFU)								
255	FFH	(Do Not Use)										

Notes 1: RFU bits shall be set to ‘0’ during Mode Register writes.
2: RFU bits shall be read as ‘0’ during Mode Register reads.
3: All Mode Registers that are specified as RFU or write-only shall return undefined data when read and DQS, /DQS shall be toggled.
4: All Mode Registers that are specified as RFU shall not be written.
5: Writes to read-only registers shall have no impact on the functionality of the device.

MR#0_Device Information (MA<7:0> = 00H): Read-only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)			RZQI		(RFU)	DI	DAI

OP<0>	DAI (Device Auto-Initialization Status) 0B: DAI complete 1B: DAI still in progress
OP<1>	DI (Device Information) 0B: DDR2 Mobile RAM
OP<4:3>	RZQI (Built in Self Test for RZQ Information) 01B: ZQ-pin may connect to VDD2 or float 10B: ZQ-pin may short to GND 11B: ZQ-pin self test completed, no error condition detected (ZQ-pin may not connect to VDD or float nor short to GND)

Notes: 1. DDR2 Mobile RAM will not implement DNV functionality.
2. RZQI will be set upon completion of the MRW ZQ Initialization Calibration command.
3. If ZQ is connected to VDD2 to set default calibration, OP[4:3] shall be set to 01. If ZQ is not connected to VDD2, either OP[4:3]=01 or OP[4:3]=10 might indicate a ZQ-pin assembly error. It is recommended that the assembly error is corrected.
4. In the case of possible assembly error (either OP[4:3]=01 or OP[4:3]=10 per Note 3), the LPDDR2 device will default to factory trim settings for RON, and will ignore ZQ calibration commands. In either case, the system may not function as intended.
5. In the case of the ZQ self-test returning a value of 11b, this result indicates that the device has detected a resistor connection to the ZQ pin. However, this result cannot be used to validate the ZQ resistor value or that the ZQ resistor tolerance meets the specified limits (i.e. 240Ω ± 1%).

MR#1_Device Feature 1 (MA<7:0> = 01H): Write-only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
nWR (for AP)			WC	BT	BL		

OP<2:0>	BL 010B: BL4 (default) 011B: BL8 100B: BL16 All others: Reserved
OP<3>	BT 0B: Sequential (default) 1B: Interleaved
OP<4>	WC 0B: Wrap (default) 1B: No wrap (allowed for BL4 only)
OP<7:5>	nWR 001B: nWR=3 (default) 010B: nWR=4 011B: nWR=5 100B: nWR=6 101B: nWR=7 110B: nWR=8 All others: Reserved

Notes: 1. BL 16, interleaved is not an official combination to be supported.
2. Programmed value in nWR register is the number of clock cycles which determines when to start internal precharge operation for a write burst with AP enabled. It is determined by RU(tWR/tCK).

Table 44 Burst Sequence by BL, BT, and WC

C3	C2	C1	C0	WC	BT	BL	Burst Cycle Number and Burst Address Sequence															
							1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
X	X	0B	0B	wrap	any	4	0	1	2	3												
X	X	1B	0B				2	3	0	1												
X	X	X	0B	nw	any		y	y+1	y+2	y+3												
X	0B	0B	0B	wrap	seq	8	0	1	2	3	4	5	6	7								
X	0B	1B	0B				2	3	4	5	6	7	0	1								
X	1B	0B	0B				4	5	6	7	0	1	2	3								
X	1B	1B	0B				6	7	0	1	2	3	4	5								
X	0B	0B	0B		int		0	1	2	3	4	5	6	7								
X	0B	1B	0B				2	3	0	1	6	7	4	5								
X	1B	0B	0B				4	5	6	7	0	1	2	3								
X	1B	1B	0B				6	7	4	5	2	3	0	1								
X	X	X	0B	nw	any		illegal (not allowed)															
0B	0B	0B	0B	wrap	seq	16	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0B	0B	1B	0B				2	3	4	5	6	7	8	9	A	B	C	D	E	F	0	1
0B	1B	0B	0B				4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3
0B	1B	1B	0B				6	7	8	9	A	B	C	D	E	F	0	1	2	3	4	5
1B	0B	0B	0B				8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7
1B	0B	1B	0B				A	B	C	D	E	F	0	1	2	3	4	5	6	7	8	9
1B	1B	0B	0B				C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B
1B	1B	1B	0B				E	F	0	1	2	3	4	5	6	7	8	9	A	B	C	D
X	X	X	0B		int		illegal (not allowed)															
X	X	X	0B	nw	any		illegal (not allowed)															

Notes: 1. C0 input is not present on CA bus. It is implied zero.

2. For BL=4, the burst address represents C1 - C0.
3. For BL=8, the burst address represents C2 - C0.
4. For BL=16, the burst address represents C3 - C0.
5. For no-wrap (nw), BL4, the burst shall not cross the page boundary and shall not cross sub-page boundary. The variable y may start at any address with C0 equal to 0 and may not start at any address in Table 45 below for the respective density and bus width combinations.

Table 45 Non Wrap Restrictions

Not across full page boundary	x16	3FE, 3FF, 000, 001
	x32	1FE, 1FF, 000, 001
Not across sub page boundary	x16	1FE, 1FF, 200, 201
	x32	None

Note: 1. Non-wrap BL=4 data-orders shown above are prohibited.

MR#2_Device Feature 2 (MA<7:0> = 02H): Write-only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)				RL & WL			

OP<3:0>	RL & WL 0001B: RL3 / WL1(default) 0010B: RL4 / WL2 0011B: RL5 / WL2 0100B: RL6 / WL3 0101B: RL7 / WL4 0110B: RL8 / WL4 All others: Reserved

MR#3_I/O Configuration 1 (MA<7:0> = 03H): Write-only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)				DS			

OP<3:0>	DS 0000B: Reserved 0001B: 34.3 Ω typ. 0010B: 40 Ω typ. (default) 0011B: 48 Ω typ. 0100B: 60 Ω typ. 0101B: Reserved 0110B: 80 Ω typ. 0111B: 120 Ω typ. All others: Reserved

MR#4_Device Temperature (MA<7:0> = 04H): Read-only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
TUF	(RFU)				Refresh Rate		

OP<2:0>	Refresh Rate 000B: Low temperature operating limit exceeded 001B: 4× tREFI, 4× tREFIpb, 4× tREFW 010B: 2× tREFI, 2× tREFIpb, 2× tREFW 011B: 1× tREFI, 1× tREFIpb, 1× tREFW(≤ +85°C) 100B: RFU 101B: 0.25× tREFI, 0.25× tREFIpb, 0.25× tREFW, do not de-rate AC timing 110B: 0.25× tREFI, 0.25× tREFIpb, 0.25× tREFW, de-rate AC timing 111B: High temperature operating limit exceeded
OP<7>	TUF(Temperature Update Flag) 0B: OP<2:0> value has not changed since last read of MR4. 1B: OP<2:0> value has changed since last read of MR4.

Notes: 1. A Mode Register Read from MR4 will reset OP7 to ‘0’.
2. OP7 is reset to ‘0’ at power-up. OP<2:0> bits are undefined after power-up.
3. If OP2 equals ‘1’, the device temperature is greater than 85°C.
4. OP7 is set to “1” if OP2:OP0 has changed at any time since the last read of MR4.
5. DDR2 Mobile RAM will drive OP<6:5> to ‘0’.
6. Specified operating temperature range and maximum operating temperature are refer to “Electrical Conditions” on page 4. If maximum temperature is 85°C, functionality for over 85°C is not guaranteed.

MR#5_Basic Configuration 1 (MA<7:0> = 05H): Read-only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Manufacturer ID							

OP<7:0>	Manufacturer ID 00000011B

MR#6_Basic Configuration 2 (MA<7:0> = 06H): Read-only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID1(Die Revision)							

OP<7:0>	Revision ID1 (Die Revision) 00000001B: B-version

MR#7_Basic Configuration 3 (MA<7:0> = 07H): Read-only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID2 (RFU)							

OP<7:0>	Revision ID2 (RFU) 00000000B: Default Value

MR#8_Basic Configuration 4 (MA<7:0> = 08BH): Read-only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
I/O width		Density				Type	

OP<1:0>	Type 00B: S4 Device
OP<5:2>	Density 0101B: 4Gb
OP<7:6>	I/O width 00B: ×32 01B: ×16

MR#10_Calibration (MA<7:0> = 0AH): Write-only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Calibration Code							

OP<7:0>	Calibration Code 0xFF: Calibration command after initialization 0xAB: Long calibration 0x56: Short calibration 0xC3: ZQ Reset others: Reserved

Notes: 1. Host processor shall not write MR10 with “Reserved” values.
2. DDR2 Mobile RAM Devices shall ignore calibration command when a “Reserved” value is written into MR10.
3. See AC timing table for the calibration latency.
4. If ZQ is connected to VSS through RZQ, either the ZQ calibration function (see “Mode Register Write ZQ Calibration Command” of “DDR2 Mobile RAM General Functionality and Electrical Condition” datasheet (E1354E).) or default calibration (through the ZQreset command) is supported. If ZQ is connected to VDD2, the device operates with default calibration, and ZQ calibration commands are ignored. In both cases, the ZQ connection shall not change after power is applied to the device.

MR#16_PASR_Bank Mask (MA<7:0> = 010H): Write-only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Bank Mask							

OP<7:0>

Bank Mask
0B: refresh enable to the bank (=unmasked, default)
1B: refresh blocked (=masked)

Bank and OP corresponding table

OP<7:0>	Bank	
	Bank #	Bank Address
OP0	Bank 0	000B
OP1	Bank 1	001B
OP2	Bank 2	010B
OP3	Bank 3	011B
OP4	Bank 4	100B
OP5	Bank 5	101B
OP6	Bank 6	110B
OP7	Bank 7	111B

Note: 1. Each bank can be masked independently by setting each OP value.

MR#17_PASR_Segment Mask (MA<7:0> = 0H): Write-only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Segment Mask							

OP<7:0>

Segment
0B: refresh enable to the segment (=unmasked, default)
1B: refresh blocked (=masked)

Segment and OP corresponding table

OP<7:0>	Segment	
	Segment #	Row Address (R13:11)
OP0	Segment 0	000B
OP1	Segment 1	001B
OP2	Segment 2	010B
OP3	Segment 3	011B
OP4	Segment 4	100B
OP5	Segment 5	101B
OP6	Segment 6	110B
OP7	Segment 7	111B

Note: 1. Each segment can be masked independently by setting each OP value.

MR#32_DQ Calibration Pattern A (MA<7:0> = 20H):

Reads to MR32 return DQ Calibration Pattern “A”. See “DDR2 Mobile RAM General Functionality and Electrical Condition” datasheet (E1354E).

MR#40_DQ Calibration Pattern B (MA<7:0> = 28H):

Reads to MR40 return DQ Calibration Pattern “B”. See “DDR2 Mobile RAM General Functionality and Electrical Condition” datasheet (E1354E).

MR#63_Reset (MA<7:0> = 3FH): MRW only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
X							

Note: 1. For additonal information on MRW RESET see “DDR2 Mobile RAM General Functionality and Electrical Condition” datasheet (E1354E).

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR MOS DEVICES

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.