Semi Conductor and electronic devices

Learn

Metals → $\rho = 10^{-2}$ to 10^{-8} Ωm
→ $\sigma = \frac{1}{\rho}$ (10^{2} to 10^{8} Sm) (high conductivity)

Semi-Conductor → $\rho = 10^{-2}$ to 10^{6} Ωm
→ $\sigma = 10^{2}$ to 10^{-6} Sm

$\rho = \frac{1}{\sigma}$

Insulators → $\rho = 10^{11} - 10^{19}$ Ωm
$\sigma = 10^{-11} - 10^{-19}$ Ωm. (low conductivity)

Energy Band Theory

$\Delta E_g = (CB)_{min} - (VB)_{max}$

(ev)

** Temp ↑, ΔE_g ↓

atomic no.:-
Si : (14) → 2,8,4
Ge : (32) → 2,8,18,4

**
$\Delta E_g > 3$ ev (in insulators)
$\Delta E_g = 3$ ev (in semi conductors)
$\Delta E_g < 3$ ev (in metals)

NOTE:- Semi-conductor is formed by covalent Bonds.

Intrinsic Semi-conductor

$n_e = n_h$

$i = i_e + i_n$

Mass action law

$n_i^2 = n_e n_h$

where n_i is the intrinsic carrier conc.

$J = \sigma E$

$\mu = \frac{v_d}{E}$

$J = n e v_d$

$J = n_e e \mu_e E + n_h e \mu_h E$

$J = (n_e e \mu_e + n_h e \mu_h) E$

$\therefore \sigma = (n_e e \mu_e + n_h e \mu_h)$

NOTE:- Generally, $\mu_e > \mu_n$

N-Type Semiconductors

pentavalent impurity phosphorus

e^- in C.B → Majority Charge carriers

e^- in V.B → Minority Charge carriers

P-type Semiconductors

Trivalent impurity → Aluminium

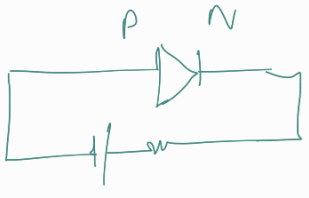
$n_h >> n_e$

* The intrinsic semi-conductor becomes insulator at 0 K.

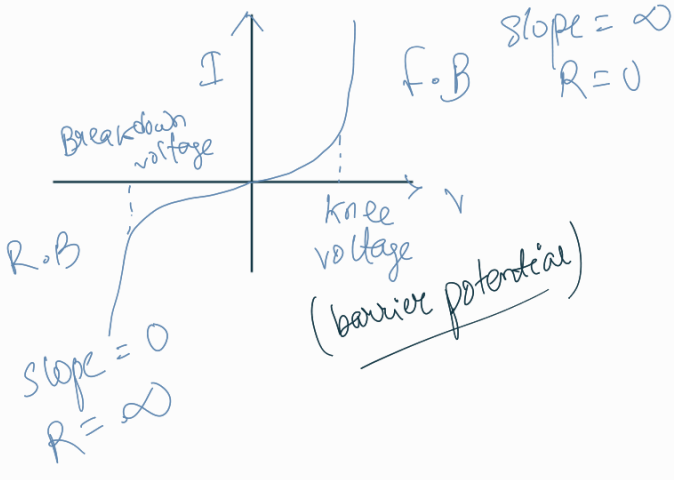
Intrinsic Semi-Conductor	N-Type	P-Type
$n_e = n_h$	$n_h >> n_e$	$n_e >> n_h$
$J = ne[V_e + V_h]$	$J = e n_h V_h$	$J = e n_e V_e$
$\sigma = en[\mu_e + \mu_h]$	$\sigma = e n_h \mu_h$	$\sigma = e n_e \mu_e$

Forward Bias

Reverse Bias



I-V Characteristics



NOTE

$\Delta V = 0.7$ (Si)

$\Delta V = 0.3$ (Ge)

Logic Gates

(1) OR Gate

$(A+B)$

Truth Table

A	B	R
0	0	0
0	1	1
1	0	1
1	1	1

(2) AND Gate

$(A \cdot B)$

Truth Table

A	B	R
0	0	0
0	1	0
1	0	0
1	1	1

(3) NOT Gate (Inverter Gate)

$\overline{A}$

(4) NOR

Inverter of OR

A	B	OR	NOR
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

$(\overline{A+B})$

NAND

Inverter of AND

A	B	AND	NAND
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

$(\overline{A \cdot B})$

(*) De Morgan's Theorem

(i) $\overline{A+B} = \overline{A} \cdot \overline{B}$

(ii) $\overline{A \cdot B} = \overline{A} + \overline{B}$

(5) XOR Gate (Exclusive OR gate)

⇒ output will be 1, only if both the inputs are different.

$A \oplus B$

(6) XNOR Gate (Exclusive NOR Gate)

⇒ output will be 1, only if both the inputs are same.

$\overline{A \oplus B}$