FAULT TESTING AND ANALYSIS OF DIGITAL CIRCUITS

ABSTRACT

Our project is to test 8 input and 8 output digital combinational circuits using FPGA and UART interfacing. It can be used to quickly verify any combinational circuit by giving the Boolean formula corresponding to the circuit under consideration. We provide easy to use interface for giving the inputs and observing the truth tables (using UART terminal).

The second part of the project demands exploring various possibilities for sequential circuit testing and comparing their performance. Several recent advancement in this field has been highlighted at the end.

INTRODUCTION (for combination circuit)

It can be very cumbersome to test the correctness of circuits (e.g. on breadboard) by manually changing the input combination one by one. Using this project we can simply give the Boolean formula for a circuit with 8 inputs and 8 outputs and observe the expected output and the actual output from circuit in form of truth table on the UART terminal. This can also be used to test faulty IC's.

PROJECT DESCRIPTION

PROJECT GOAL FOR COMBINATIONAL CIRCUITS

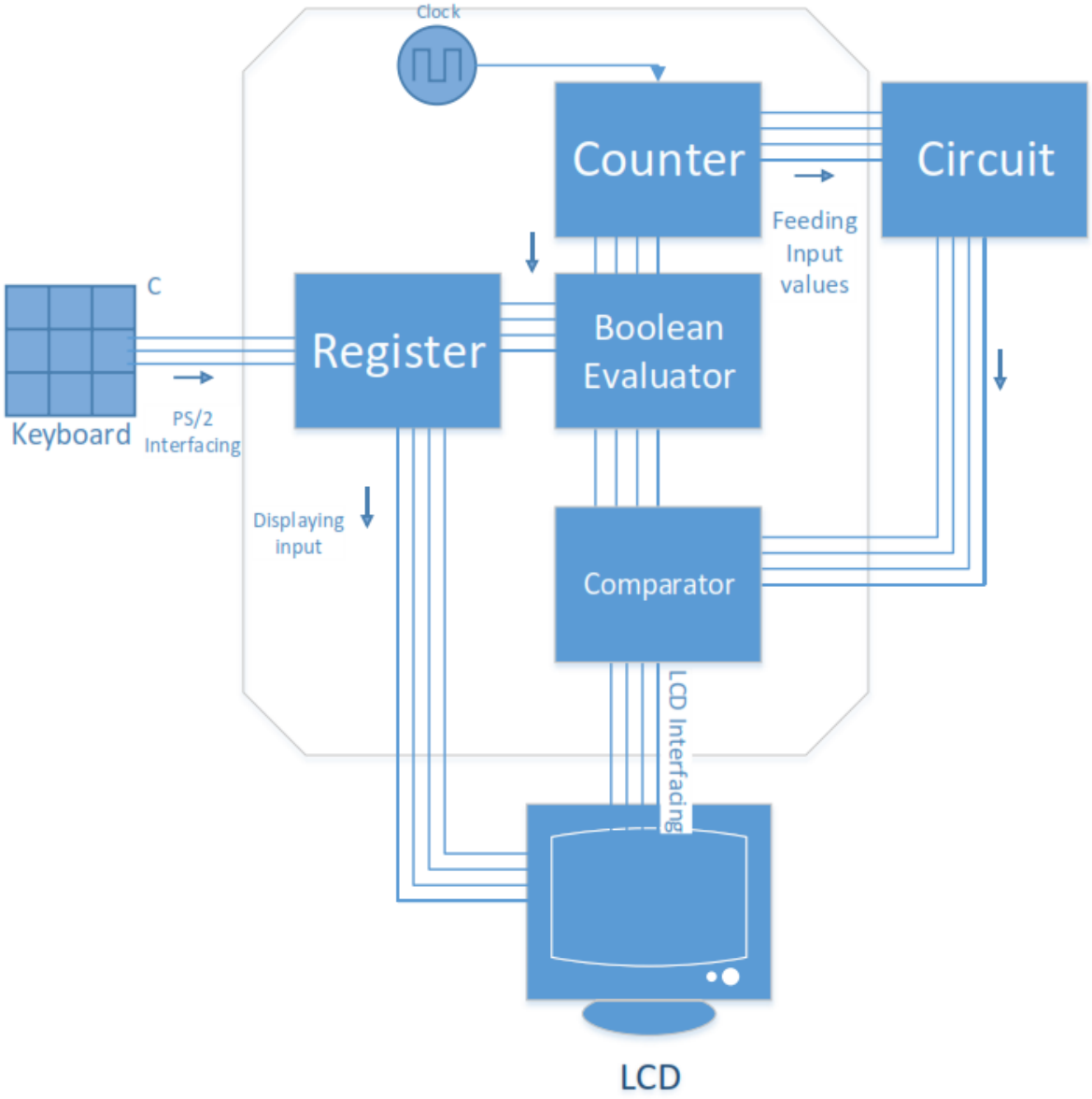
To test a combinational circuit, the user should connect the input and output pins of the circuit to specified pins on the FPGA board and open the UART terminal. When prompted for input, user should enter the no. of inputs, no. of outputs and the formula for each output separated by \. Q or q should be typed to end the input. For example, 2\1\~(A+B)\Q

The formula can have and (.), or (+), not (~), xor (*) and parenthesis '(' ,')' (the precedence order is described in the Boolean Evaluator section). The inputs should be specified as A,B…H.

The output is displayed in the form of Truth table, one for each output. In the truth table, the input combination (eg A=0,B=1 represented in form of integer), the expected output (evaluated by the Boolean Evaluator block) and the actual output from the circuit are displayed. Looking at this the user can easily find out errors, if any, in the circuit.

TECHNICAL DESIGN

BLOCK DIAGRAM



The input entered by the user (in format given above) is first parsed to get the no. of inputs etc. Then, for each output, each of the 2^n input combinations is applied to the circuit and to the Boolean evaluator block. After waiting for some clock cycles for the outputs to stabilize, the outputs are read and displayed on the UART terminal.

METHODS FOR TESTING SEQUENTIAL CIRCUITS

Fault Classification

- Single observation time
- Multiple observation time

depending upon whether a fault affects the overall circuit at a 'specified' time or 'some' time from start.

Various algorithms for fault analysis of sequential circuits

- *Scan chain*: scanning in set of input and output values and comparing them. This reduces the sequential test generation problem to that of a test generation for the combinational logic.

- *Checking experiments* (based on Synchronizing and Desynchronizing sequence to identify final state and initial state of a machine respectively)): The first part uses the synchronizing sequence or a reset input to transfer machine into a pre-specified state and the second part is a preset experiment in which the machine is taken through all possible transitions. The second part is further divided into dispaying the response of each of its state to the distinguishing sequence while in the second subpart the actual transitions are verified. This method is applicable to diagnosable sequential machine that possess one or more distinguishing sequences and thus permits us to identify uniquely the states of the machine. There are methods like testing graph that modify the design of sequential machine in such a way that they will possess special distinguishing sequence for which relatively short checking experiments are required.

- *State-table-based test generation:* This fault model assumes that the fault is associated with a state transition in the state table i.e. fault results in the destination state of a state transition becoming corrupted while retaining its correct input/output symbol (which is combinational).

- Some other methods include Extended D-algorithm, Built-in self test (by adding additional circuitry on integrated design)