



*Dipartimento di Ingegneria dell' Innovazione*

*Universita' degli Studi di Lecce*

*Andrea Baschirotto*

[andrea.baschirotto@unile.it](mailto:andrea.baschirotto@unile.it)

---

## **Analog Filters for Telecommunications**

*Universita' degli Studi di Bologna*

*June, 16<sup>th</sup>-17<sup>th</sup>, 2005*

## **Active-RC Filters**



# 1<sup>st</sup> order cell

## Filter Frequency Response

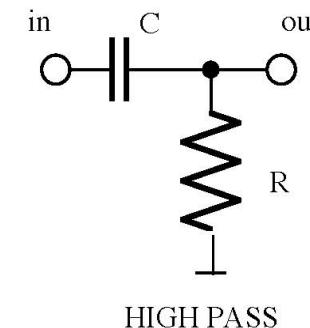
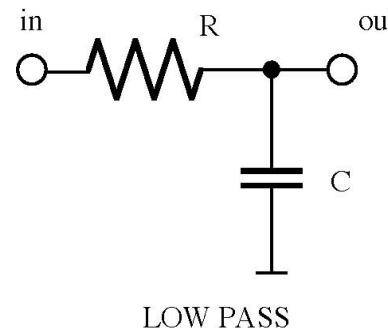
- First order cell

$$H(s) = A_o \cdot \frac{1 + s \cdot \tau_z}{1 + s \cdot \tau_p}$$

- Passive implementation
- Specific cases

$$H_{LP}(s) = \frac{1}{1 + s \cdot R \cdot C}$$

$$H_{HP}(s) = \frac{s \cdot R \cdot C}{1 + s \cdot R \cdot C}$$

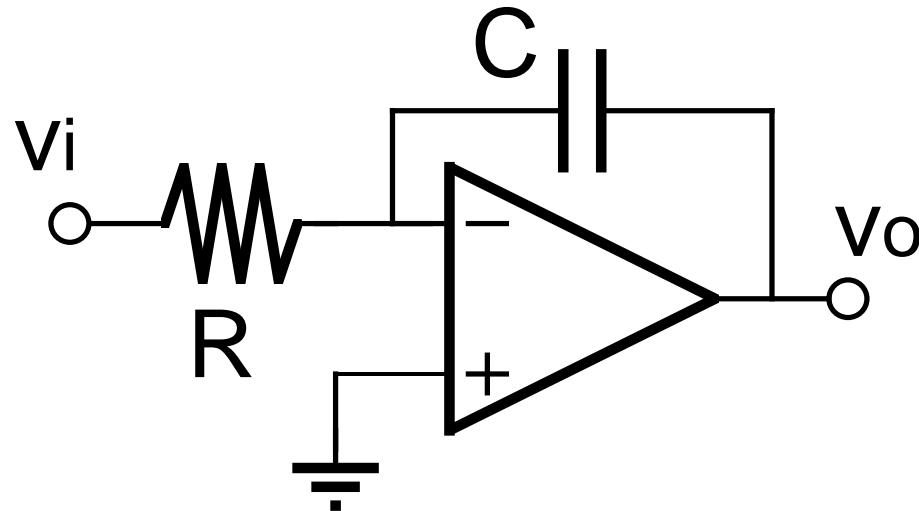


- Zero power consumption
- Non-zero output impedance
- Useful for infinite input impedance block to be fed by this filtering stage



# Active-RC Filters

Basic building block: The integrator



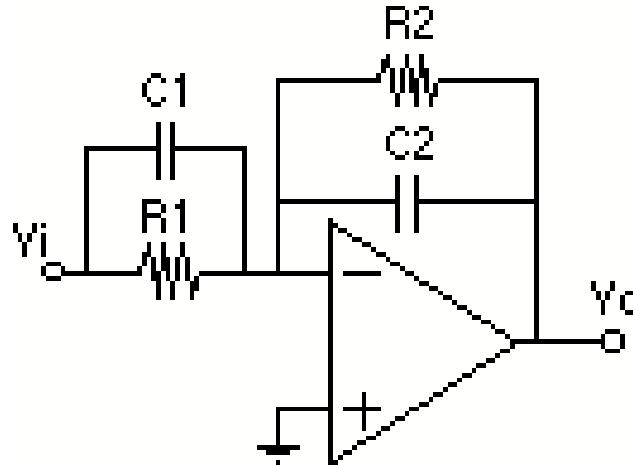
$$H(s) = -\frac{1}{s \cdot R \cdot C}$$

- The building block for ladder structures



# Active-RC Filters

## 1<sup>st</sup> order cell: Filter Frequency Response



$$H(s) = -\frac{R_2}{R_1} \cdot \frac{1 + s \cdot R_1 \cdot C_1}{1 + s \cdot R_2 \cdot C_2}$$

- The ratio  $R_2/R_1$  defines the dc-gain
- Their absolute values are defined by other parameters (noise, dynamics, etc ....)
- Non-zero power consumption due to the opamp
- Zero output impedance
- Output load (of following stages) can be driven



## 2<sup>nd</sup> order cell (Biquadratic) cell

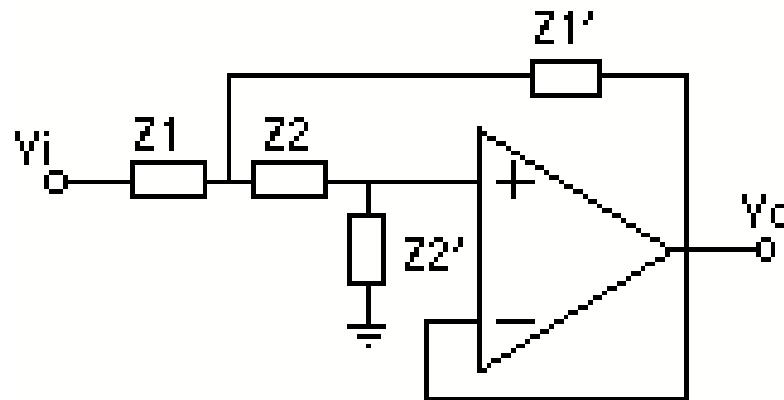
$$H(s) = \frac{(s^2 + s \cdot \omega_{z1} / Q_{z1} + \omega_{z1}^2)}{(s^2 + s \cdot \omega_{p1} / Q_{p1} + \omega_{p1}^2)}$$

- Complex poles/zeros are present
  - A passive RC implementation is not possible (a regenerative loop is need to have complex poles)
- Possible Active-RC implementations
  - Single-Opamp Biquad
    - Sallen&Key Biquadratic cell
    - Rauch Biquadratic cell
  - Multi-Opamp Biquad
    - Kerwin-Huelsman-Newcomb (KHN) Biquadratic cell
    - Tow-Thomas Biquadratic cell



# Single-Opamp Biquad

Sallen&Key Biquadratic cell



$$H(s) = \frac{V_o}{V_i} = \frac{Z_1 \cdot Z_2}{(Z_1 + Z_2 + Z_2') \cdot Z_1 + Z_1 \cdot Z_2}$$

- The opamp is in a buffer configuration
- The opamp output swing is present at the opamp input nodes
  - ⌚ The input stage may be critical

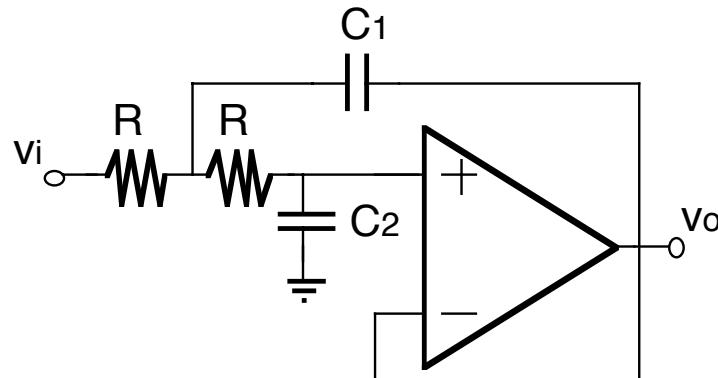


# Single-Opamp Biquad

## Sallen&Key Biquadratic cell

- Low-pass frequency response

$$Z_1 = Z_2 = R$$



$$Z_1' = \frac{1}{s C_1}$$

$$Z_2' = \frac{1}{s C_2}$$

$$H(s) = \frac{1}{1 + 2 \cdot R \cdot C_2 \cdot s + R^2 \cdot C_1 \cdot C_2 \cdot s^2}$$

$$\omega_o = \frac{1}{\sqrt{C_1 \cdot C_2} \cdot R}$$

$$C_1 = \frac{\sqrt{2} \cdot Q}{R \cdot \omega_o}$$

$$Q = \frac{1}{2} \cdot \sqrt{\frac{C_1}{C_2}}$$

$$C_2 = \frac{1}{\sqrt{2} \cdot Q \cdot R \cdot \omega_o}$$

- In-band maximally-flat frequency response for ( $Q = \sqrt{2}/2$ )

$$C_1 = 2 \cdot C_2$$

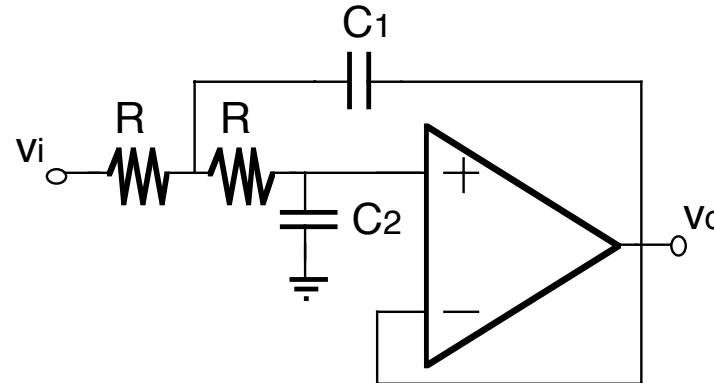
$$f_p = \frac{1}{2 \cdot \pi} \cdot \frac{1}{\sqrt{2} \cdot R \cdot C}$$



# Single-Opamp Biquad

## Sallen&Key biquad

- Noise performance



$$\overline{V_{n\_out}^2} = \frac{2 \cdot 4 \cdot k \cdot T \cdot R + V_{n\_opamp}^2}{}$$

- Linearity performance

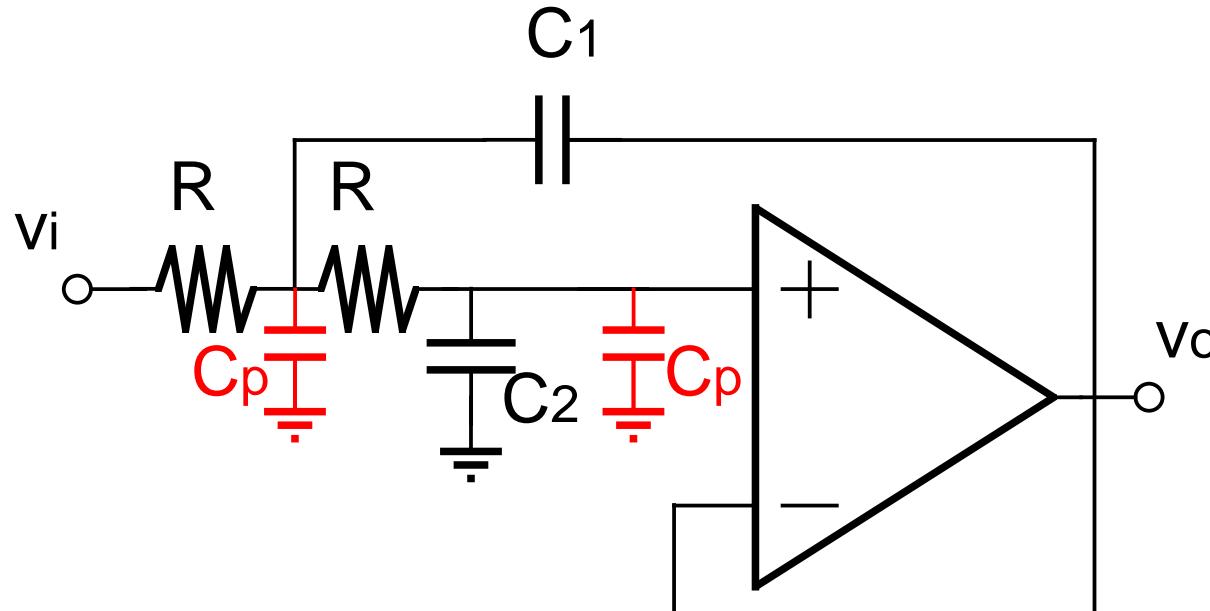
- Good linearity for closed loop configuration
- For out-of-band signal a  $2 \cdot R \cdot C_2$  prefilter increases out-of-band linearity



# Single-Opamp Biquad

Sallen&Key biquad

- Parasitic capacitance sensitivity



- The transfer function is affected by the parasitic capacitance at the two nodes

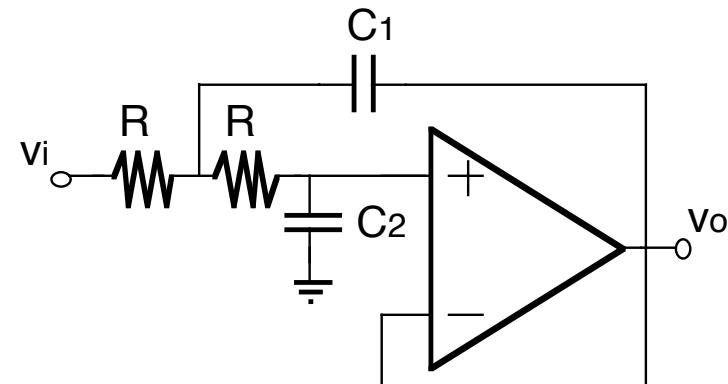


# Single-Opamp Biquad

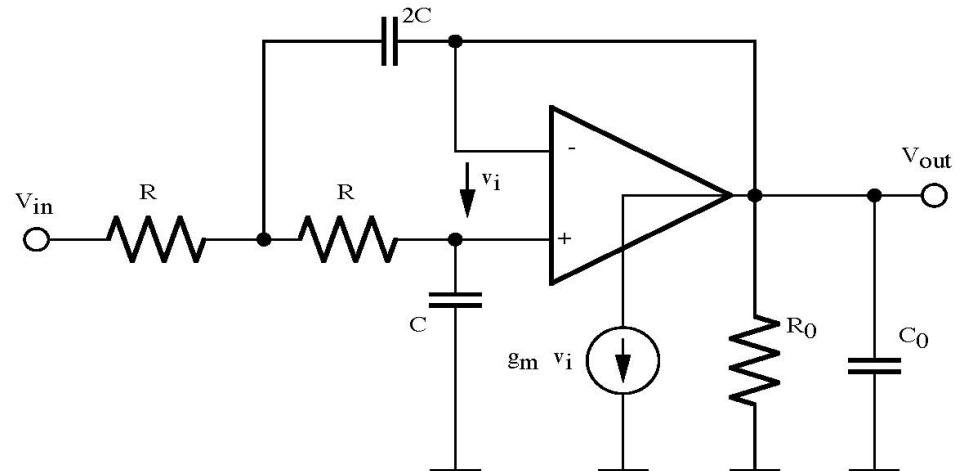
## Sallen&Key Biquadratic cell

- Lowpass configuration: Design issue

😊 In the passband no current flows on the resistances (even if they are non linear, non harmonic distortion results).

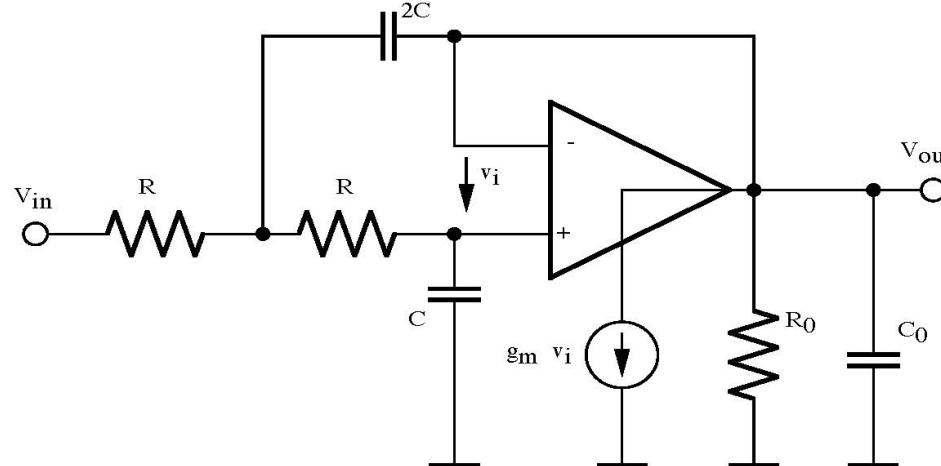


- Low pass Sallen and Key filter with real op-amp:
- A real op-amp used in CMOS monolithic S&K filter is a transconductance op-amp



# Single-Opamp Biquad

## Sallen&Key Biquadratic cell



$$H(s) = \frac{1 + 2 \cdot s \cdot \frac{C}{g_m} + 2 \cdot s^2 \cdot R \cdot \frac{C^2}{g_m}}{\alpha + s \cdot \beta + s^2 \cdot \gamma + s^2 \cdot \delta}$$

$$\alpha = 1 + \frac{1}{A_0} \quad \beta = 2RC + \frac{R_0C_0 + 2R_0C + 4RC}{A_0}$$

$$\gamma = 2R^2C^2 + \frac{1}{A_0}(4RR_0C(C + C_0) + 2R^2C^2) \quad \delta = 2 \cdot \frac{R^2C^2}{C_0} g_m \quad A_0 = g_m R_0$$

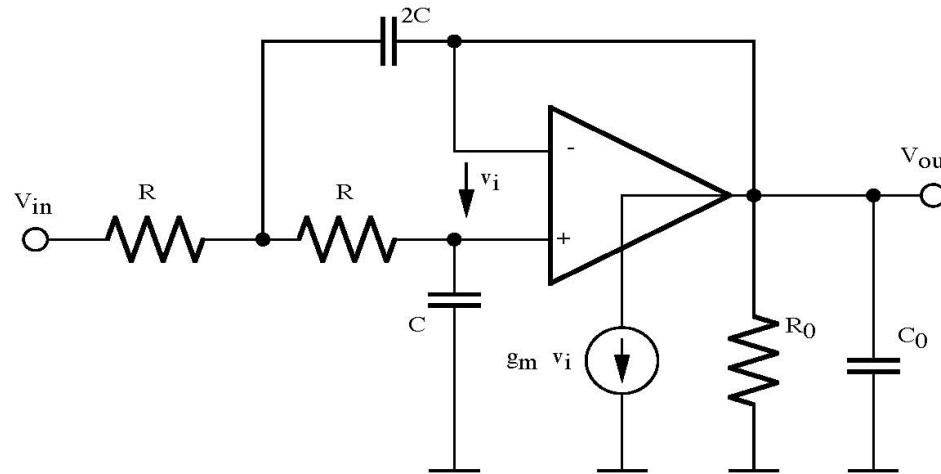
- The real transfer function has two zeros and three poles



# Single-Opamp Biquad

## Sallen&Key Biquadratic cell

- Lowpass configuration: Design issue



- The real transfer function has two zeros and three poles
- If  $k = R \cdot g_m \gg 1$  the zeros are practically complex conjugates and are located at

$$\omega_0 = \sqrt{\frac{g_m}{2 \cdot R \cdot C^2}} = \omega_p \cdot \sqrt{k}$$

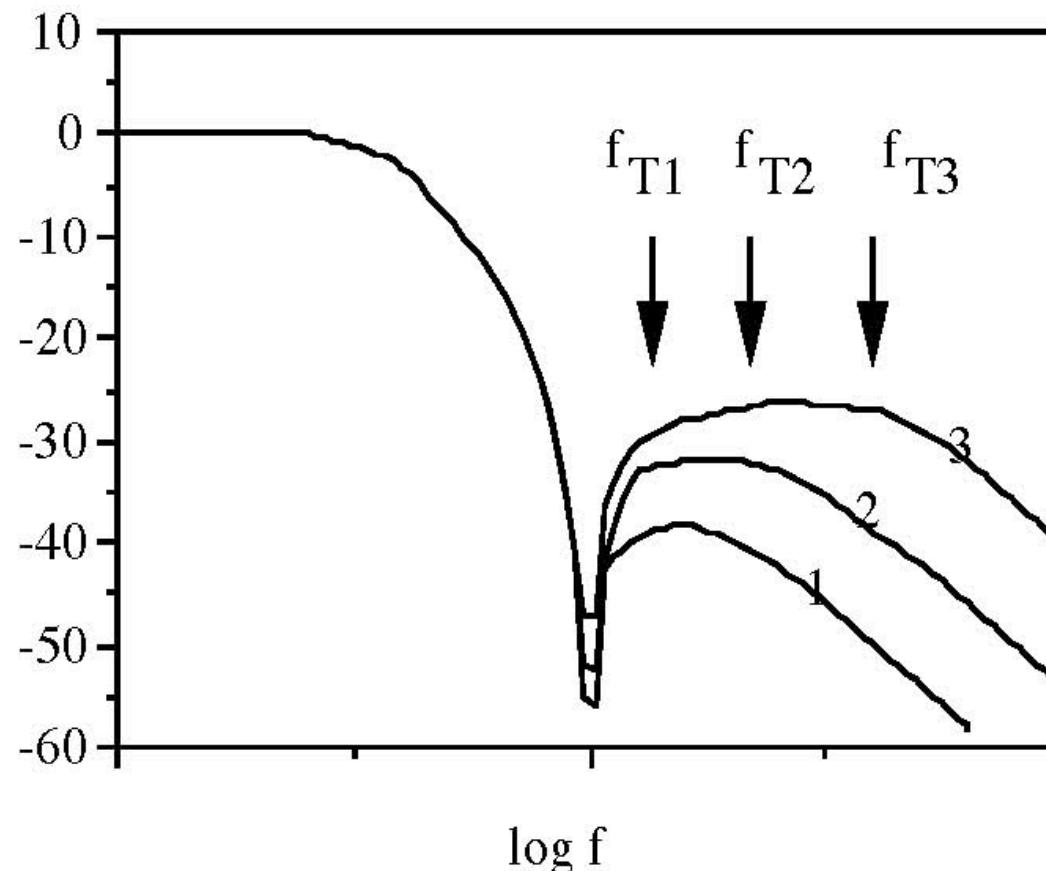
- The extra-pole is real and is located around the GBW of the op-amp



# Single-Opamp Biquad

## Sallen&Key Biquadratic cell

- Lowpass configuration: Opamp GBW effect



$$1: f_T/f_p = 100$$

$$2: f_T/f_p = 20$$

$$3: f_T/f_p = 4$$

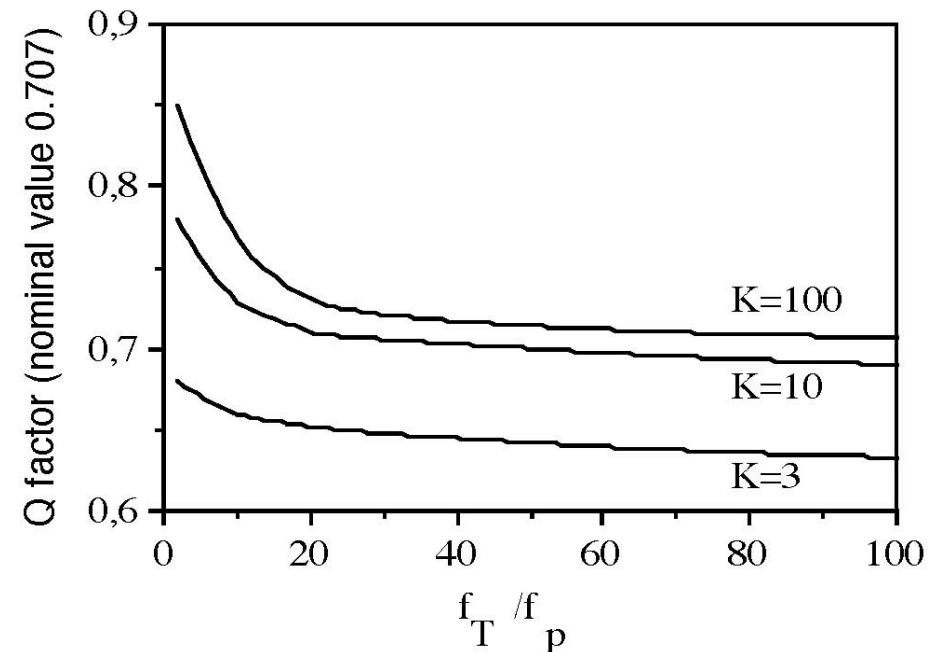
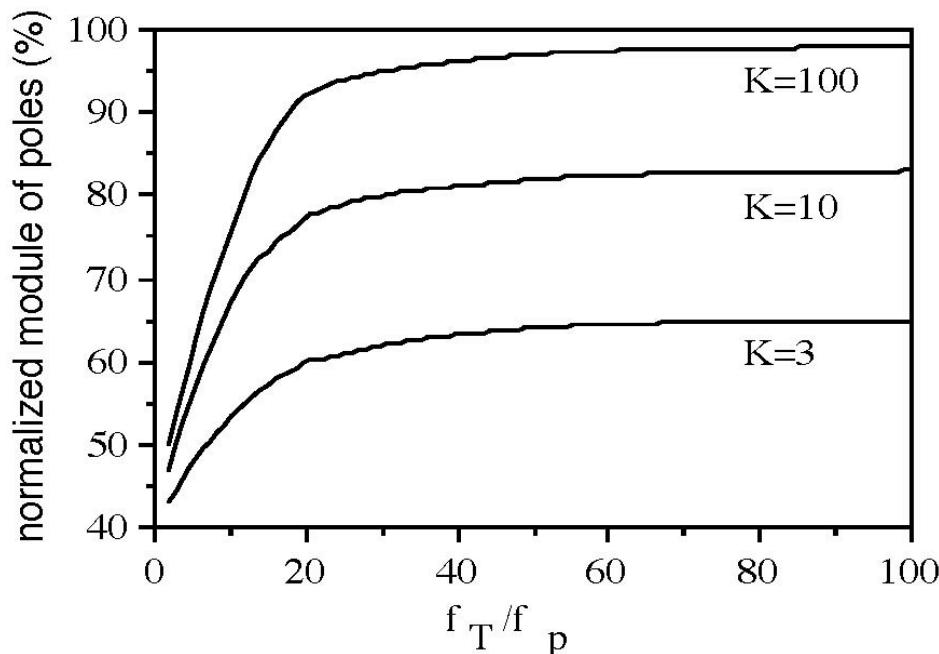
$$K = 40$$



# Single-Opamp Biquad

## Sallen&Key Biquadratic cell

- A low value of  $k=R \cdot g_m$  determines a shift of the poles of the S&K filter with respect to the designed position



- Design criteria

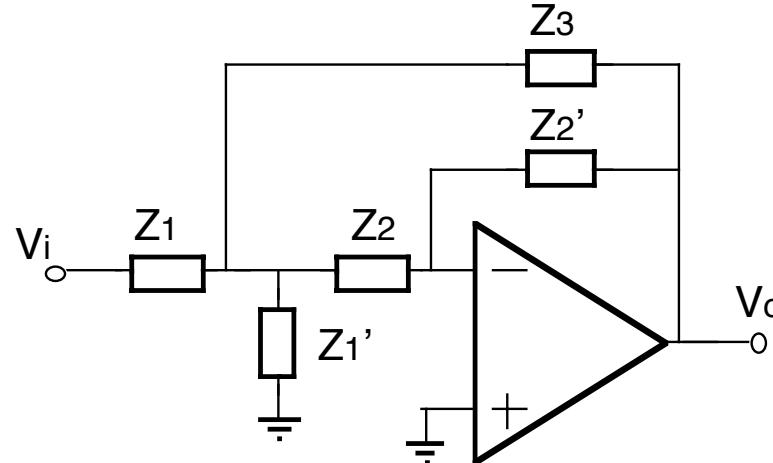
Use an op-amp with  $f_T > 20 \cdot f_0$

Use resistances  $R > 40/g_m$



# Single-Opamp Biquad

## Rauch Biquadratic cell



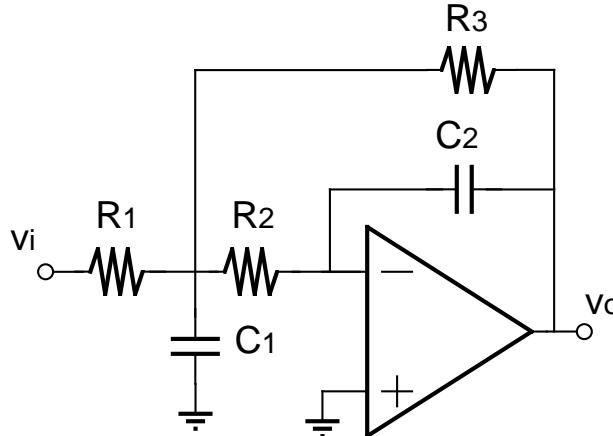
$$H(s) = \frac{V_o(s)}{V_i(s)} = -\frac{1}{\frac{Z_1}{Z_3} + \frac{Z_2}{Z_2'} \cdot \left(1 + \frac{Z_1}{Z_1'} + \frac{Z_1}{Z_2} + \frac{Z_1}{Z_3}\right)}$$

- The two opamp input nodes are at ground
  - 😊 No swing is present at the opamp input nodes
- Any parasitic impedance at node X ( $Z_{px}$ ) is in parallel with  $Z_1'$  which has to be replaced by  $Z_1' // Z_{px}$ 
  - 😢 A frequency response deviation is possible



# Rauch Biquadratic cell

## Lowpass Frequency Response



$$Z_1 = R_1$$

$$Z_2 = R_2$$

$$Z_3 = R_3$$

$$Z_1' = 1/s \cdot C_1$$

$$Z_2' = 1/s \cdot C_2$$

- In the passband, a current flows into the resistors

$$H(s) = \frac{1}{s^2 \cdot R_1 \cdot R_2 \cdot C_1 \cdot C_2 + s \cdot C_2 \cdot \left( R_1 + R_2 + \frac{R_1 \cdot R_2}{R_3} \right) + \frac{R_1}{R_3}}$$

- For an in-band maximally flat frequency response ( $Q = \sqrt{2}/2$ )

$$R_1 = R_3 = 2 \cdot R_2 = 2R$$

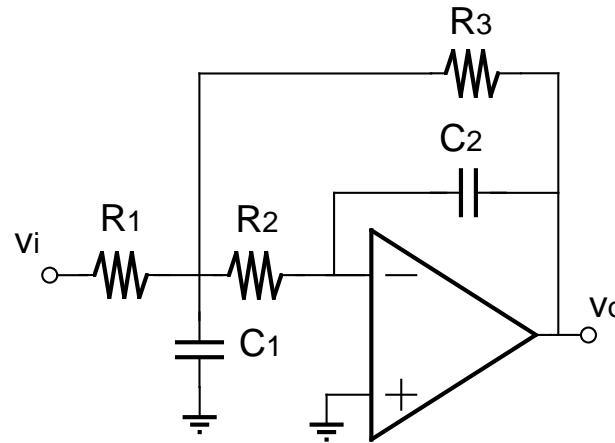
$$C_1 = 4 \cdot C_2 = 4C$$

$$f_o = 1/(4 \cdot \pi \cdot \sqrt{2} \cdot R \cdot C)$$

- The transfer function is sensitive to any parasitic capacitance in parallel at  $C_1$



# Rauch Biquadratic cell



- Noise Performance

$$\overline{V_{n\_out}^2} = 4 \cdot k \cdot T \cdot R_1 \cdot \left( \frac{R_3}{R_1} \right)^2 + 4 \cdot k \cdot T \cdot R_2 \cdot \left( 1 + \frac{R_3}{R_1} \right)^2 + 4 \cdot k \cdot T \cdot R_3 + \overline{V_{n\_opamp}^2} \cdot \left( 1 + \frac{R_3}{R_1} \right)^2$$

- Linearity performance

- Good linearity for closed loop configuration
- For out-of-band signal a  $R_1$ - $C_1$  prefilter increases out-of-band linearity

Filter  
before  
distortion



# Rauch Biquadratic cell

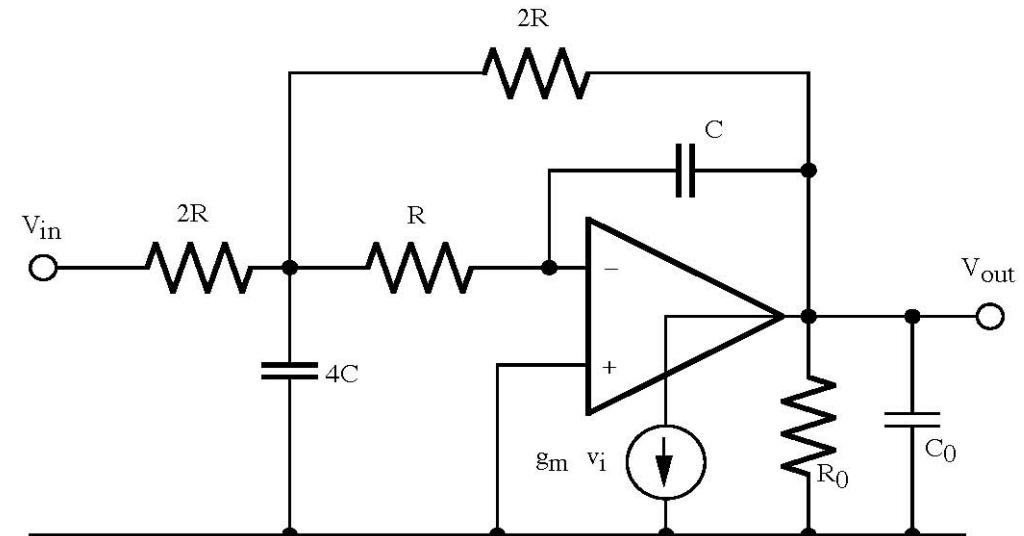
- Real op-amp effects

$$H(s) = \frac{-1 + s(R + R_0)C / (A_0 + 1)}{\alpha + s\beta + s^2\gamma + s^3\delta}$$

$$\alpha = 1 + \frac{4}{A_0 - 1}$$

$$\beta = 4RC + \frac{2R_0C_0 + R_0C + 13RC}{A_0 - 1}$$

$$\gamma = 8R^2C^2 + \frac{6RR_0CC_0 + 2RR_0C^2 + 18R^2C^2}{A_0 - 1}$$



$$\delta = 8 \cdot \frac{R^2 R_0 C_0 C^2}{A_0 - 1} g_m$$

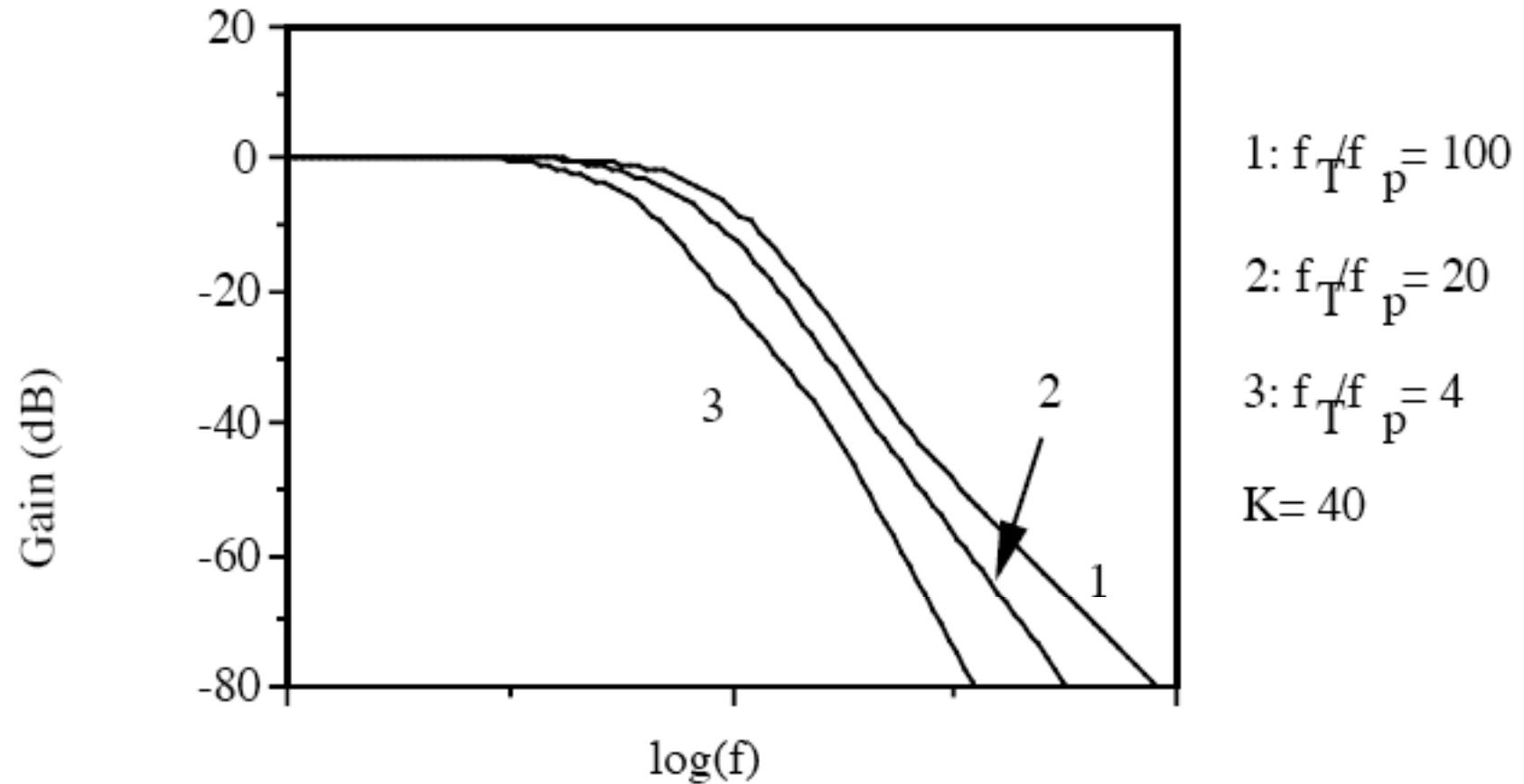
$$A_0 = g_m R_0$$

- The transfer function has one zero and three poles
- The zero is far away from  $f_p$  if  $A_0 \gg 1$
- The extra-pole is around the unity gain frequency of the op-amp



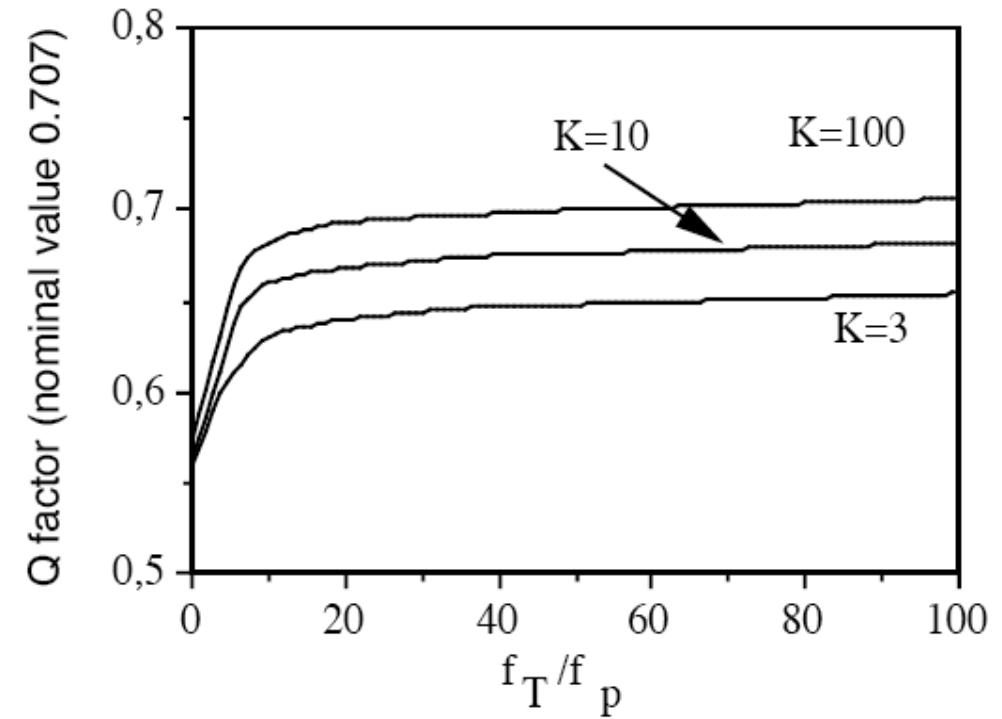
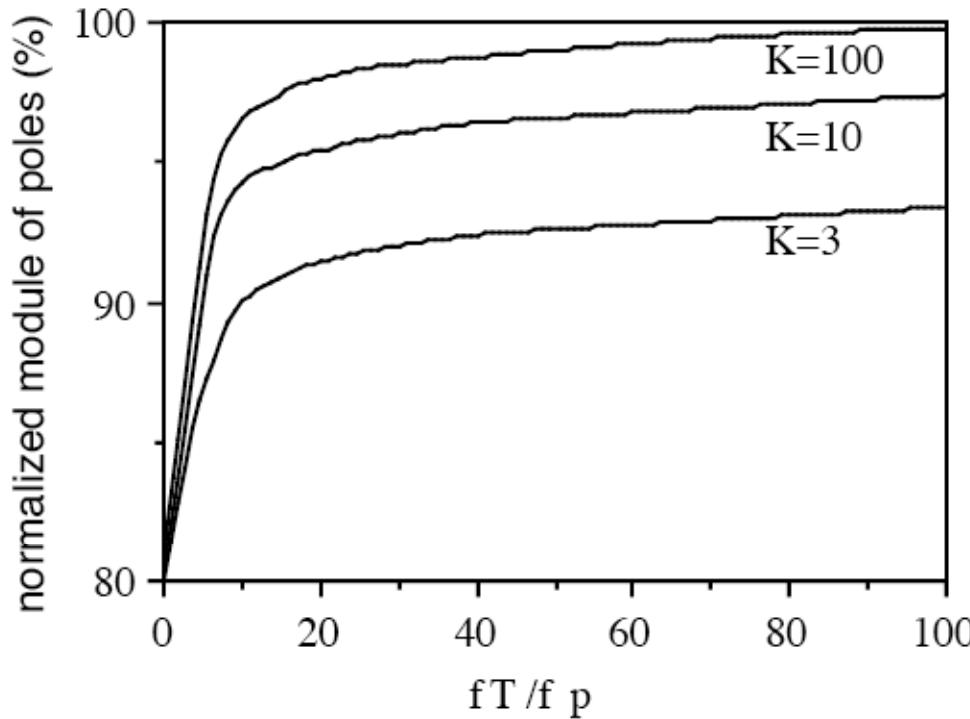
# Rauch Biquadratic cell

- Real opamp effects



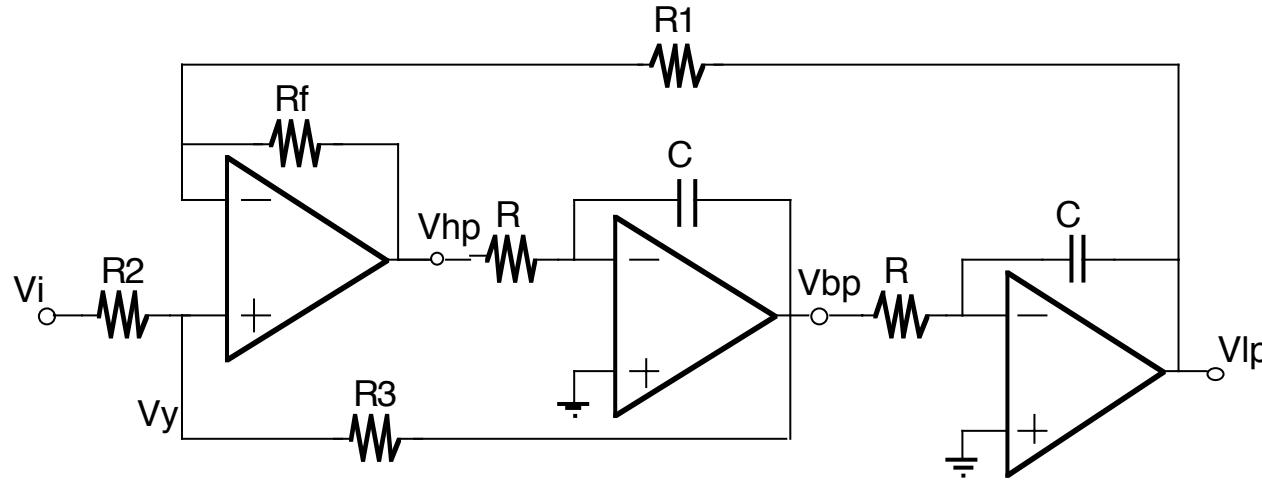
# Rauch Biquadratic cell

- Real op-amp effects
- The two other poles are shifted with respect to the designed location



# Multi-opamp biquad cell

Kerwin-Huelsman-Newcomb (KHN) Biquadratic cell

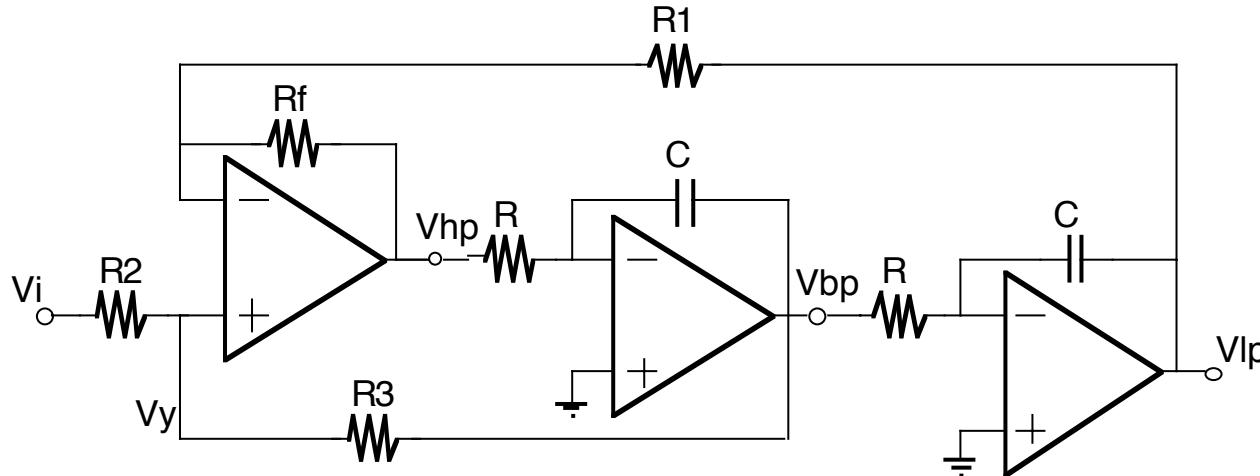


$$\left\{ \begin{array}{l} \frac{V_i - V_y}{R_2} = \frac{V_y - V_{bp}}{R_3} \\ \frac{V_{lp} - V_y}{R_1} = \frac{V_y - V_{hp}}{R_f} \\ V_{bp} = \frac{V_{hp}}{s \cdot R \cdot C} \\ V_{lp} = \frac{V_{bp}}{s \cdot R \cdot C} \end{array} \right.$$



# Multi-opamp biquad cell

Kerwin-Huelsman-Newcomb (KHN) Biquadratic cell



$$H_{LP}(s) = \frac{R_3 \cdot (R_f + R_1)}{C^2 \cdot R^2 \cdot R_1 \cdot (R_2 + R_3) \cdot s^2 + C \cdot R \cdot R_2 \cdot (R_f + R_1) \cdot s + R_f \cdot (R_2 + R_3)}$$

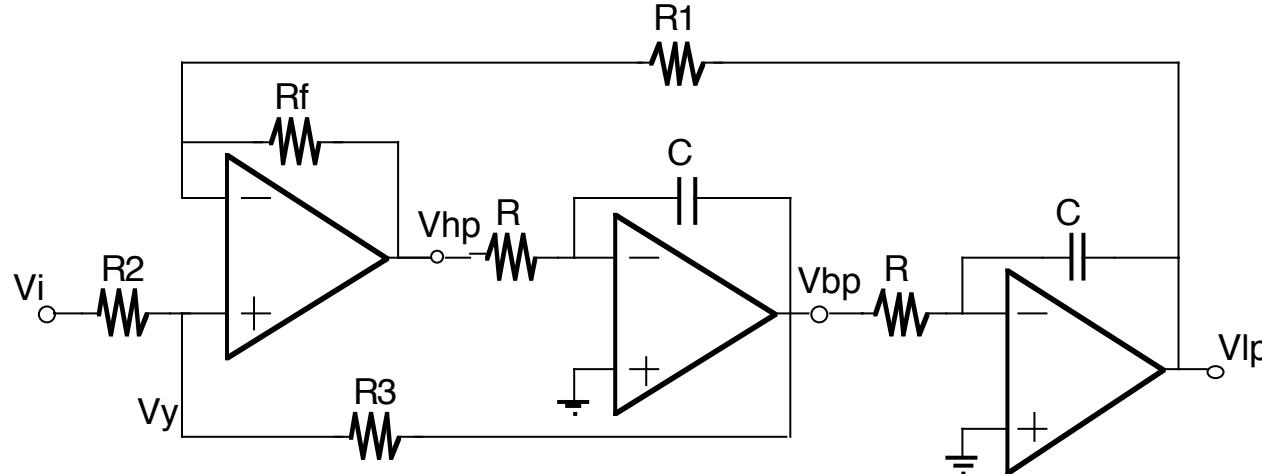
$$H_{BP}(s) = \frac{C \cdot R \cdot R_3 \cdot (R_f + R_1) \cdot s}{C^2 \cdot R^2 \cdot R_1 \cdot (R_2 + R_3) \cdot s^2 + C \cdot R \cdot R_2 \cdot (R_f + R_1) \cdot s + R_f \cdot (R_2 + R_3)}$$

$$H_{HP}(s) = \frac{C^2 \cdot R^2 \cdot R_3 \cdot (R_f + R_1) \cdot s^2}{C^2 \cdot R^2 \cdot R_1 \cdot (R_2 + R_3) \cdot s^2 + C \cdot R \cdot R_2 \cdot (R_f + R_1) \cdot s + R_f \cdot (R_2 + R_3)}$$



# Multi-opamp biquad cell

Kerwin-Huelsman-Newcomb (KHN) Biquadratic cell



- The pole frequency and quality factor are defined by the denominator
- The denominator is fixed by the loop and it is then common to the three t,f,'s

$$DEN(s) = C^2 \cdot R^2 \cdot R_1 \cdot (R_2 + R_3) \cdot s^2 + C \cdot R \cdot R_2 \cdot (R_f + R_1) \cdot s + R_f \cdot (R_2 + R_3)$$

$$DEN(s) = s^2 + s \cdot \frac{R_2 \cdot (R_f + R_1)}{C \cdot R \cdot R_1 \cdot (R_2 + R_3)} + \frac{R_f}{C^2 \cdot R^2 \cdot R_1} = s^2 + s \cdot \frac{\omega_O}{Q} + \omega_O^2$$

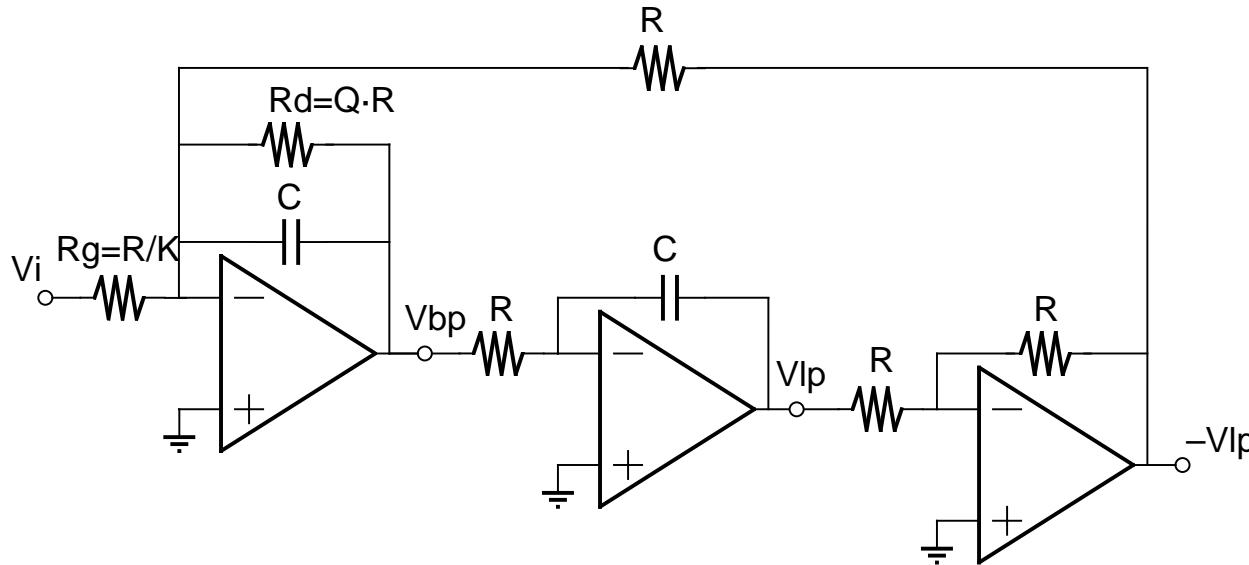
$$\omega_O = \frac{1}{C \cdot R} \cdot \sqrt{\frac{R_f}{R_1}}$$

$$Q = \left(1 + \frac{R_3}{R_2}\right) \cdot \frac{\sqrt{R_f \cdot R_1}}{R_f + R_1}$$



# Multi-opamp biquad cell

## Tow-Thomas Biquadratic cell



$$\begin{cases} \frac{V_i}{R_g} = s \cdot C \cdot V_{bp} \cdot \frac{V_{bp}}{R_d} + \frac{V_{lp}}{R} \\ V_{lp} = \frac{V_{bp}}{s \cdot R \cdot C} \end{cases}$$

$$H_{LP}(s) = \frac{R \cdot R_d}{R_d \cdot R_g + C \cdot R^2 \cdot R_g \cdot s + C^2 \cdot R^2 \cdot R_g \cdot R_d \cdot s^2}$$

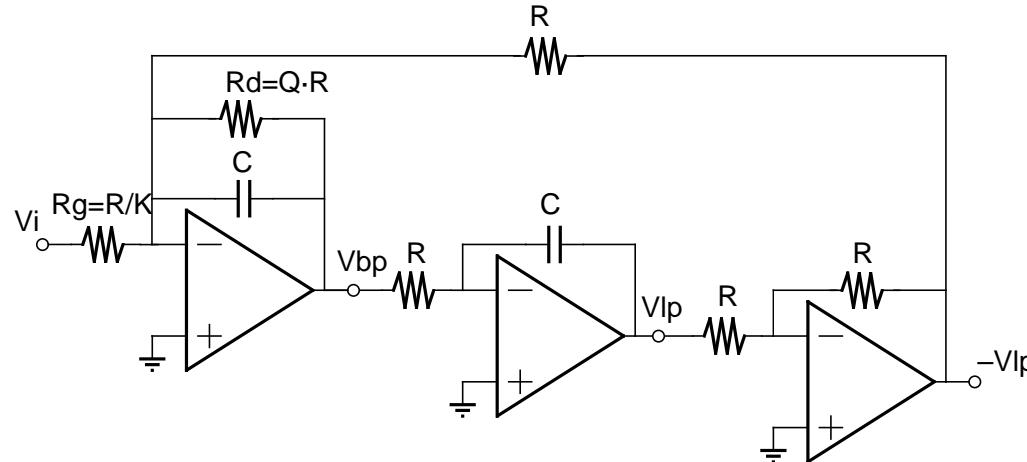
$$H_{BP}(s) = \frac{C \cdot R^2 \cdot R_d \cdot s}{R_d \cdot R_g + C \cdot R^2 \cdot R_g \cdot s + C^2 \cdot R^2 \cdot R_g \cdot R_d \cdot s^2}$$

- No sensitivity to parasitic capacitance



# Multi-opamp biquad cell

## Tow-Thomas Biquadratic cell



- The zero position (Numerator) depends on input and output nodes
- The pole position (Denominator) depends on feedback loop

$$DEN(s) = R_d \cdot R_g + C \cdot R^2 \cdot R_g \cdot s + C^2 \cdot R^2 \cdot R_g \cdot R_d \cdot s^2$$

$$DEN(s) = s^2 + s \cdot \frac{1}{C \cdot R_d} + \frac{1}{C^2 \cdot R^2} = s^2 + s \cdot \frac{\omega_o}{Q} + \omega_o^2$$

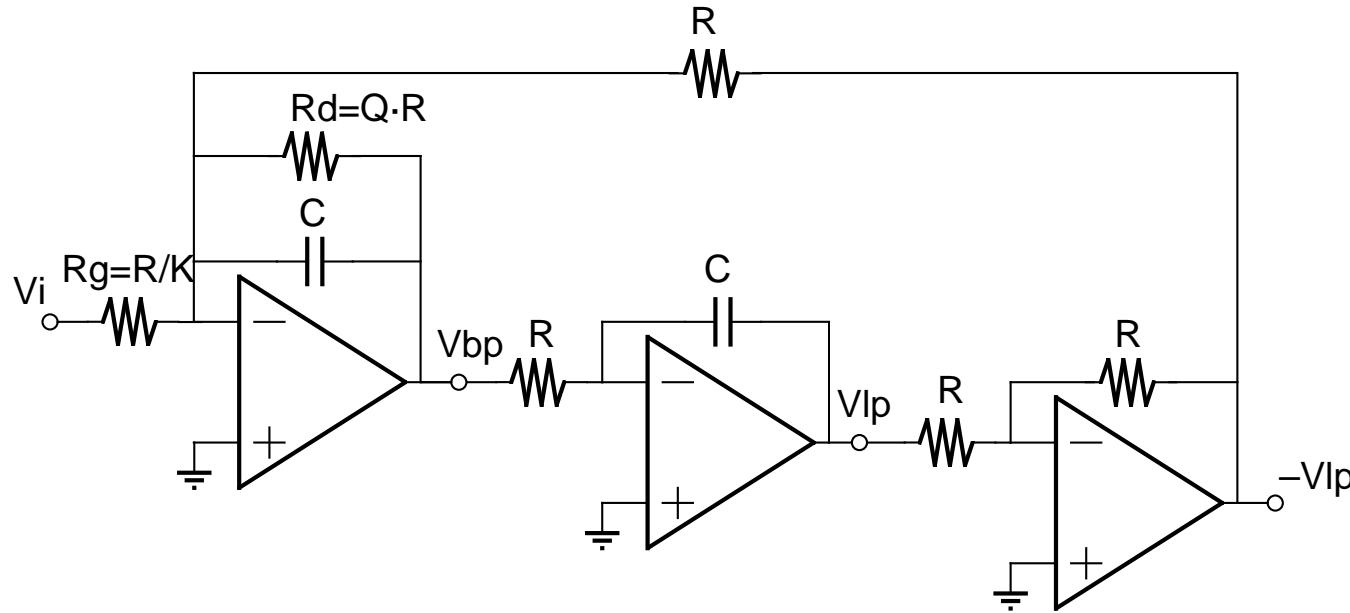
$$\omega_o = \frac{1}{C \cdot R}$$

$$Q = \frac{R_d}{R}$$



# Multi-opamp biquad cell

## Tow-Thomas Biquadratic cell



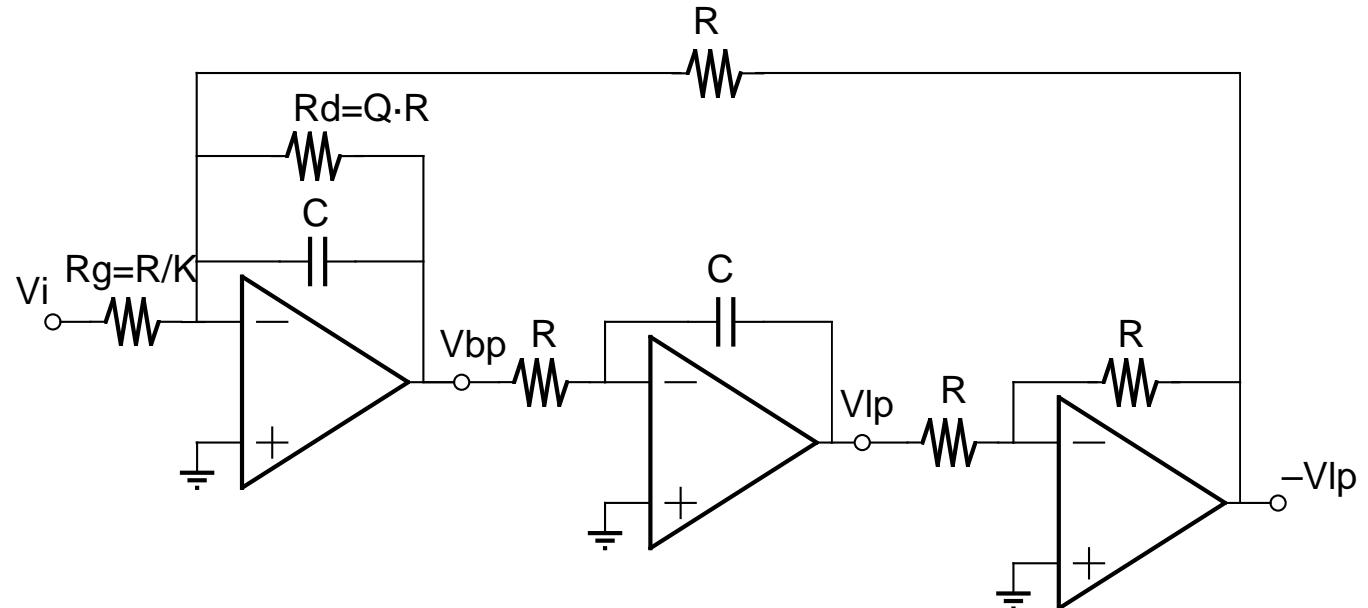
- The 3<sup>rd</sup> opamp has just to invert the signal
- In a fully differential implementation it can be replaced by crossing the lines



# Active-RC filters

## Opamp design

- In any circuit configuration, a resistor is connected to the output node
- This resistor is in parallel to the output impedance



- The effects of this resistor have to be reduced
  - Use of low output impedance opamp (output buffer)
    - Power hungry in CMOS
  - Use of multistage opamp structure
    - The load of the output stage is the external resistor
      - The output stage gain is very low



# Active-RC filters

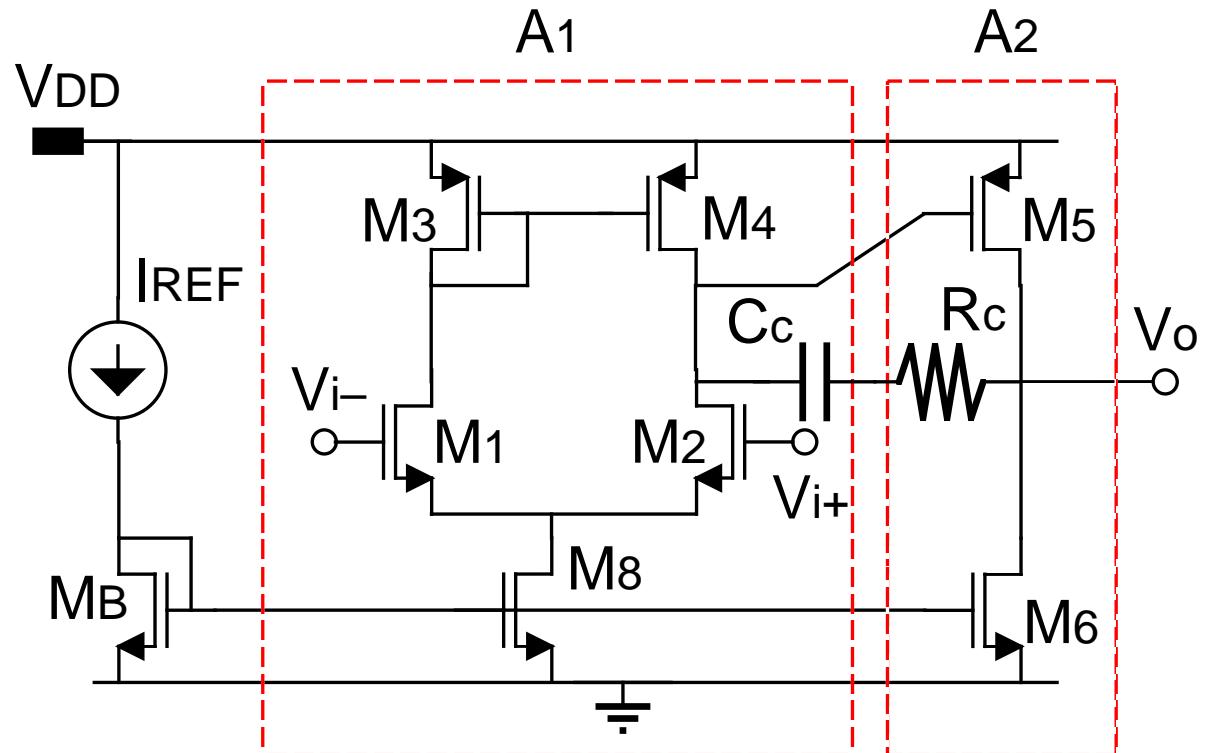
## Opamp design

- Typical solution: two stage opamp

- The 1<sup>st</sup> (input) stage is designed to fit bandwidth and noise performance

- The 2<sup>nd</sup> (output) stage is designed to drive the output resistive and capacitive load

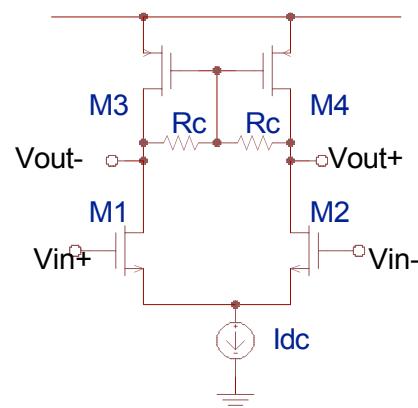
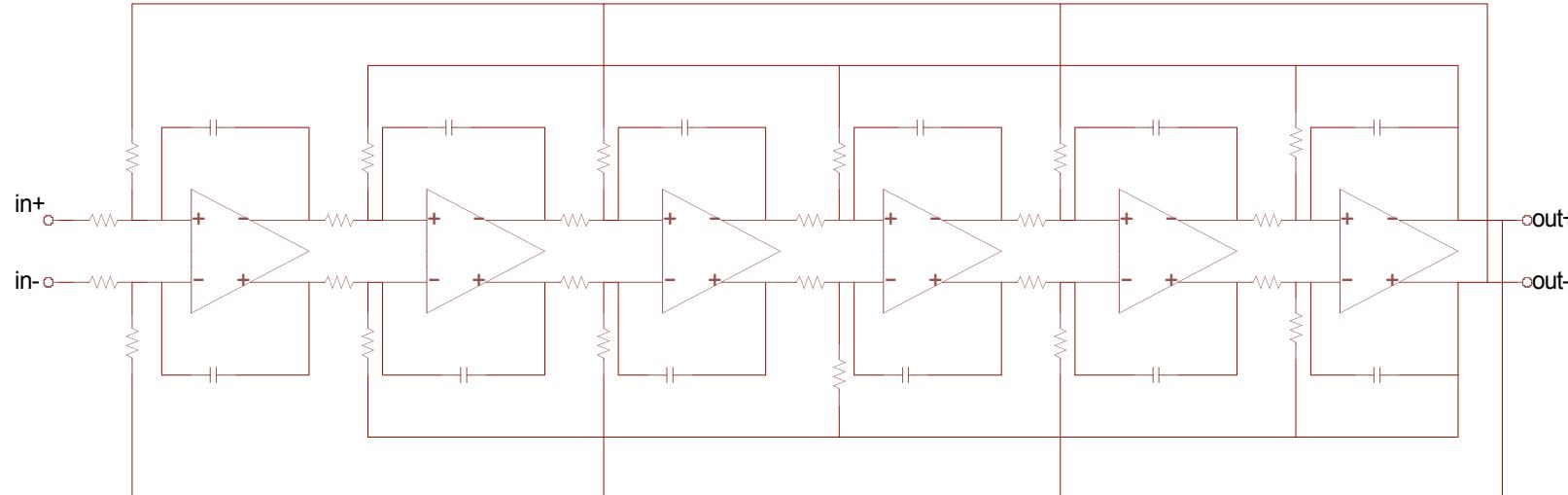
- A class-AB output stage could be eventually used to reduce distortion due to class-A current limitation



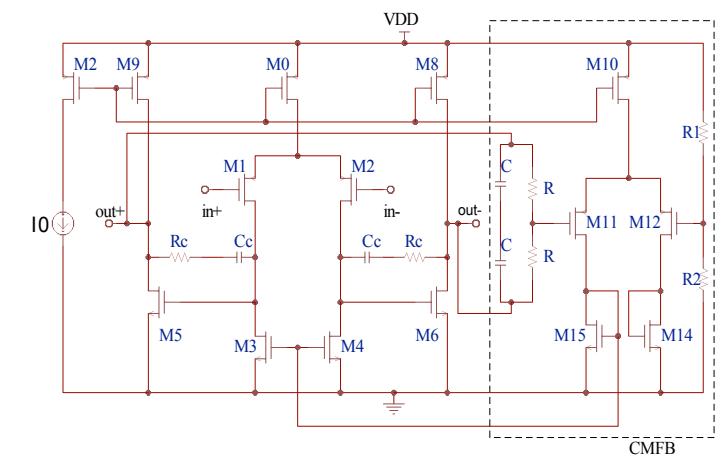
# Active-RC Filters

## Low-noise solution – IFLF Structure

- Example: 6<sup>th</sup> order filter

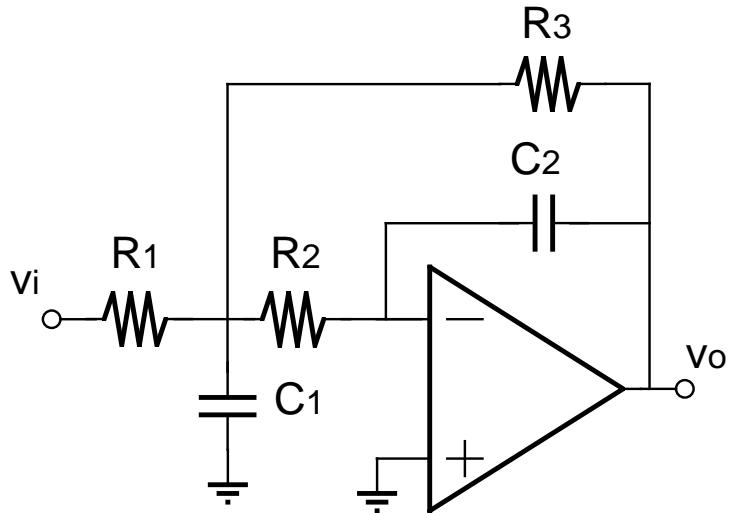


- Opamp 1, 2, 3, 5
- Single stage
- Low-noise
- Power optimized (no CMFB)
- Opamp 4, 6
- Two-stage
- Driving capability



# Active-RC Filters

## Tunability / Programmability



$$H(s) = \frac{1}{s^2 \cdot R_1 \cdot R_2 \cdot C_1 \cdot C_2 + s \cdot C_2 \cdot \left( R_1 + R_2 + \frac{R_1 \cdot R_2}{R_3} \right) + \frac{R_1}{R_3}}$$

- The frequency response depends on the value of passive components
- Their value cannot be changed with a continuous tuning
- A digital control is possible

- Capacitors and/or Resistors are implemented with a digitally-controlled array, which selects the amount of passive components “effectively” connected to the network
- Tuning for significantly different filter bandwidth could allow to modify the opamp performance to save power consumption



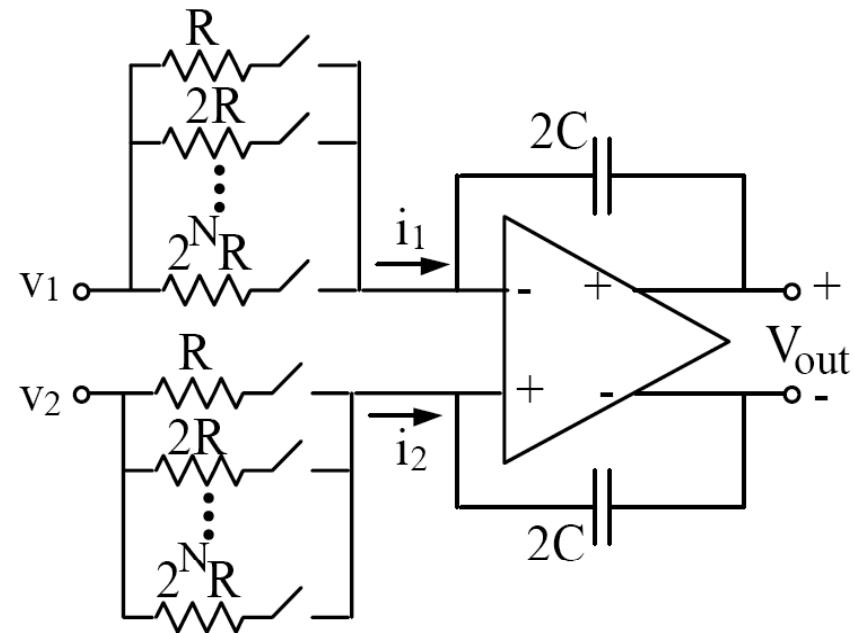
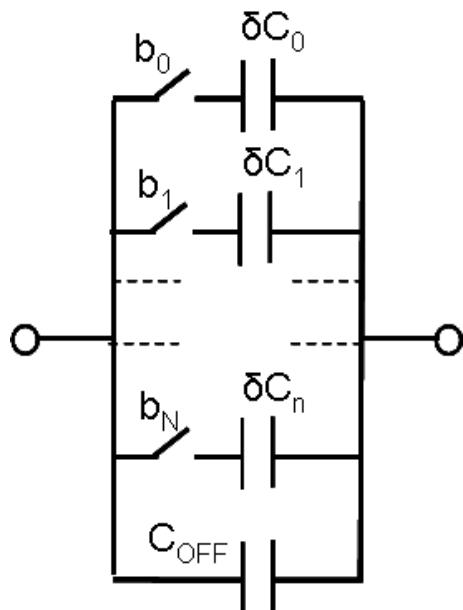
# Active-RC Filters

## Tunability / Programmability

- Discrete tuning approaches

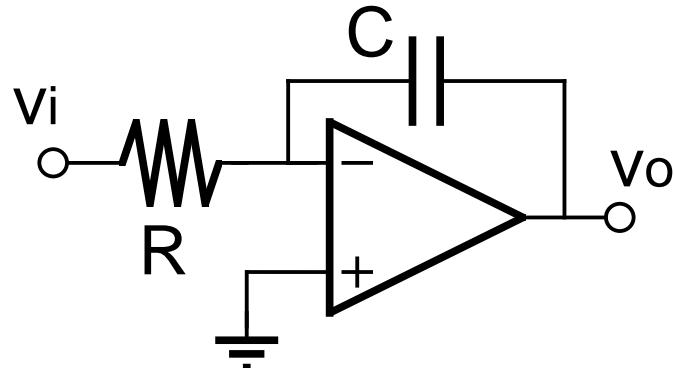
Changing capacitors maintains the same in-band noise level

Changing resistors maintains the same overall noise ( $\approx kT/C$ )



# Active-RC Filters

## Frequency response sensitivity



$$H_{id}(s) = -\frac{1}{s \cdot R \cdot C}$$

- Assuming a single-pole open-loop opamp

$$H_{opamp}(s) = \frac{A_o}{1 + s \cdot \tau}$$

- The integrator closed loop frequency response

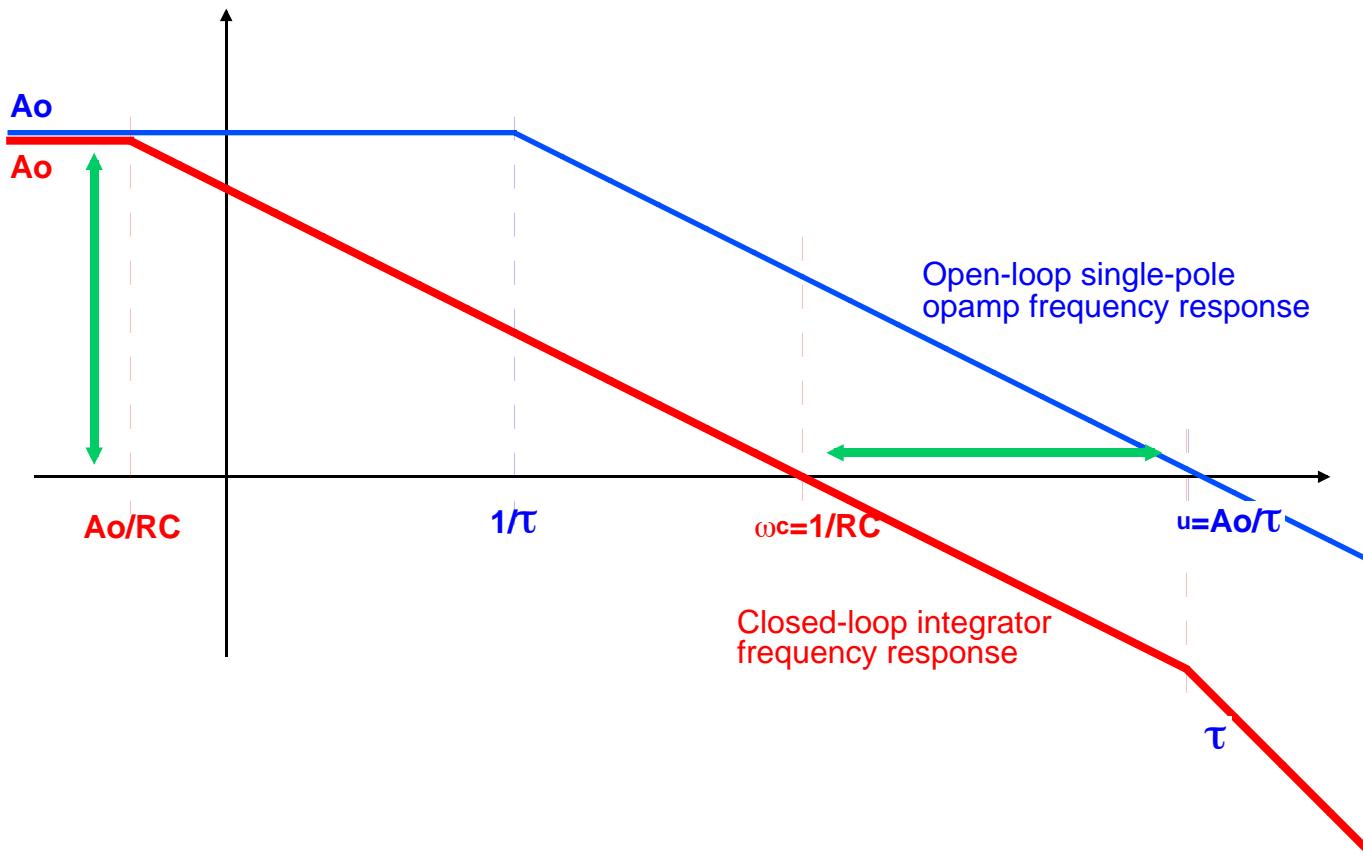
$$H_{int\_real}(s) = -\frac{A_o}{(1 + s \cdot R \cdot C \cdot A_o) \cdot (1 + s \cdot \tau / A_o)} \xrightarrow{A_o \rightarrow \infty} -\frac{1}{s \cdot R \cdot C}$$



# Active-RC Filters

## Frequency response sensitivity

$$H_{\text{int\_real}}(s) = -\frac{A_o}{(1+s \cdot R \cdot C \cdot A_o) \cdot (1+s \cdot \tau / A_o)} \xrightarrow[A_o \rightarrow \infty]{} \frac{1}{s \cdot R \cdot C}$$

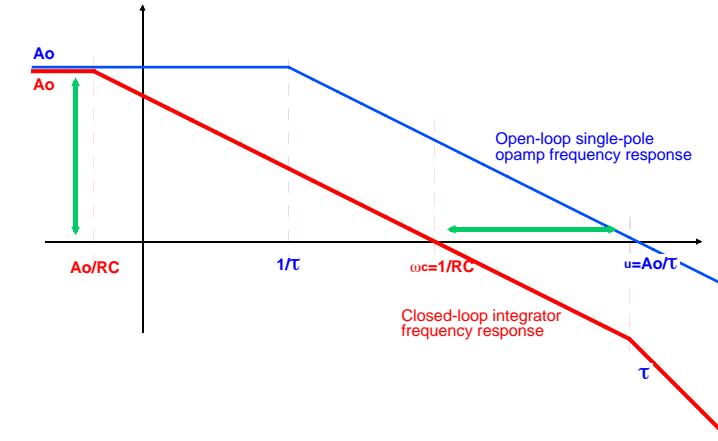
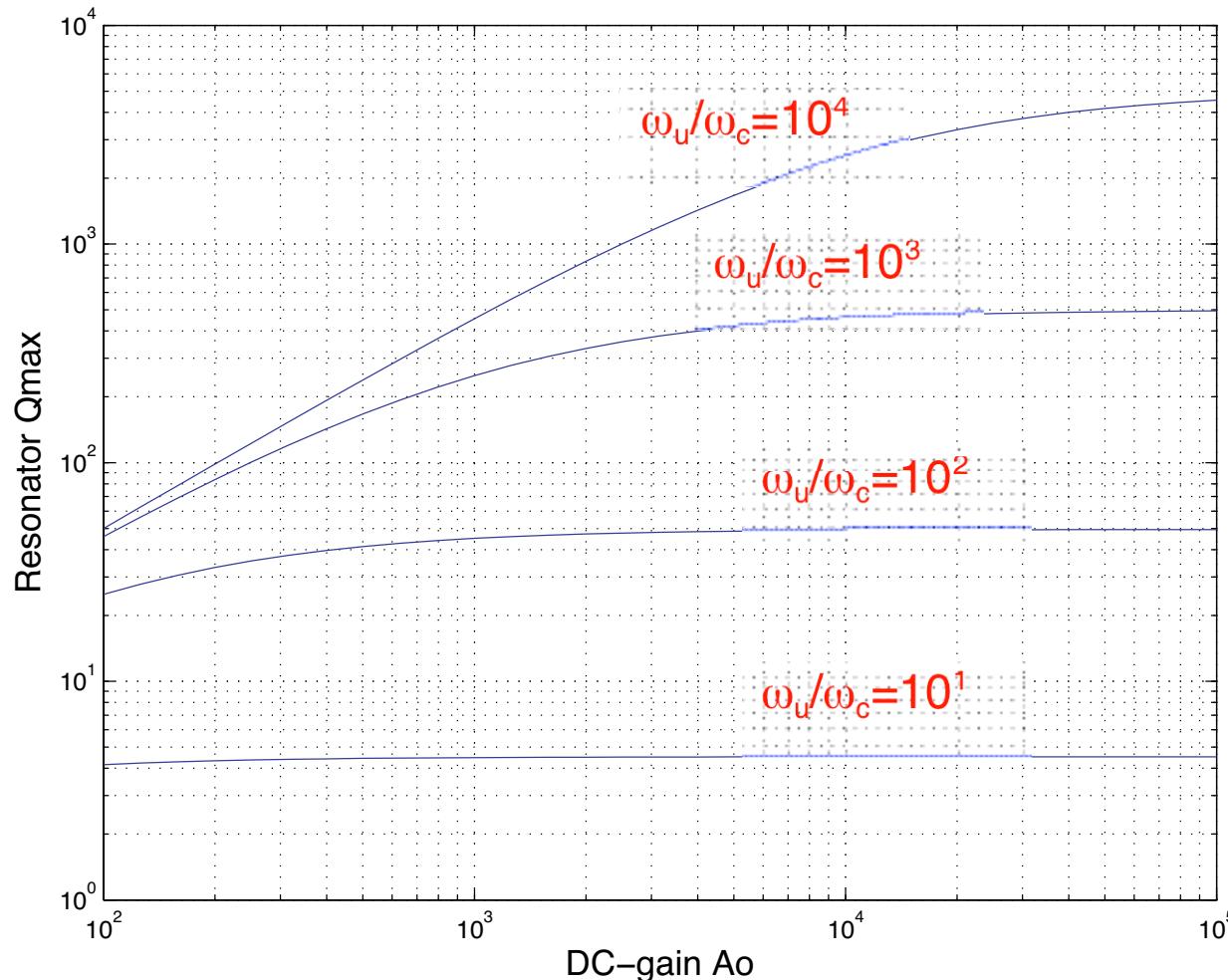


- Two real poles are present
- The finite gain results in a LF pole that gives a phase lead
- The UGB gives a HF pole that gives a phase lag



# Resonator Q Quality Factor

- The resonator Q is affected by the opamp performance (Ao & UGB)

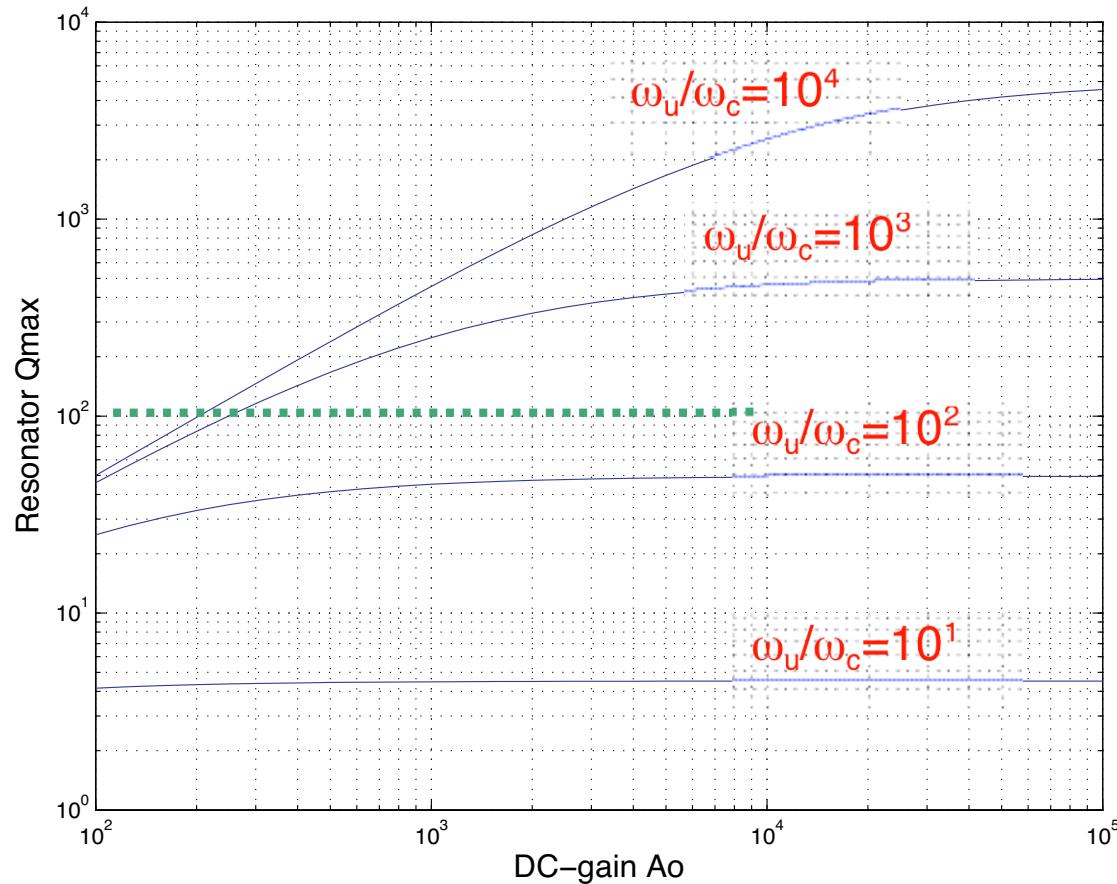


- $Q_{real}$  is the parallel of  $Q_{res}$  and of  $Q_{ideal}$

$$\frac{1}{Q_{real}} = \frac{1}{Q_{res}} + \frac{1}{Q_{ideal}}$$



# Resonator $Q$ Quality Factor



$$\frac{1}{Q_{real}} = \frac{1}{Q_{res}} + \frac{1}{Q_{ideal}}$$

$$\frac{1}{Q_{res}} = \frac{\Delta Q}{Q_{ideal} + \Delta Q} \cdot \frac{1}{Q_{ideal}}$$

$$\frac{1}{Q_{res}} \approx \frac{\Delta Q}{Q_{ideal}} \cdot \frac{1}{Q_{ideal}}$$

- To have  $Q_{real} \approx Q_{ideal}$ ,
- $Q_{res} \gg Q_{ideal}$
- High gain  $A_o$  and large UGB are needed
- Ex.:  $Q=5$  and  $\Delta Q/Q < 5\%$ 
  - $\rightarrow Q_{res} > 100$

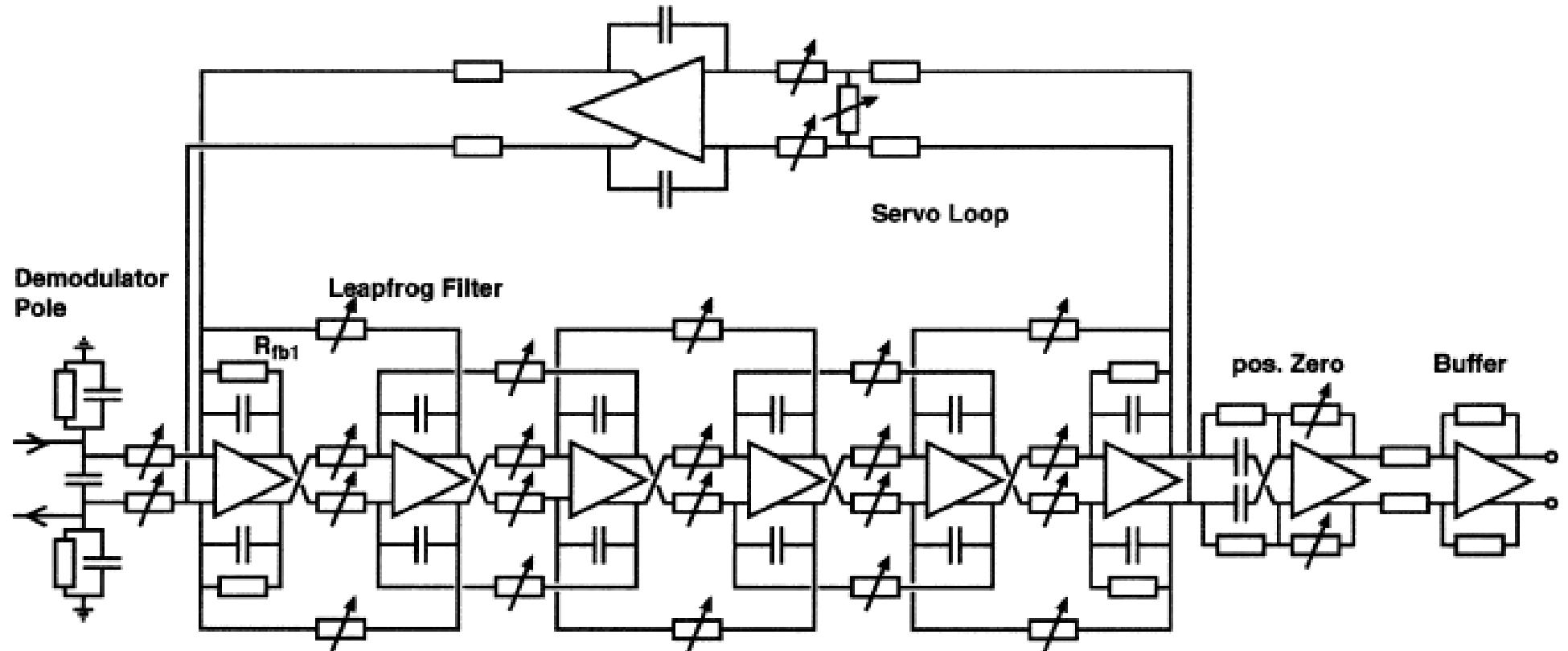
- Active-RC filters require high-performance opamps !!!



# Active-RC filters

## Design example

- WCDMA receiver (Rogin@ETH-Zurich, ISSCC03)
  - a 6<sup>th</sup> order Chebychev low-pass filter with 0.2-dB ripple



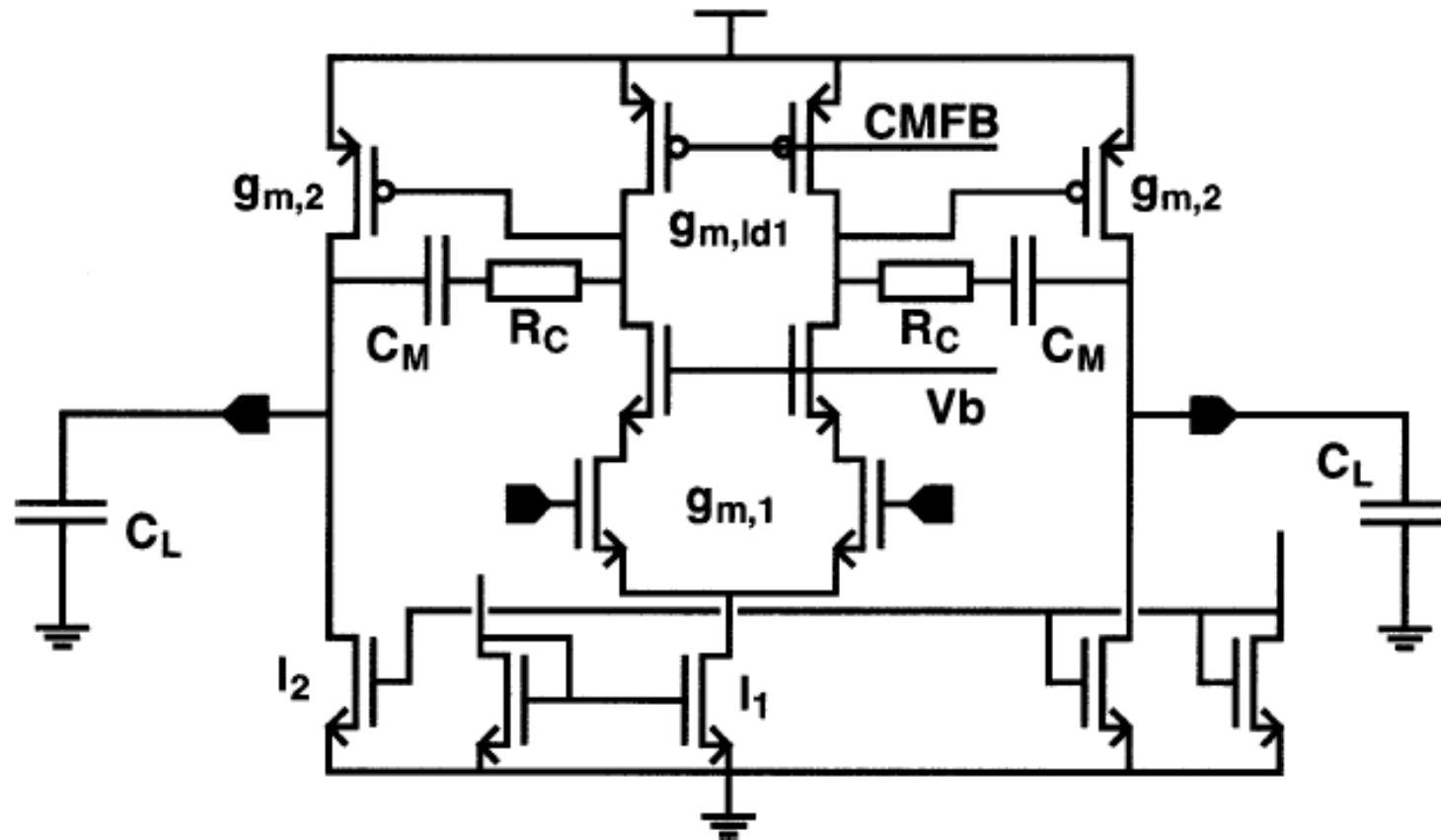
- Cascade of three biquadratic cells



# Active-RC filters

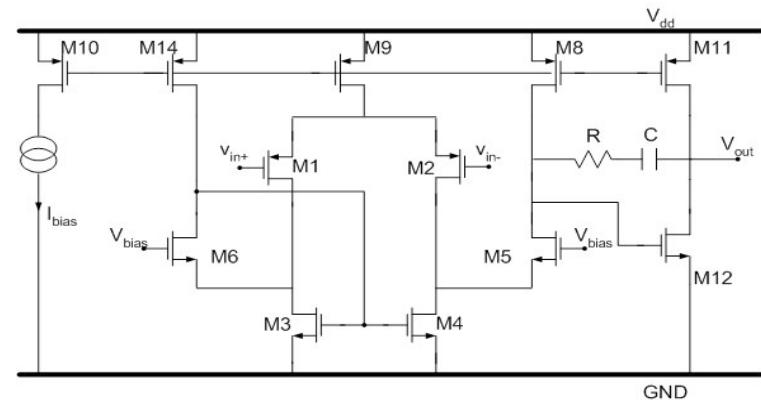
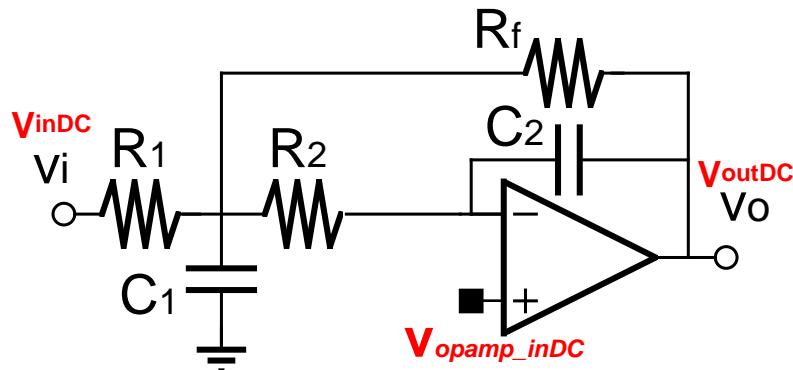
## Design example

- WCDMA receiver (Rogin@ETH-Zurich, ISSCC03)
  - a two-stage opamp



# Active-RC filters

## Bias Point Design



- To maximize output swing

$$V_{outDC} = V_{DD}/2$$

- To have a dc-coupling between cells

$$V_{inDC} = V_{outDC} = V_{DD}/2$$

- To balance dc-currents

$$V_{in\_opampDC} = V_{inDC} = V_{outDC} = V_{DD}/2$$

- To bias input PMOS devices

$$V_{in\_opampDC} = V_{DD} - V_{GS\_inputpair} + V_{sat\_currentsource}$$

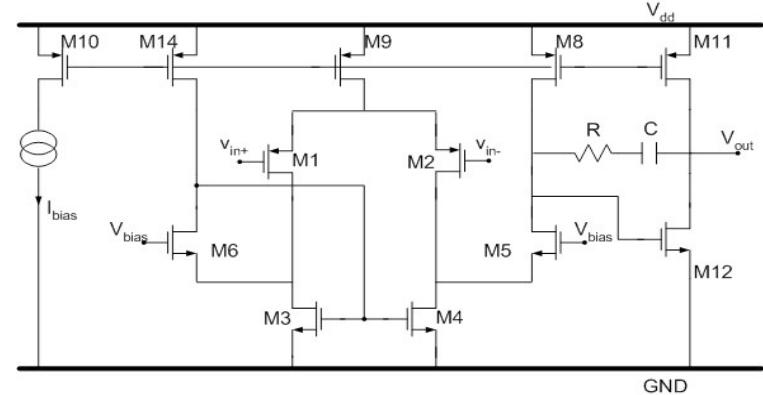
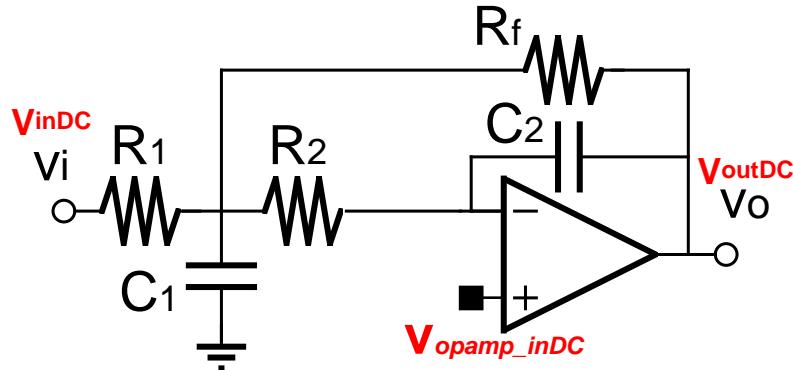
- The minimum  $V_{DDmin}$  results

$$V_{DDmin} = V_{opamp\_inDC} + V_{GS\_inputpair} + V_{sat\_currentsource}$$



# Active-RC filters

## Low-voltage Design



- The minimum  $V_{DDmin}$  results

$$V_{DDmin} = V_{opamp\_inDC} + V_{GS\_inputpair} + V_{sat\_currentsource} \quad \text{with} \quad V_{opamp\_inDC} = V_{DDmin}/2$$

$$V_{DDmin} = 2 \cdot (V_{GS\_inputpair} + V_{sat\_currentsource}) = 2 \cdot V_{TH} + 4 \cdot V_{ov}$$

- Example:

- 0.13 μm CMOS technology
- $V_{TH} = 0.3V$
- $V_{ov} = 0.1 V$ 
  - $V_{DDmin} = 1.4V$



# Active-RC filters

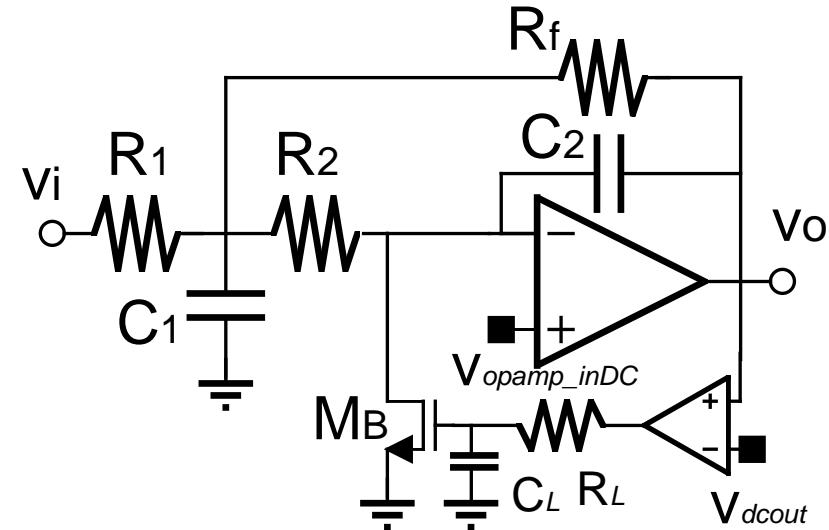
## Low-voltage Design

- Current source  $M_B$  allows to reduce  $V_{DDmin}$
- The current source (together with the control loop with the low-pass filter) allows to fix  

$$V_{outDC} = V_{DD}/2$$
- → the virtual ground principle forces to have  $V_{opamp\_inDC} = V_B$ , which is fixed to be  $V_B = V_{ov} = 200\text{mV}$ , i.e. the  $M_B$  saturation/overdrive voltage
- It follows that:

$$V_{DDmin} = V_{ov} + V_{GS\_inputpair} + V_{sat\_currentsource} = V_{TH} + 3 \cdot V_{ov} \ll 2 \cdot V_{TH} + 4 \cdot V_{ov}$$

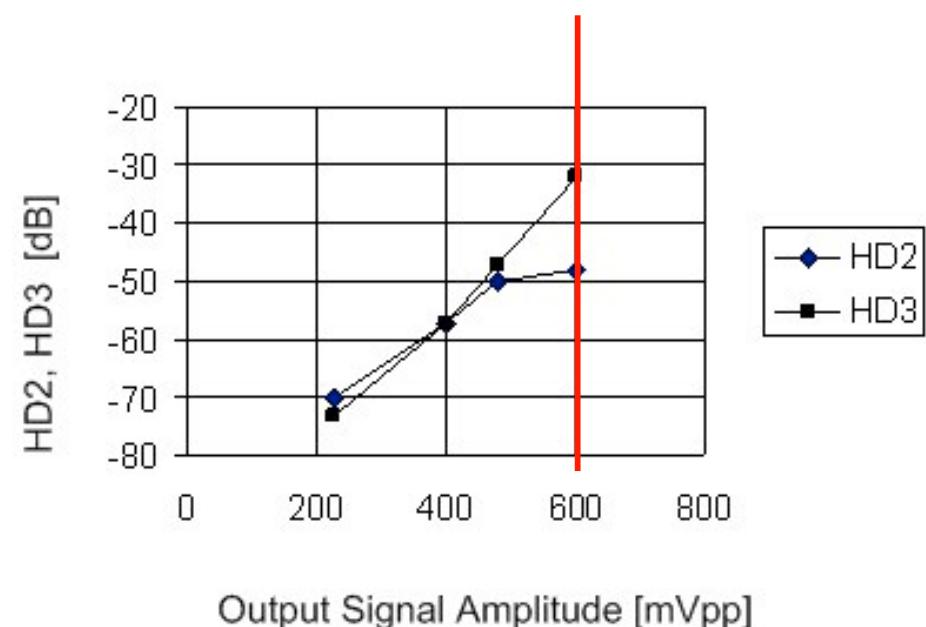
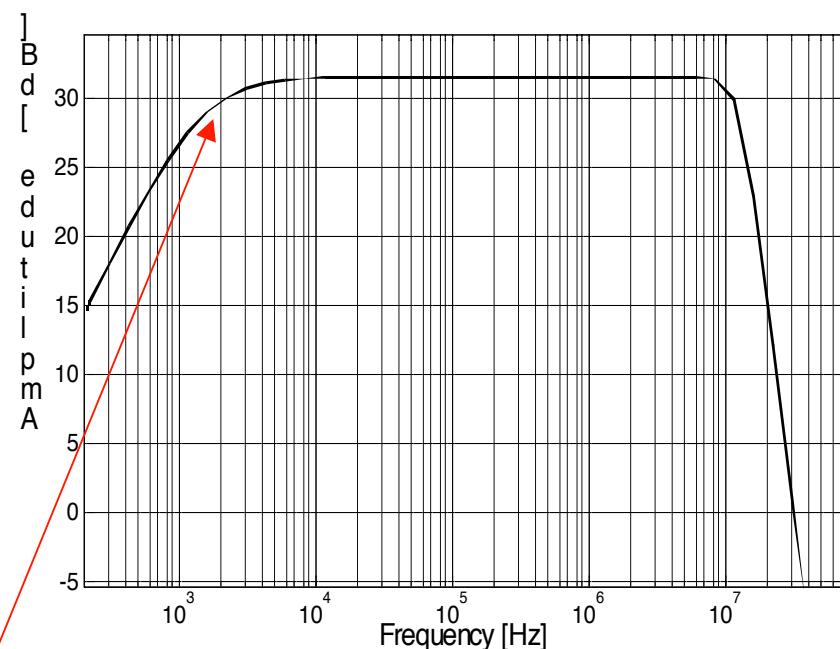
- The LP filter in the control-loop places a zero at dc and a pole at low frequency (few kHz)
- These additional singularities in the overall frequency allow to relax the front-end dc-offset performance without a significant signal degradation.
  - Ex.:  $0.13\mu\text{m}$  CMOS technology,  $V_{TH} = 0.3\text{V}$ ,  $V_{ov} = 0.1\text{ V} \rightarrow V_{DDmin} = 0.6\text{V} \ll 1.4\text{V}$



# Active-RC filters

## Low-voltage Design

- Simulated performance



- Highpass filter for DC-control
  - Large linearity for a single-ended 0.6V filter





*Dipartimento di Ingegneria dell' Innovazione*

*Universita' degli Studi di Lecce*

*Andrea Baschirotto*

[andrea.baschirotto@unile.it](mailto:andrea.baschirotto@unile.it)

---

## Analog Filters for Telecommunications

*Universita' degli Studi di Bologna*

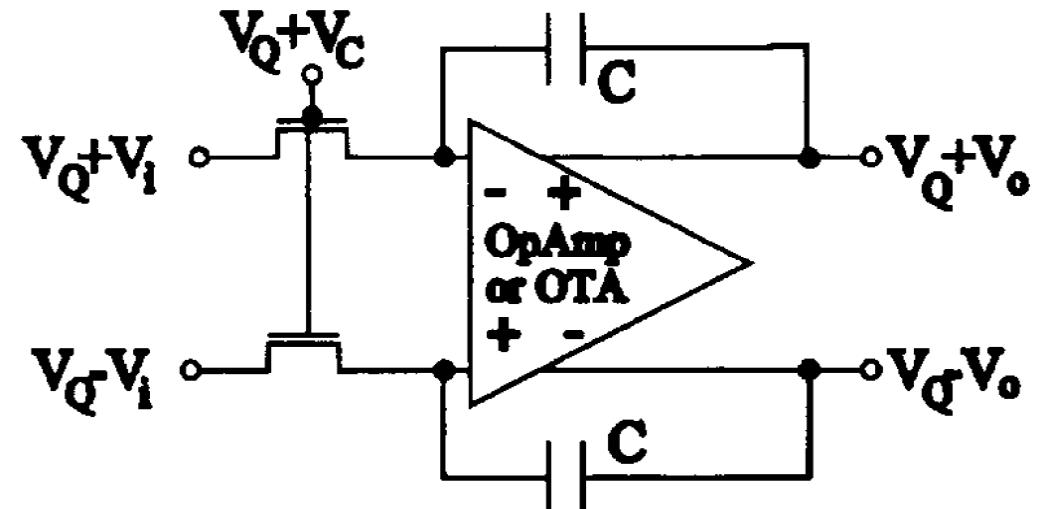
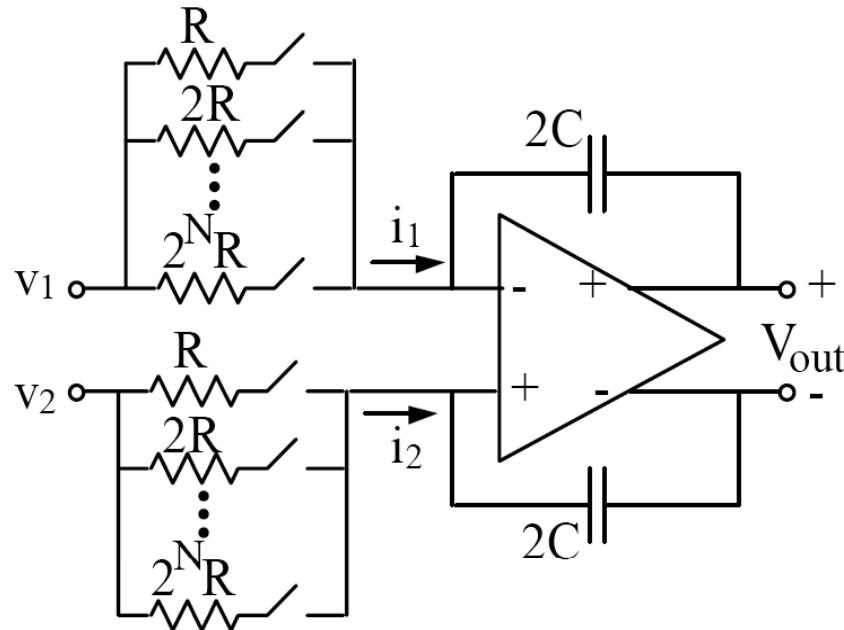
*June, 16<sup>th</sup>-17<sup>th</sup>, 2005*

## MOSFET-C Filters



# MOSFET-C Filters

- A MOS device operating in triode region can replace the resistor



- ☺ Resistor linearity
- ☹ Discrete tuning
- ☹ Integrated resistors are needed

- ☺ Full CMOS solution
- ☺ Continuous tuning
- ☹ MOS non-linearity



# MOSFET-C Filters

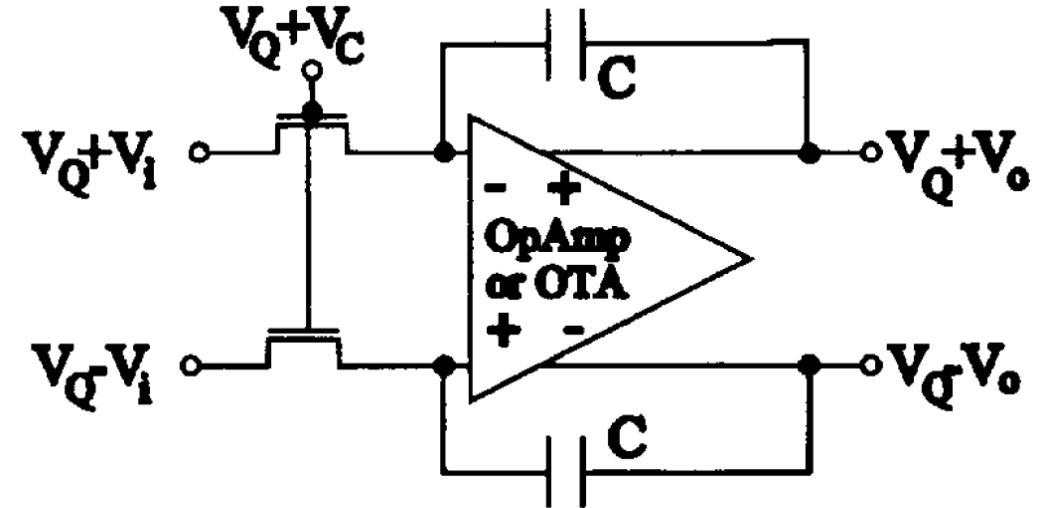
## Basic integrator

$V_Q$ : bias voltage

$V_i$ : input signal

$V_C$ : control voltage

$V_o$ : Output signal



- The MOS devices have to operate in triode region:

$$V_{DS} < V_{GS} - V_{TH}$$

$$V_i - V_Q < (V_C - V_Q) - V_{TH}$$

$$V_i < V_C - V_{TH}$$

- The MOS devices in triode region exhibits a resistance:

$$R_{MOS} = \frac{1}{\mu \cdot C_{ox} \cdot \left(\frac{W}{L}\right) \cdot (V_C - V_{TH})}$$



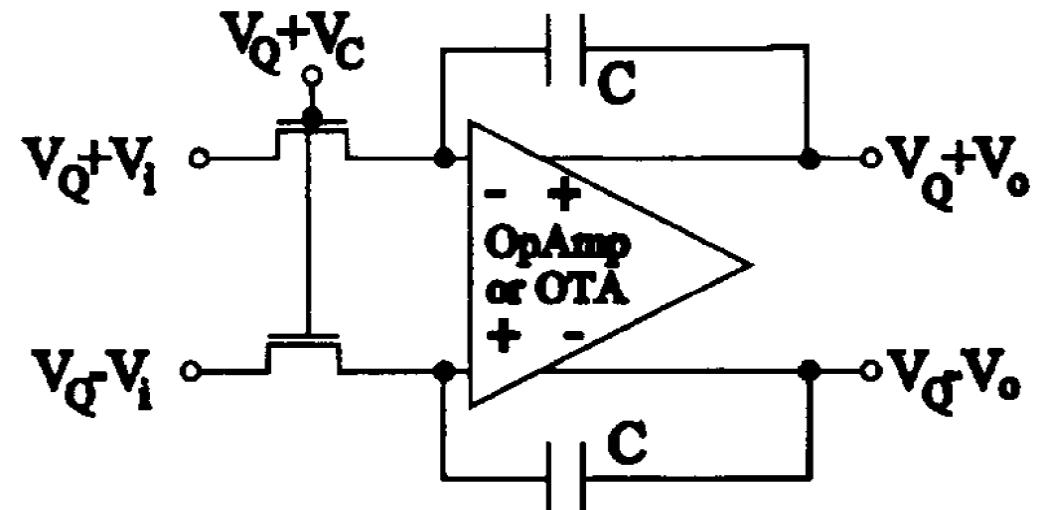
# MOSFET-C Filters

## Basic integrator

$$H(s) = -\frac{1}{s \cdot R_{MOS} \cdot C}$$

$$H(s) = -\frac{\mu \cdot C_{ox} \cdot \left(\frac{W}{L}\right) \cdot (V_C - V_{TH})}{s \cdot C}$$

$$\omega_o = \frac{1}{R_{MOS} \cdot C} = \frac{\mu \cdot C_{ox} \cdot \left(\frac{W}{L}\right) \cdot (V_C - V_{TH})}{C}$$

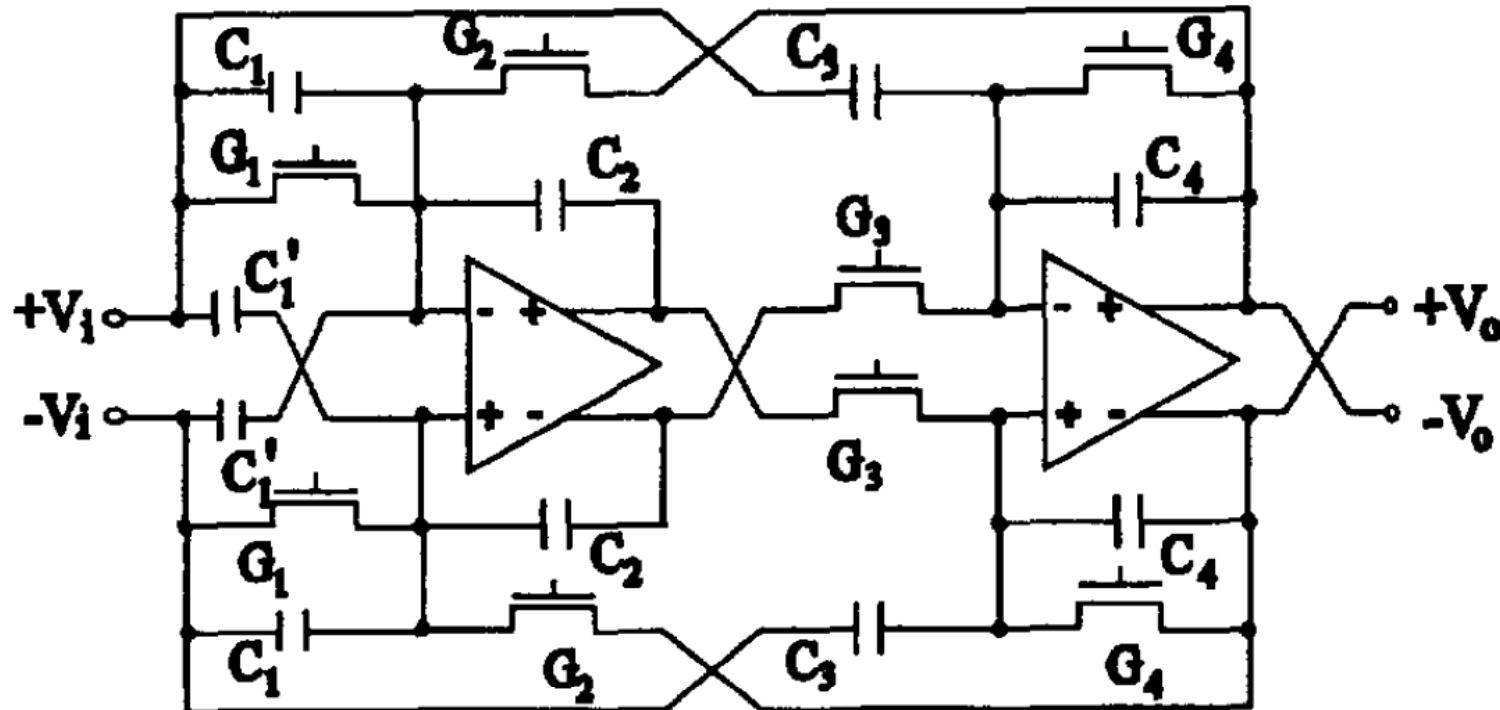


- Very poor linear range (particularly critical in scaled technology at low supply voltages)
- Differential and balanced operation partially cancel even-order non-linearities



# MOSFET-C Filters

## Programmable biquadratic cell

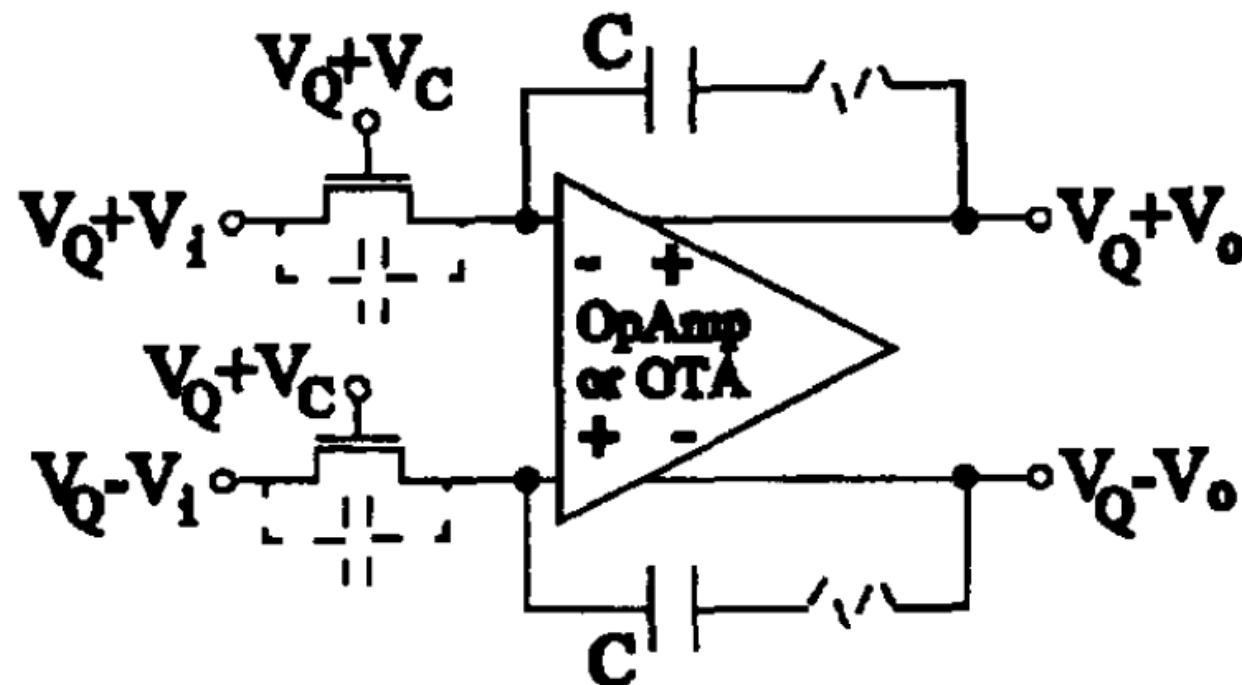


- Low-pass (all-pole) ( $C_1 = C_1' = C_3 = 0$ )
- High-pass ( $G_1 = 0, C_1 = C_1' = 0$ )
- Bandpass ( $G_1 = 0, C_3 = C_1' = 0$ )
- All-pass ( $G_1 = G_2, G_3 = G_4, C_1 = 0, C_1' = C_2, C_3 = C_4$ )
- Responses with transmission zeros ( $C_1 = C_1' = 0$ )



# MOSFET-C filters

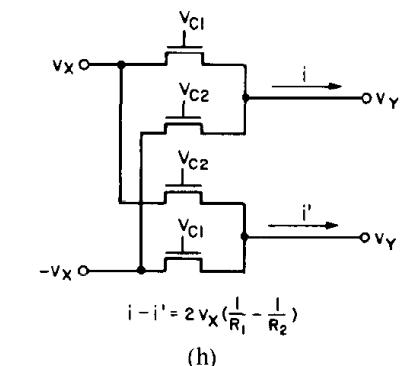
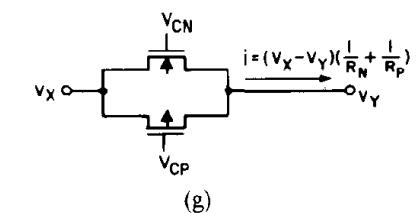
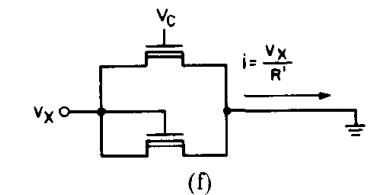
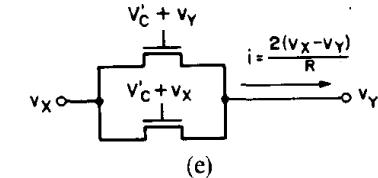
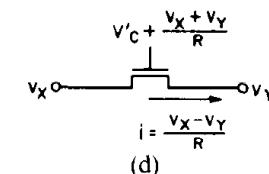
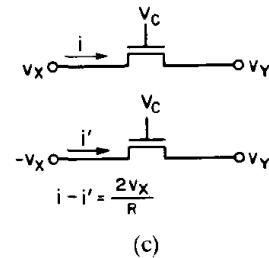
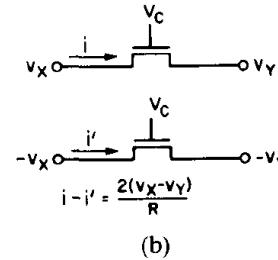
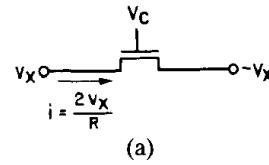
## Phase compensation



# MOSFET-C filters

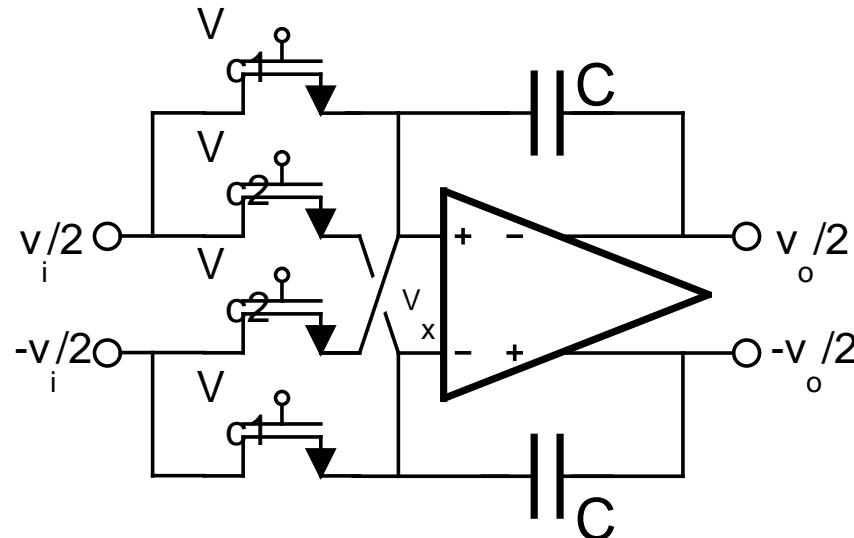
## Linearity improvement

- Several circuit solutions are possible for improving linearity



# MOSFET-C filters

## Linearity improvement



$$v_o = \frac{1}{s \cdot r_{ds1} \cdot C} \cdot \left( \frac{v_i}{2} - \left( -\frac{v_i}{2} \right) \right) + \frac{1}{s \cdot r_{ds2} \cdot C} \cdot \left( \left( -\frac{v_i}{2} \right) - \frac{v_i}{2} \right)$$

$$r_{ds1} = \frac{1}{k \cdot \left[ \frac{W}{L} \right]_1 \cdot (V_{C1} - V_X \cdot V_{TH})}$$

$$r_{ds2} = \frac{1}{k \cdot \left[ \frac{W}{L} \right]_2 \cdot (V_{C2} - V_X \cdot V_{TH})}$$



# MOSFET-C filters

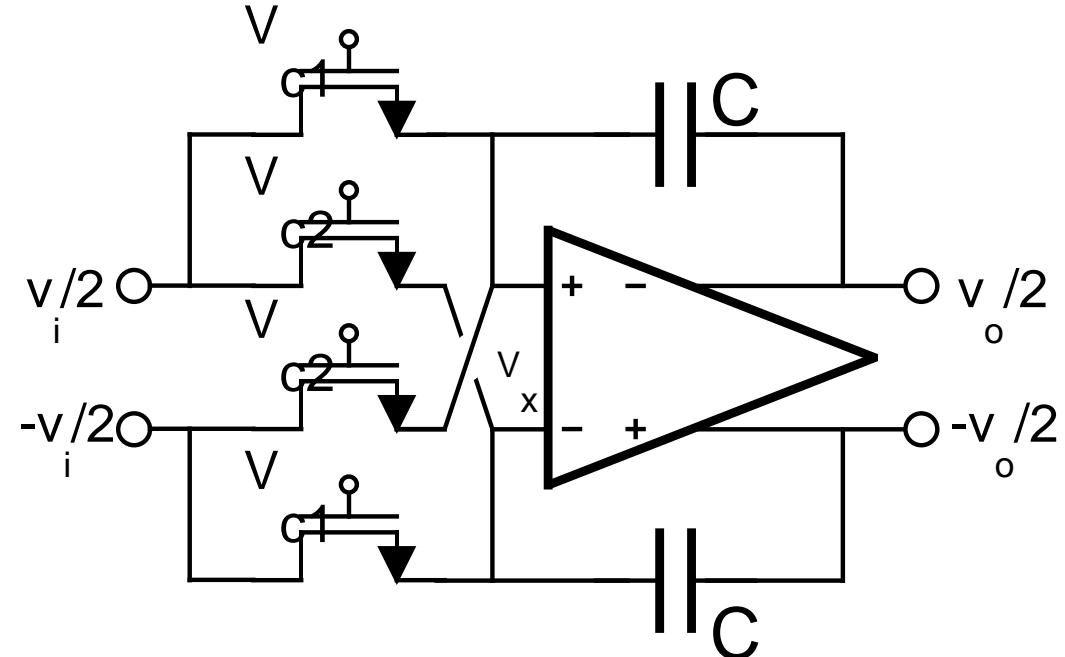
## Linearity improvement

- Assuming  $\left[\frac{W}{L}\right]_1 = \left[\frac{W}{L}\right]_2 = \left[\frac{W}{L}\right]$

$$v_o = \frac{1}{s \cdot r_{ds} \cdot C} \cdot \left( \frac{v_i}{2} - \left( -\frac{v_i}{2} \right) \right)$$

- The effective equivalent resistance is determined by the difference in the control voltages.

$$r_{ds} = \frac{1}{k \cdot \left[\frac{W}{L}\right] \cdot (V_{C1} - V_{C2})}$$



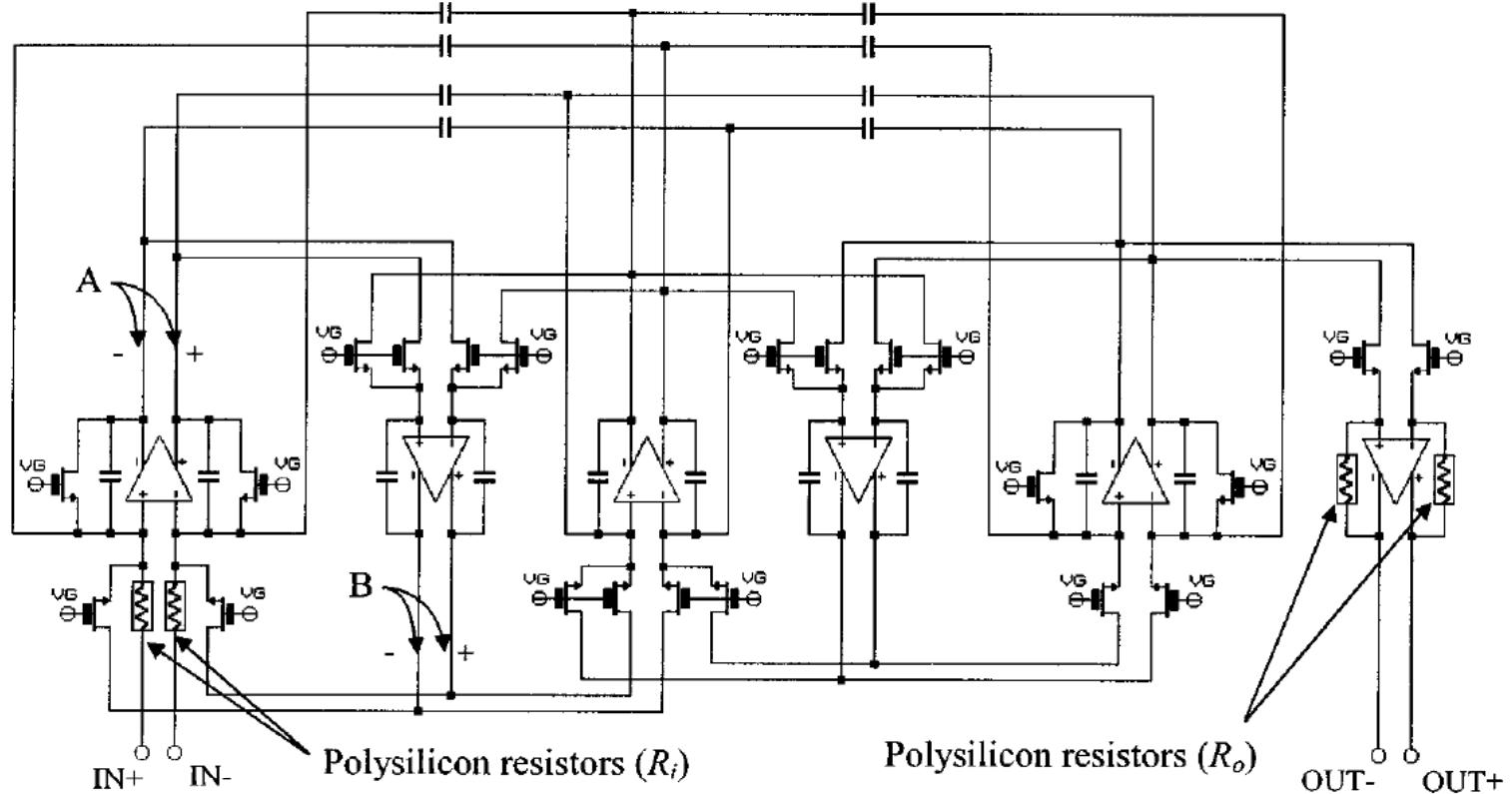
- Even and odd distortion products are canceled if the nonlinear terms are not dependent on the control signals  $V_{c1}$  and  $V_{c2}$
- Although the linear component of the drain current is controlled by  $V_{c1-2}$ , the nonlinear components are equal in pairs ( $M_{p1}-M_{p2}$  and  $M_{n1}-M_{n2}$ ) since the drain-source voltages are equal within each pair



# MOSFET-C Filters

Design example (A. Yoshizawa - JSSC 2002)

- Ladder structure



- MOS non-linearity in-the-loop are reduced by the loop gain
- Input MOS non-linearity is cancelled by replacing a non-linear MOS with a linear resistor



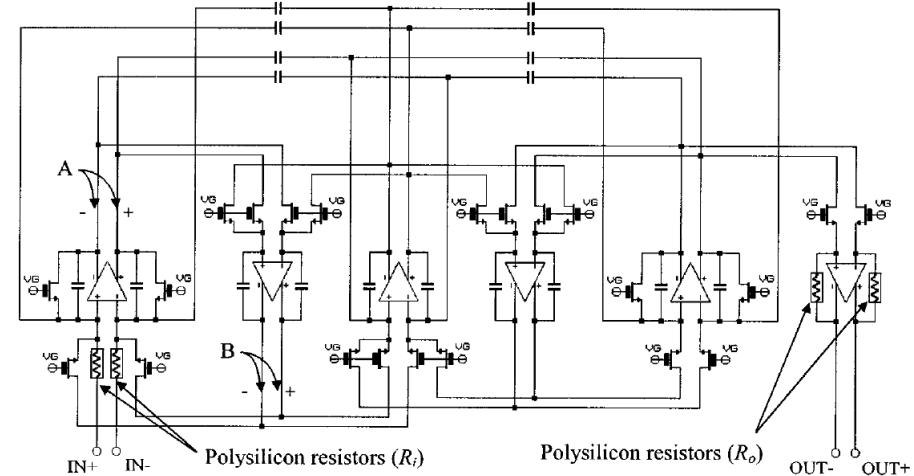
# MOSFET-C Filters

## Design example (A. Yoshizawa - JSSC 2002)

TABLE I

FILTER PERFORMANCE SUMMARY ( $T_a = 25^\circ\text{C}$ , dBm:  $50\ \Omega$ )

Supply voltage	<u>2.7 V</u>
Current consumption	<u>2.3 mA</u>
5th-order elliptic filter	0.5 mA
2nd-order phase equalizer	1.5 mA
Bias & tuning circuit	
Cut-off frequency	1.92 MHz
In-band gain	8.5 dB
Out-of-band rejection (@10 MHz)	64 dB
In-band IIP3 ( $f_1 = 1.28\ \text{MHz}$ , $f_2 = 1.44\ \text{MHz}$ )	<u>-2 dBV (+11 dBm)</u>
Out-of-band IIP3 ( $f_1 = 10\ \text{MHz}$ , $f_2 = 20.5\ \text{MHz}$ )	+28 dBV (+41 dBm)
Out-of-band IIP2 ( $f_1 = 10\ \text{MHz}$ , $f_2 = 10.5\ \text{MHz}$ )	+94 dBV (+107 dBm)
Input 1 dB compression level ( $f_1 = 1\ \text{MHz}$ )	-16 dBV (-3 dBm)
Integrated input-referred noise	-87 dBV (47 $\mu\text{VRms}$ )
Tuning system settling time (from supply voltage On)	150 $\mu\text{s}$
$V_G$ ripple level	560 $\mu\text{VRms}$



- Limited in-band linearity (1dBCP @  $\pm 600\text{mVp}$  output voltage w.r.t. the supply voltage (2.7))
  - Linearity requires large  $V_C$
  - Low-voltage reduces linear swing







*Dipartimento di Ingegneria dell' Innovazione*

*Universita' degli Studi di Lecce*

*Andrea Baschirotto*

[andrea.baschirotto@unile.it](mailto:andrea.baschirotto@unile.it)

---

## **Analog Filters for Telecommunications**

*Universita' degli Studi di Bologna*

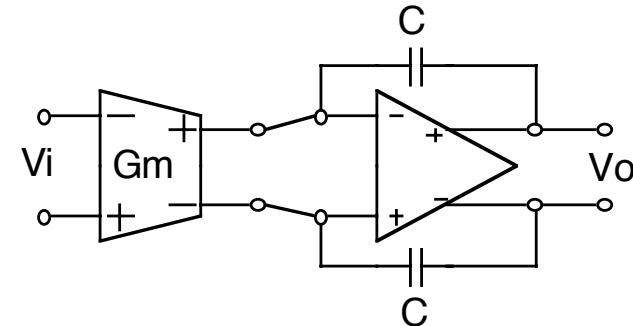
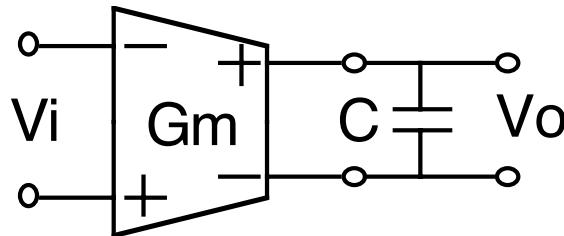
*June, 16<sup>th</sup>-17<sup>th</sup>, 2005*

## **Gm-C Filters**



# Basic Gm-C Integrator

- The basic building block is an integrator
- Gm-C Type
- Gm-C-Opamp Type

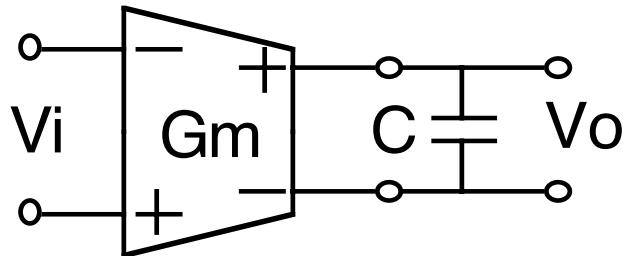


- |   |   |
|---|---|
| 😊 Fastest of all possible approaches      | 😊 Insensitive to parasitics               |
| 😊 It has not to drive low impedance loads | 😊 It has not to drive low impedance loads |
| 😢 Sensitive to parasitic capacitance      | 😊 Small output swing transconductors      |
| 😢 Large input and output signals          | 😢 Largest number of active elements       |
| 😢 Larger number of active elements        | 😢 Extra poles i.e. not very fast          |



# Outline

- Building block: the Gm-C integrator



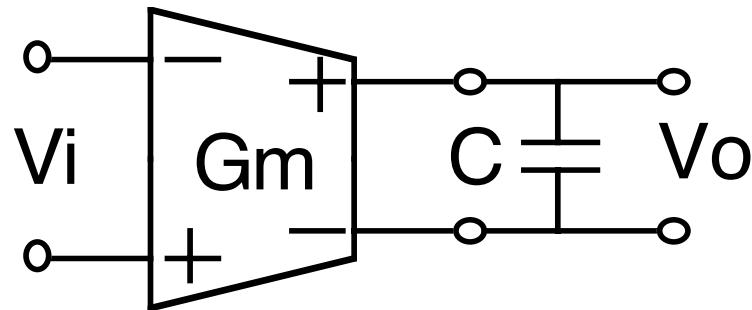
$$H(s) = \frac{V_o}{V_i} = \pm \frac{G_m}{s \cdot C}$$

- Gm-transconductor configurations
  - MOS in linear region
  - MOS in saturation region
- Transconductor limitations
  - DC-gain
  - Frequency response
  - Linearity
  - Noise
  - Tuning
- Continuous-time filter examples

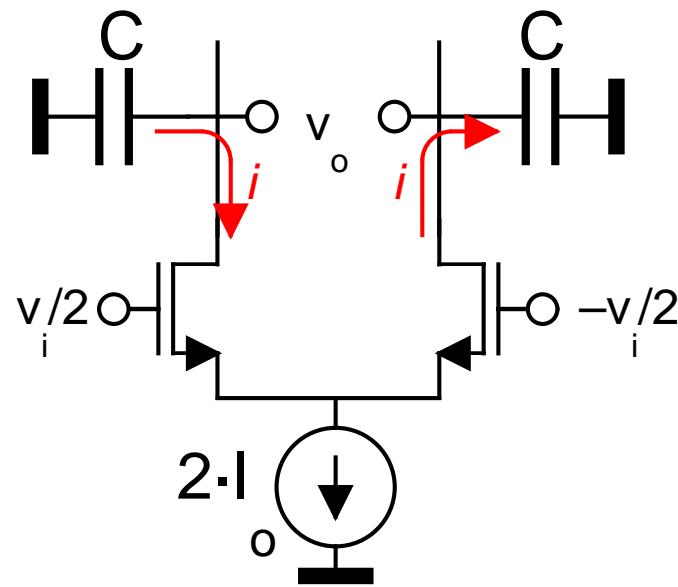


# Gm-C Filter Design

MOS in saturation region



$$H(s) = \frac{V_o}{V_i} = \pm \frac{G_m}{s \cdot C}$$



$$I_D = \frac{1}{2} \cdot \mu \cdot C_{ox} \cdot \left( \frac{W}{L} \right) \cdot (V_{GS} - V_{TH})^2$$

$$G_m = \mu \cdot C_{ox} \cdot \left( \frac{W}{L} \right) \cdot (V_{GS} - V_{TH})$$

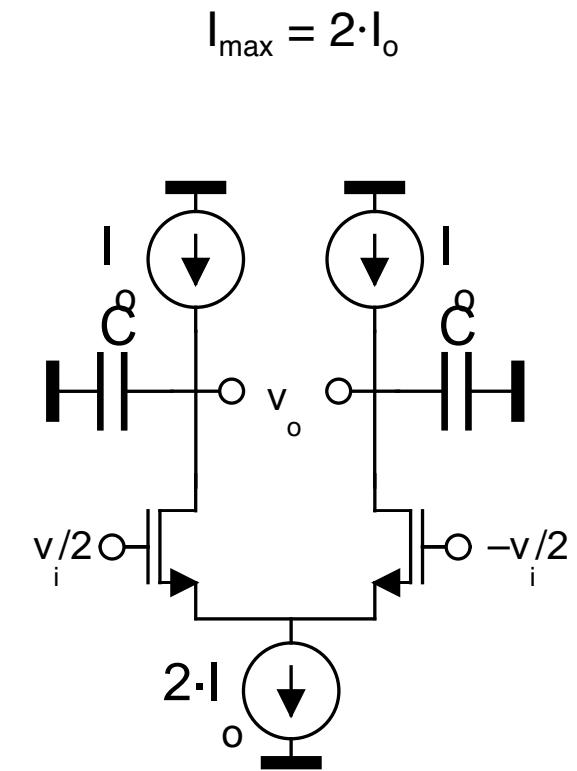
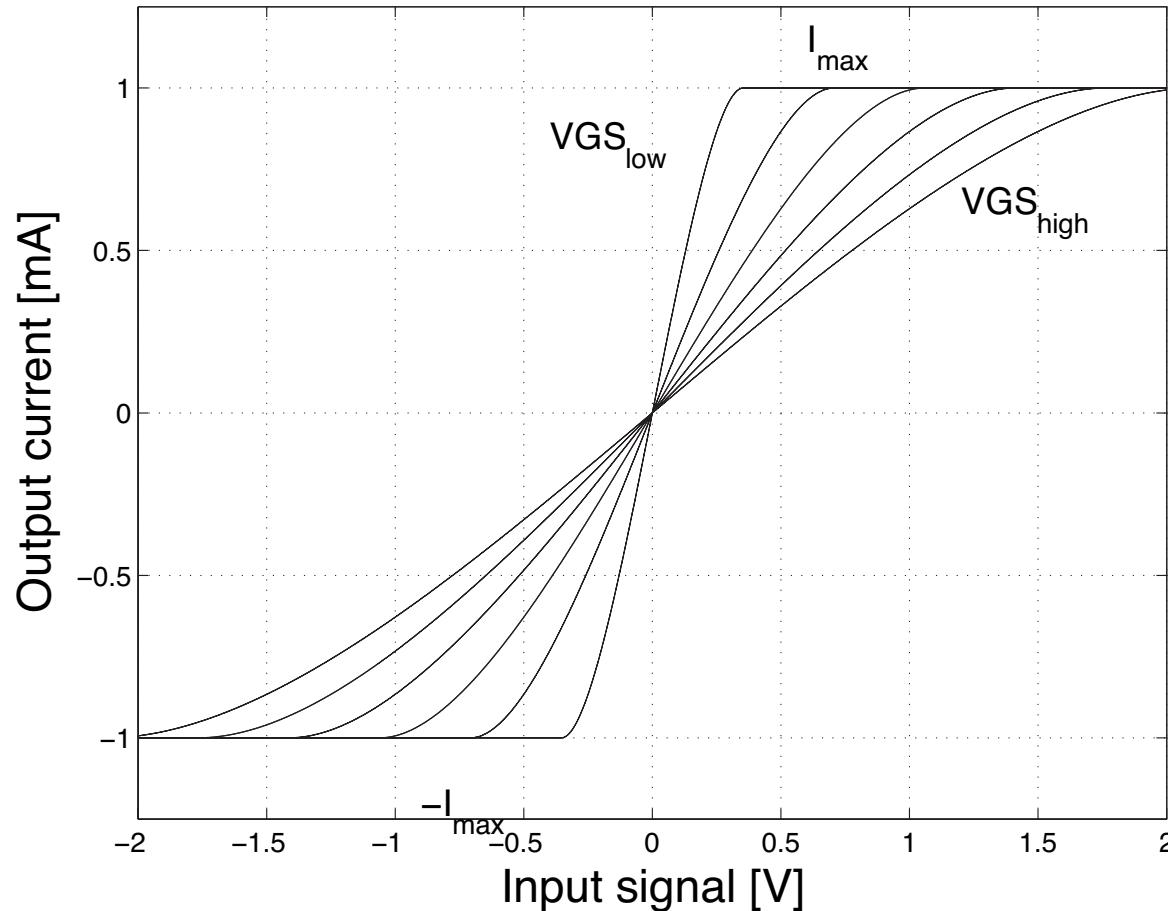
$$G_m = \frac{2 \cdot I}{V_{GS} - V_{TH}}$$



# Gm-C Filter Design

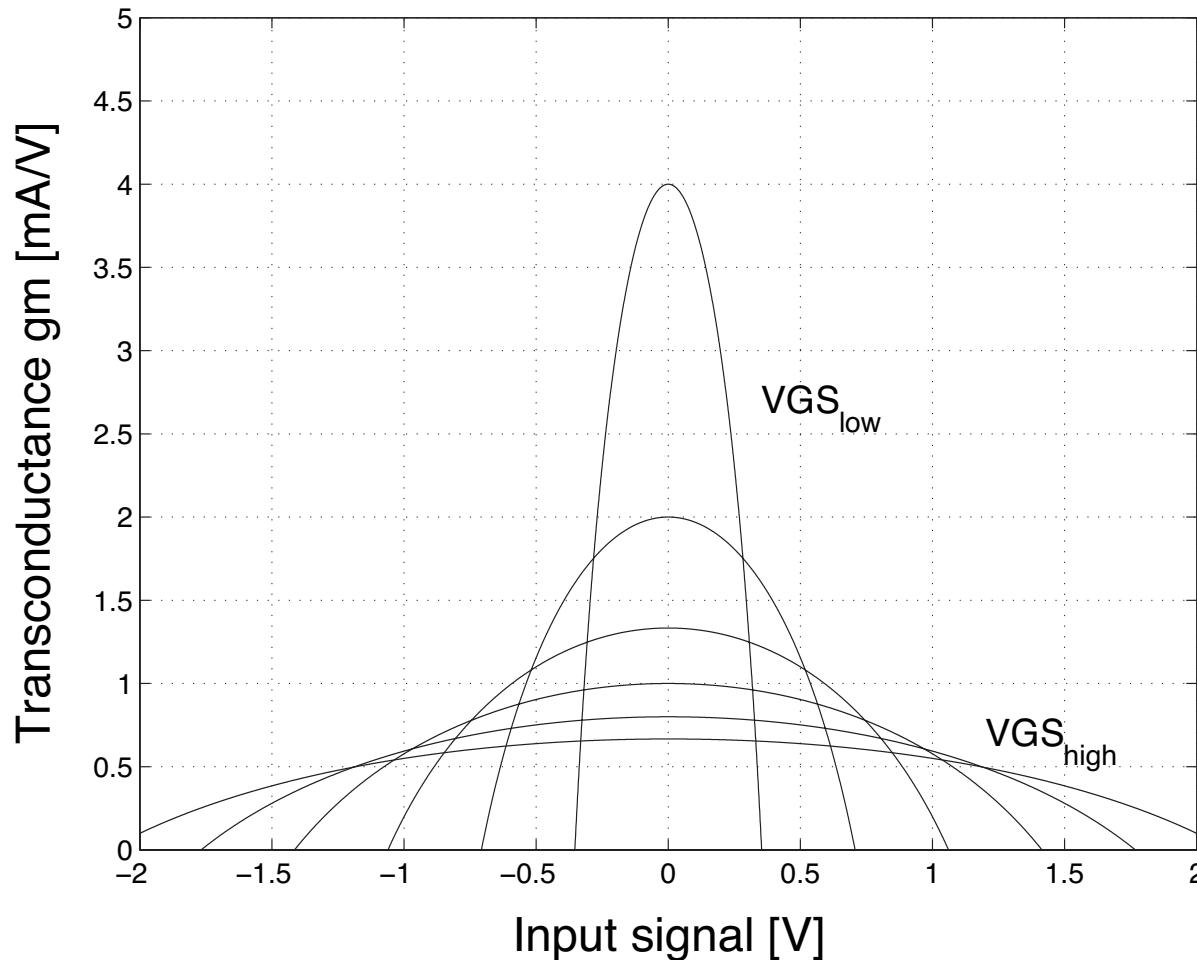
MOS in saturation region – Input linear range

- For a constant bias current  $2 \cdot I_o$



# Gm-C Filter Design

## MOS in saturation region – Input linear range



- For a constant bias current  $2 \cdot I_D$

$$g_{mo} = \mu \cdot C_{ox} \cdot (V_{GS} - V_{TH})$$

$$g_{mo} = \frac{2 \cdot I_D}{V_{GS} - V_{TH}}$$

- A higher  $g_m$  value corresponds to a smaller linear range



# Gm-C Filter Design

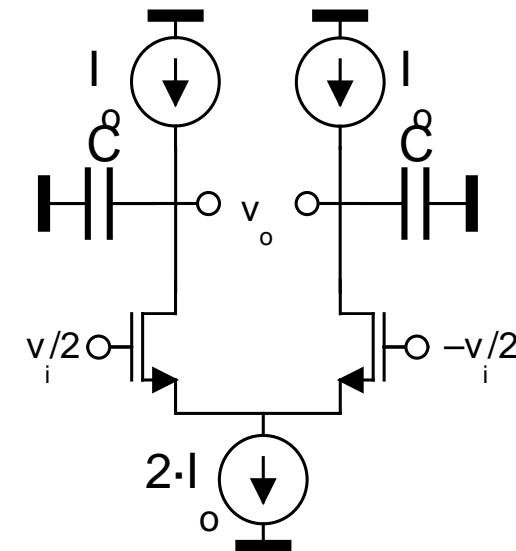
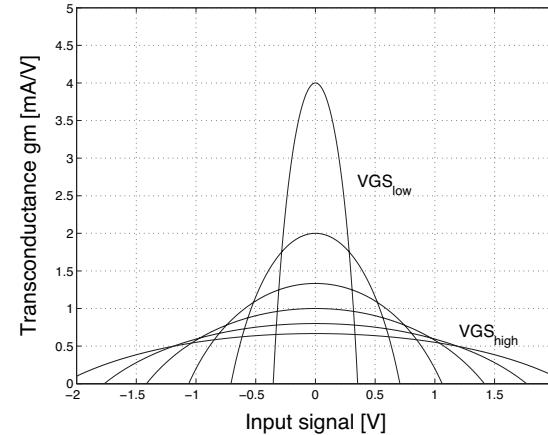
## MOS in saturation region – Input linear range

- The THD for an input voltage sinewave of the input voltage-to-current transconductor is given by:

$$THD = \frac{1}{32} \cdot \frac{V_i^2}{V_{OV}^2}$$

$$IM3 = \frac{3}{32} \cdot \frac{V_i^2}{V_{OV}^2}$$

- The sinewave stays only for a small part on the non linear region



# Gm-C Filter Design

## MOS in saturation region – Noise

- The noise of a differential pair in saturation region is:

$$\overline{V_{n\_in}^2} = 2 \cdot \frac{2}{3} \cdot 4 \cdot k \cdot T \cdot \frac{1}{g_{mo}}$$

- Large  $g_{mo}$  corresponds to
  - 😊 large Gm/C  
high frequency filters
  - 😊 low in-band noise level  $\overline{V_{n\_in}^2}$   
but the total noise is  $kT/C$  !!!
  - 😢 large bias current & power consumption  
high frequency filters

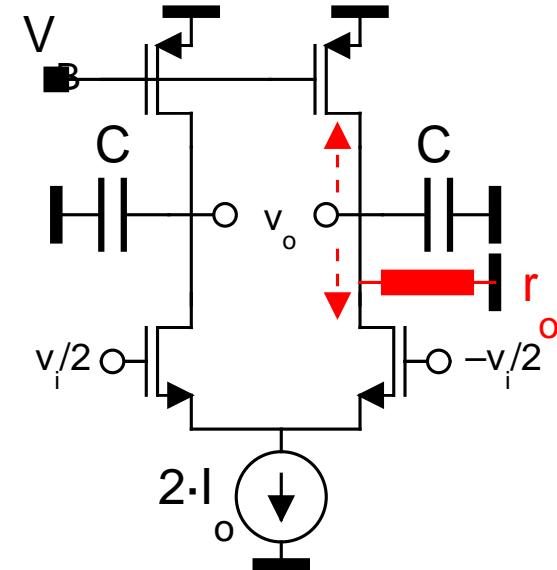
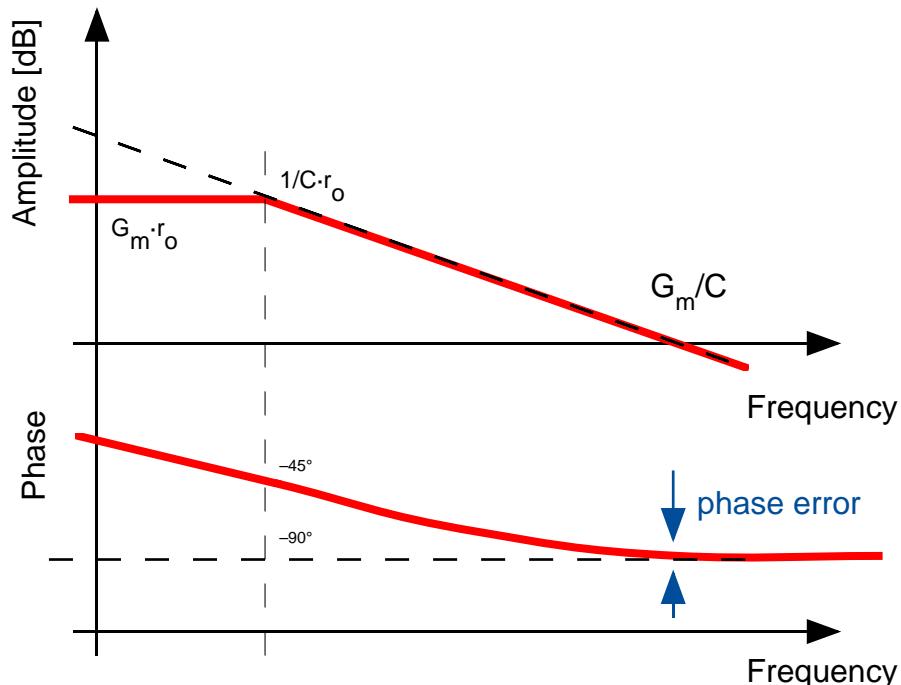


# Gm-C Filter Design

## MOS in saturation region – Output node resistance / Finite gain

- Any impedance at the output node gives a finite dc-gain
- This changes the integrator transfer function

$$H(s) = \frac{V_o}{V_i} = \pm \frac{G_m \cdot r_o}{1 + s \cdot C \cdot r_o}$$



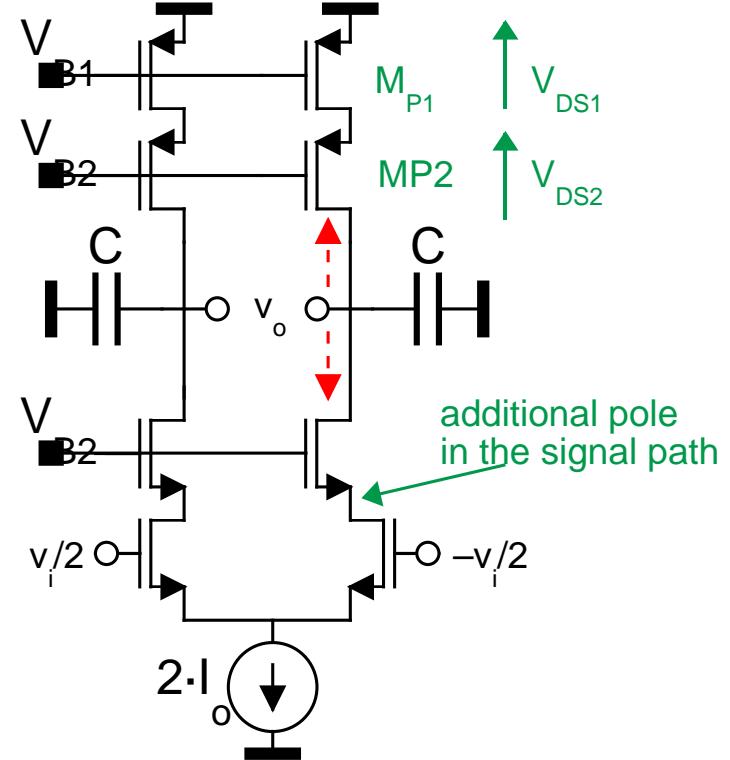
- The finite dc-gain changes the phase at the unity gain frequency
- This causes deviation in the overall filter transfer function



# Gm-C Filter Design

## MOS in saturation region – Output node resistance / Finite gain

- The dc-gain can be increased by using a cascode structure
- ☺ Cascode device designed (small W/L) to reduced output parasitic capacitance
- ☹ Reduced output swing
- ☹ Additional pole in the signal path ( $g_{mcasc}/C_{par}$ )
- ☺ Slightly increased linearity ( $V_{DS}$  of the input device is more constant)

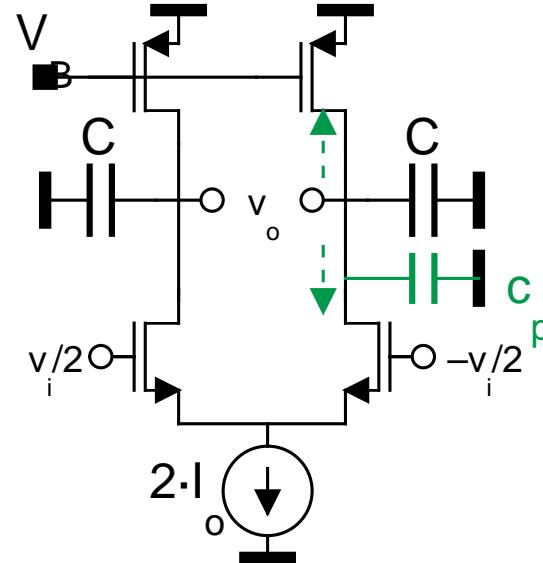


# Gm-C Filter Design

## MOS in saturation region – Parasitic capacitance

- Any parasitic capacitance at the output node is added in parallel to the load capacitance

$$H(s) = \frac{V_o}{V_i} = \pm \frac{G_m}{s \cdot (C + C_p)}$$



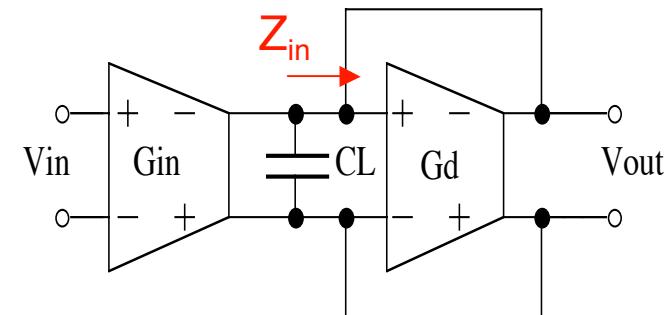
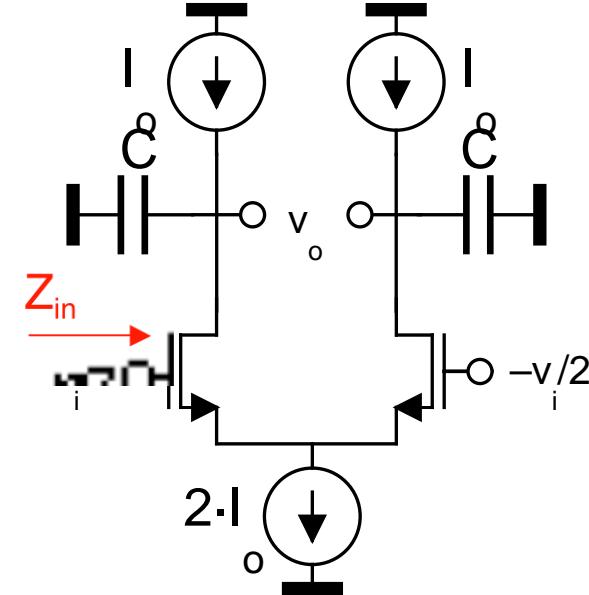
- Parasitic capacitance is due to:
  - Output transconductor capacitance
  - Output current source capacitance
  - Input following stage capacitance (Another transconductor !!)
  - Eventually-connected-circuit input capacitance (ex. CMFB)



# Gm-C Filter Design

## MOS in saturation region – Input impedance

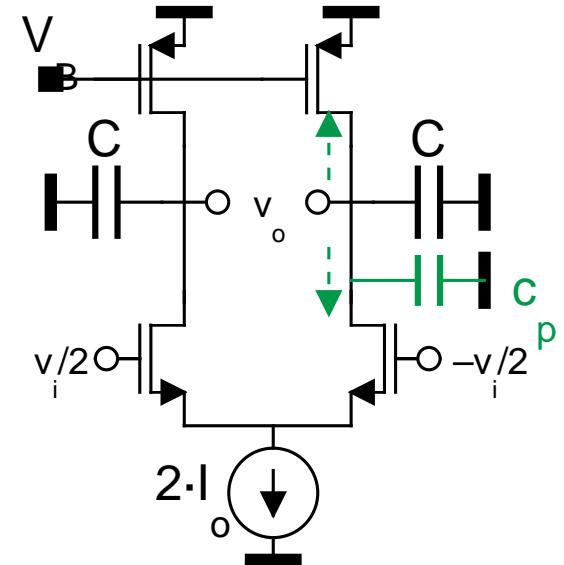
- The input impedance  $Z_{in}$  is very high
- It is only by the input capacitance
- It is an oxide capacitance → it is a “good” capacitance
- In the simple transconductor the Miller effects has to be considered
- The input impedance is the load of the previous stage
- It has to be taken into account in the total capacitance load



# Gm-C Filter Design

## MOS in saturation region – Parasitic capacitance

- Parasitic capacitance:
  - Good capacitance: Oxide ( $C_{GS}$ )
    - Constant with signal
  - Bad capacitance: Junction ( $C_D$  and  $C_S$ )
    - Dependent on signal
- Typical amount of bad parasitic capacitance  $\approx 20\%$  of the total capacitance



$$H(s) = \frac{V_o}{V_i} = \pm \frac{G_m}{s \cdot (C + C_p)} = \pm \frac{\mu \cdot C_{ox} \cdot (W/L) \cdot (V_{GS} - V_{TH})}{s \cdot (C + C_p)}$$

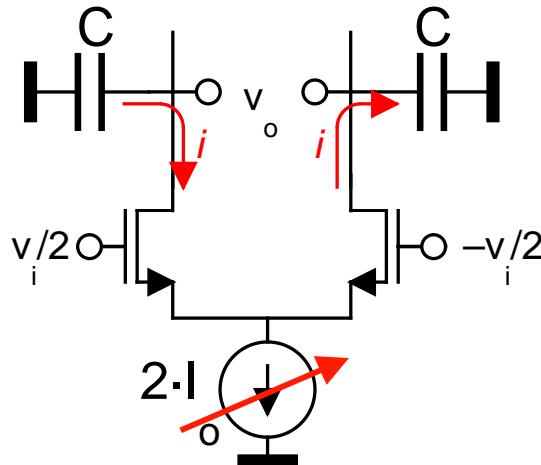
- Load capacitance should have the same dependence on technology of Gm.
- C should be done with gate capacitance  $C = C_{ox} \cdot (W/L)$

$$H(s) = \frac{V_o}{V_i} = \pm \frac{\mu \cdot C_{ox} \cdot (W/L)_M \cdot (V_{GS} - V_{TH})}{s \cdot (C_{ox} \cdot (W/L)_C + C_p)}$$



# Gm-C Filter Design

## Frequency Response Tuning



$$G_m = \frac{2 \cdot I_o}{V_{GS} - V_{TH}} = \sqrt{k \cdot I_o}$$

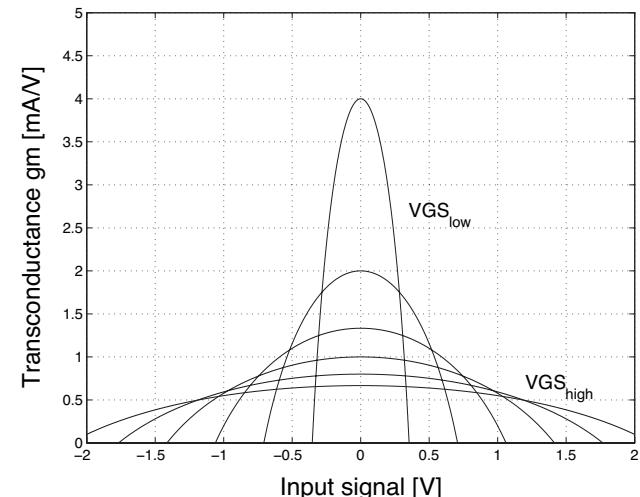
- $G_m$  and  $f_o (=G_m/C)$  are changed/tuned by controlling  $I_o$
- A quadratic law is present
  - For a factor-of-3 in  $G_m$  (i.e. in  $f_o=G_m/C$ ) the current can be changed of a factor-of-9

- The linearity depends on the  $V_{ov}$  → on the current level

$$THD = \frac{1}{32} \cdot \frac{V_i^2}{V_{ov}^2}$$

- Changing the  $G_m$  changes the **linear range**
- Higher  $G_m$ -value (for higher frequencies) gives a smaller linear range

**Linear-range vs.  $G_m$ -value trade off**



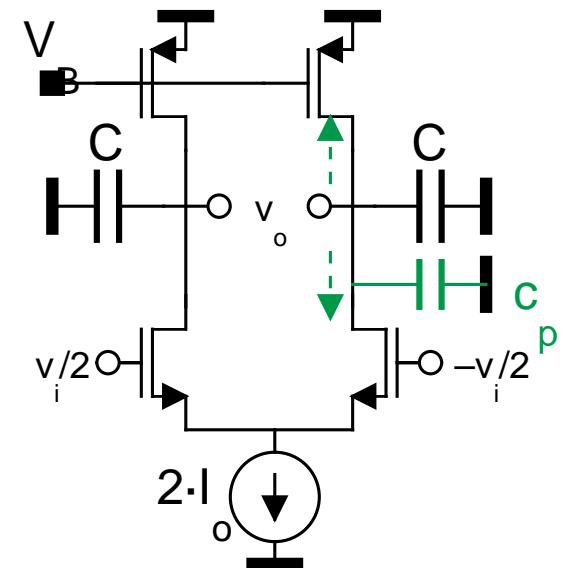
# Gm-C Filter Design

## MOS in saturation region – Output swing

- The voltage output swing is limited by the saturation-to-linear region borderline of the MOS devices (NMOS and PMOS)
- Large output swing is obtained for small  $V_{DSsat}$

$$V_{DSsat} \approx V_{ov} = V_{GS} - V_{TH} = \sqrt{\frac{I_D}{\mu \cdot C_{ox} \cdot \frac{W}{L}}}$$

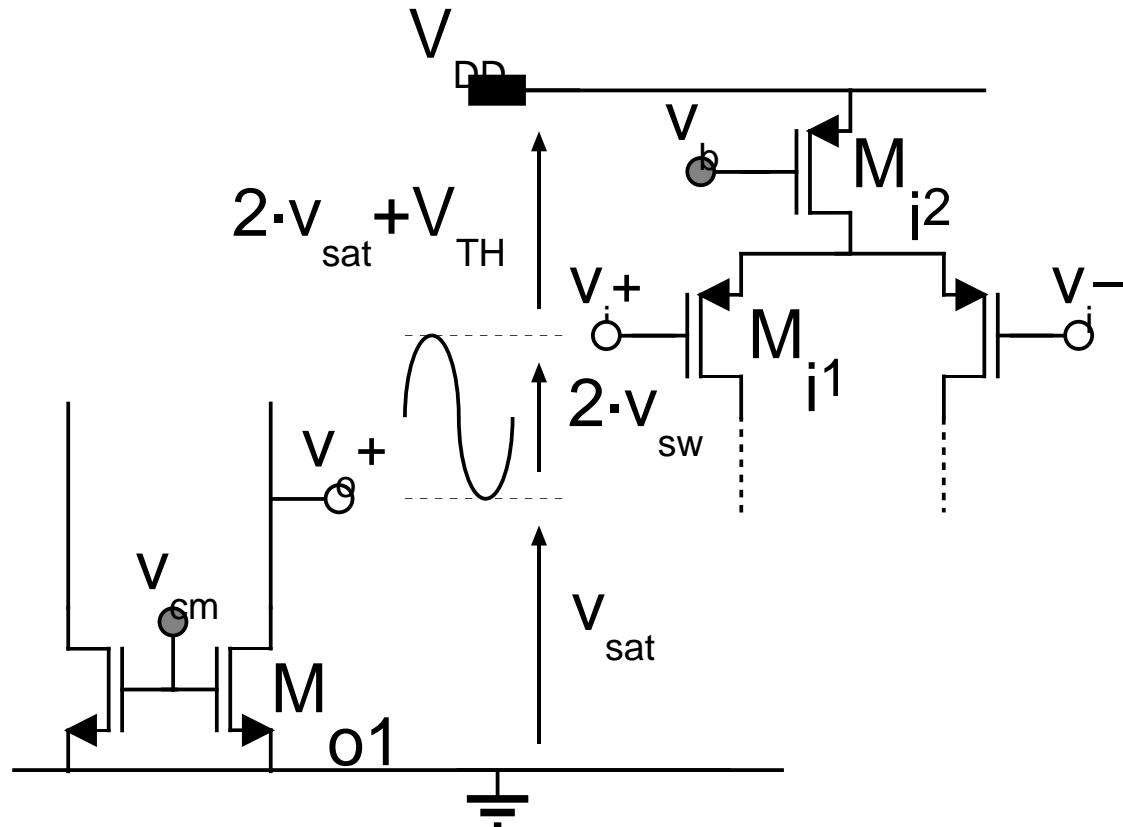
- Large output swing is obtained for large W/L
  - Large W/L presents large parasitic “bad” capacitance
- Overall linearity may be limited by output stage linearity



# Gm-C Filter Design

MOS in saturation region – Output-to-input connection

- Input and output common-mode voltages and swings have to be matched



$$V_{DDmin} = (V_{GSdiff} + V_{sat\_top}) + 2 \cdot V_{sw} + V_{sat\_bottom} = V_{TH} + 3 \cdot V_{ov} + 2 \cdot V_{sw}$$



# Gm-C Filter Design

## MOS in saturation region – Design trade-off

- The PMOS active load
- gives a bad parasitic capacitance at the output load

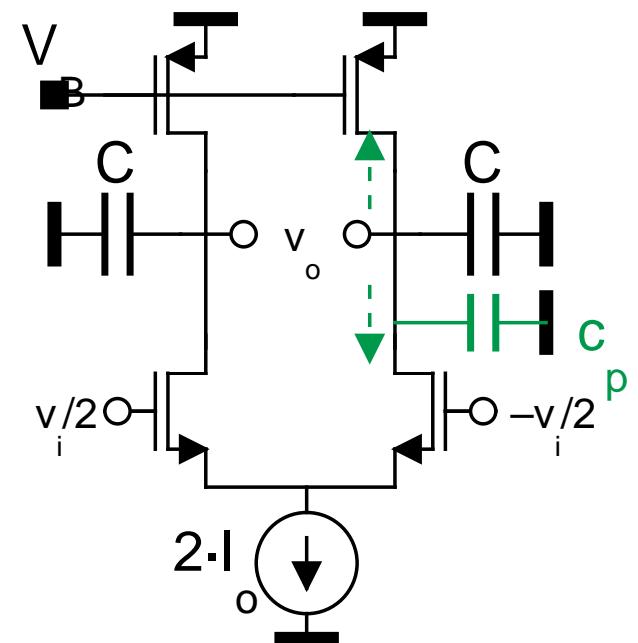
$$C_p \approx W \cdot L \quad \text{to be minimized}$$

- gives a output impedance

$$r_o \approx L \quad \text{to be maximized}$$

- reduces the output swing

$$V_{DSSat} \approx 1/(W/L) \quad \text{to be minimized}$$



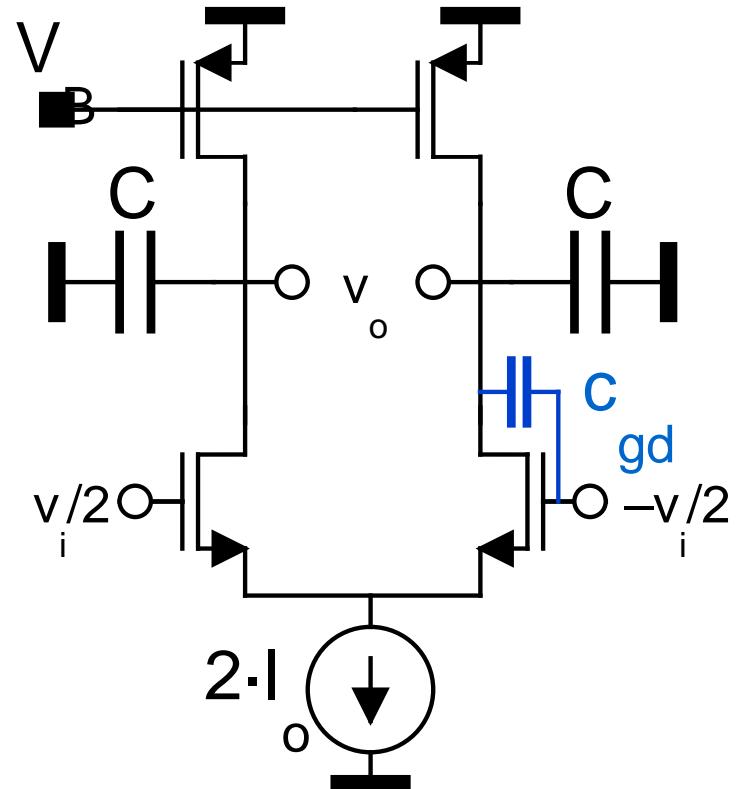
# Gm-C Filter Design

## C<sub>GD</sub> Right-hand-plane zero

- The C<sub>GD</sub> of the input device add a Right-hand-plane zero

$$H(s) = \frac{V_o}{V_i} = \pm \frac{G_m}{s \cdot C} \cdot \left( 1 - \frac{G_m}{s \cdot C_{GD}} \right)$$

- The Right-hand-plane zero changes filter frequency response



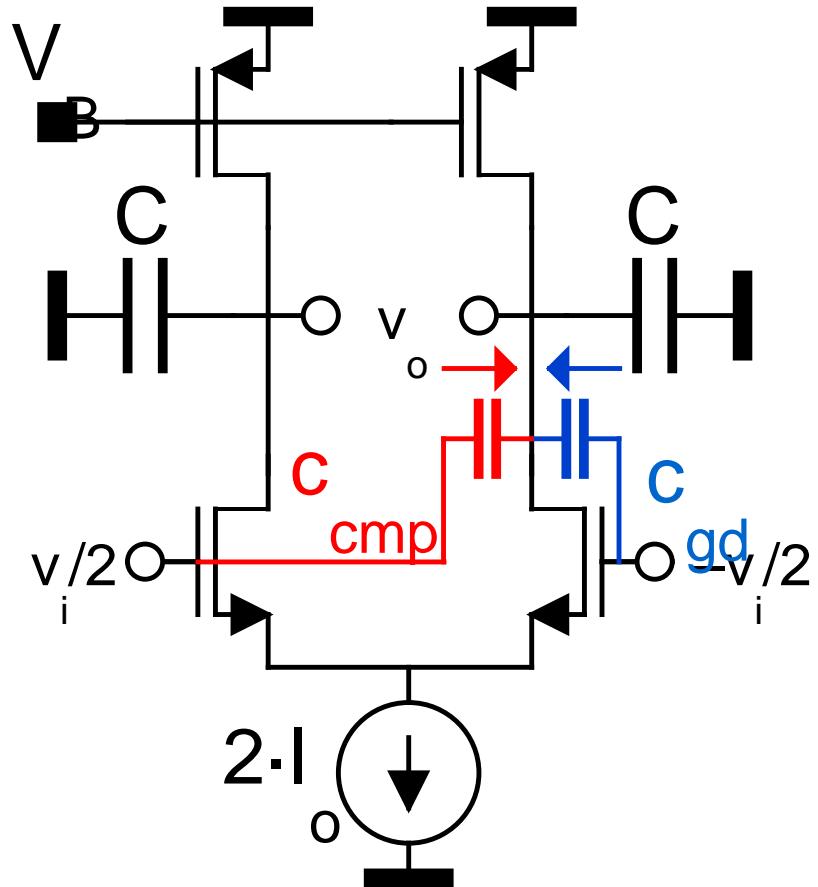
# Gm-C Filter Design

## C<sub>GD</sub> Right-hand-plane zero

- Capacitance C<sub>cmp</sub> injects an opposite amount of charge injected by C<sub>GD</sub>
- It cancels C<sub>GD</sub> effects (RHP zero)

$$H(s) = \frac{V_o}{V_i} = \pm \frac{G_m}{s \cdot C} \cdot \left( 1 - \frac{G_m}{s \cdot C_{GD}} + \frac{G_m}{s \cdot C_{cmp}} \right)$$

- Capacitor C<sub>cmp</sub> has to track C<sub>GD</sub>
  - A MOS capacitor is used ( $\approx 1/3 M_{in}$ )
- Capacitor C<sub>cmp</sub> changes integrator phase
  - C<sub>cmp</sub> may be used for Q-tuning



# Gm-C Filter Design

## Frequency response accuracy

- Ideal integrator frequency response

$$H_i(s) = \frac{\omega_o}{s} = \frac{G_m}{s \cdot C_L}$$

- Non-ideal effects

- Output impedance ( $r_o$ ) and resistive load/next stage ( $R_L$ )  $\rightarrow R_T = R_L // r_o$
- Output capacitance ( $C_o$ ) and capacitive load/next stage ( $C_x$ )  $\rightarrow C_T = C_L // C_o // C_x$
- $G_m$  single-pole frequency response  $G_m(s) = G_m/(1+s/\omega_p)$

- Real integrator frequency response

$$H_a(s) = \frac{G_m}{1+s/\omega_p} \cdot \left( R_T // \frac{1}{s \cdot C_T} \right) = H_i(s) \cdot M(s)$$

$$M(s) = \frac{1}{1+s/\omega_p} \cdot \frac{1}{1+\frac{C_o + C_x}{C_L}} \cdot \frac{1}{1+s \cdot C_T \cdot R_T}$$



# Gm-C Filter Design

## Frequency response accuracy

$$M(s) = \frac{1}{1+s/\omega_p} \cdot \frac{1}{1+\frac{C_o + C_X}{C_L}} \cdot \frac{1}{1+s \cdot C_T \cdot R_T}$$

- $C_o$  and  $C_X$  effects cause a magnitude error at  $\omega_o$  and their effect is negligible
- $R_T$  results in a low-dc-gain and results in a phase error (lead)
- $\omega_p$  gives a phase error (lag)
- Eventual RHS zeros gives a phase error
  
- Design example:  $\omega_o = 2\pi \cdot 44\text{MHz}$ 
  - DC-gain  $A_o = 40\text{dB} \rightarrow \Delta\phi(\omega_o) = +0.57^\circ$
  - $\phi(\omega_o) = -91.9^\circ$ 
    - $\rightarrow \omega_p$  contribution  $= -1.9^\circ - 0.57^\circ = -2.47^\circ$
    - $\rightarrow \omega_p \approx 2\pi \cdot 1.02\text{GHz}$   $(44\text{MHz} \cdot [360^\circ/(2\pi)] / 2.47^\circ)$



# Gm-C Filter Design

## Integrator Phase Error $\Delta\phi$

- Let's define

$$Q_{\text{int}} = \frac{1}{\Delta\phi[\text{rad}]}$$

- $\Delta\phi = -1.9^\circ \rightarrow Q_{\text{int}} = 1 / (-1.9^\circ / [360^\circ/(2\pi)]) = -30$
- Effects on a  $Q_b=1.5$  biquad
  - The biquad is made up of two integrators  $\rightarrow Q_{\text{bqd}} = Q_{\text{int}} / 2 = -15$
  - The actual Q value is
$$Q_{\text{act\_bqd}} = \frac{1}{1/Q_{\text{bqd}} + 1/Q_b} = 1.666$$
  - A 10% deviation results
- The above example gives a guideline for  $\Delta\phi$  deviation



# Gm-C Filter Design

## Integrator Phase Error $\Delta\phi$ Effects

- Example: Biquadratic cell design

- $\omega_0 = 2\pi \cdot 100\text{MHz}$
- $Q_b = 5$
- $\Delta Q/Q < 10\%$

$$Q_{act\_bqd} = \frac{1}{1/Q_{bqd} + 1/Q_b} \implies \frac{\Delta Q}{Q_b} = \frac{Q_{act\_bqd}}{1/Q_{bqd}} < 10\%$$

$$\rightarrow 1/Q_{bqd} < 0.1 / 5 \rightarrow Q_{bqd} > 50 \rightarrow Q_{int} > 100$$

- About the phase error

$$\Delta\phi[\text{rad}] = \frac{1}{Q_{int}} < 0.01 \text{ rad} = 0.57^\circ$$

$$\omega_p > 2\pi \cdot Q_{int} \cdot 100\text{MHz} = 2\pi \cdot 10\text{GHz}$$

- A positive  $\Delta\phi$  (phase lag) increases the biquad  $Q$ -factor
- A negative  $\Delta\phi$  (phase lead) decreases the biquad  $Q$ -factor (damping)



# Gm-C Filter Design

## Integrator Finite Gain & Phase Error $\Delta\phi$ Effects

- An integrator finite gain  $A_o$  gives an integrator  $Q$

$$Q = A_o$$

- This gives a *ALWAYS NEGATIVE* biquad  $\Delta Q/Q$  given by:

$$\frac{\Delta Q}{Q} \cong -\frac{2 \cdot Q}{A_o}$$

- An integrator phase error  $\Delta\phi$  gives an integrator  $Q$



# Gm-C Filter Design

## Linear range for telecom systems

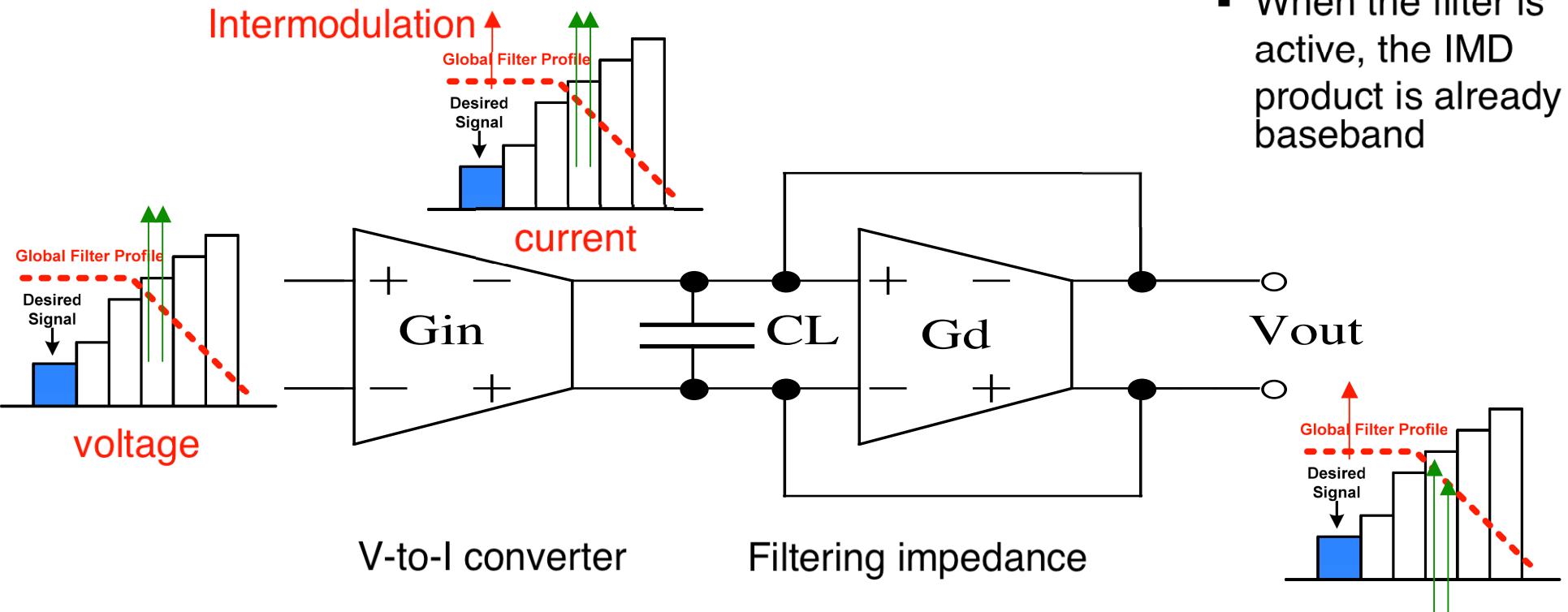
- The input stage linear range must be very large

- Ex. 1<sup>st</sup> order filter

$$H(s) = G_{in} \cdot \frac{1}{G_d + s \cdot C_L}$$

- The distortion occurs on the  $G_{in}$  output current i.e. **BEFORE** the filtering

- When the filter is active, the IMD product is already in baseband



# Gm-C Filter Design

## Linearization techniques

- The input stage linear range may be improved by:
  - Saturated MOS & circuit topology for the input stage
    - Cross-coupling topology
    - Degeneration
      - Resistor
      - Triode MOS
      - Saturation MOS
  - Triode MOS



# Linearization technique

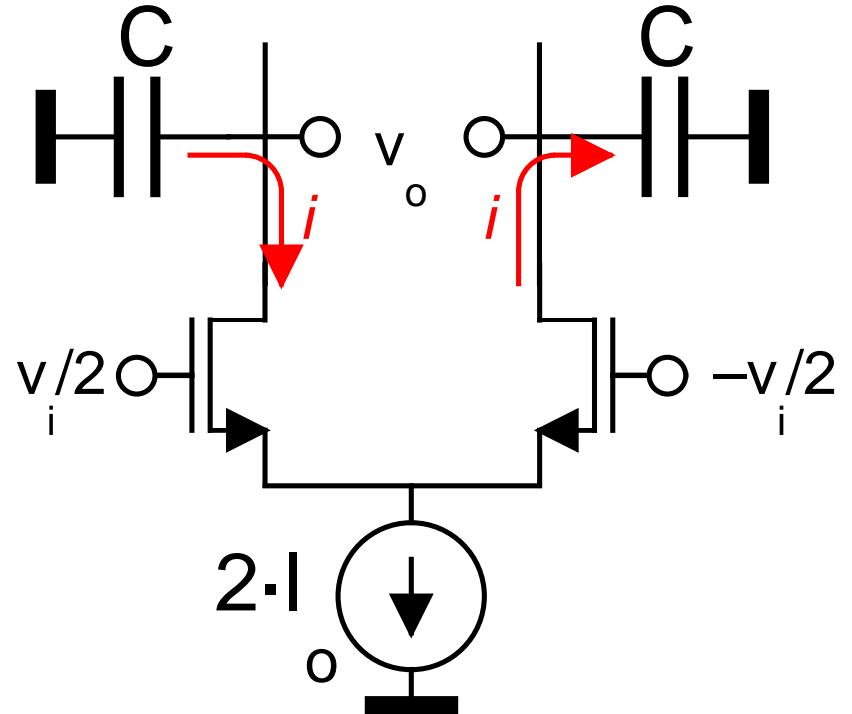
## Cross coupled structure (I)

$$I_D = \frac{k}{2} \cdot (V_{GS} - V_{TH})^2$$

- For  $k \gg \frac{k \cdot V_{in}^2}{8}$

$$I_{out} = \sqrt{\frac{k}{2}} \cdot V_{in} \cdot \sqrt{1 - \frac{k \cdot V_{in}^2}{8}} \approx \sqrt{\frac{k \cdot I}{2}} \cdot V_{in} \cdot \left(1 - \frac{k \cdot V_{in}^2}{8}\right)$$

$$I_{out} \approx \sqrt{\frac{k \cdot I}{2}} \cdot V_{in} - \frac{1}{16} \cdot \sqrt{\frac{k^3}{2 \cdot I}} \cdot V_{in}^3$$



- It is clear the 3<sup>rd</sup> order harmonic origin



# Linearization technique

## Cross coupled structure (II)

- Using two differential stages with different K values ( $K_1$  and  $K_2$ ) improves the linearity

$$I_{out1} \approx \sqrt{\frac{k_1 \cdot I_1}{2}} \cdot V_{in} - \frac{1}{16} \cdot \sqrt{\frac{k_1^3}{2 \cdot I_1}} \cdot V_{in}^3$$

$$I_{out2} \approx \sqrt{\frac{k_2 \cdot I_2}{2}} \cdot V_{in} - \frac{1}{16} \cdot \sqrt{\frac{k_2^3}{2 \cdot I_2}} \cdot V_{in}^3$$

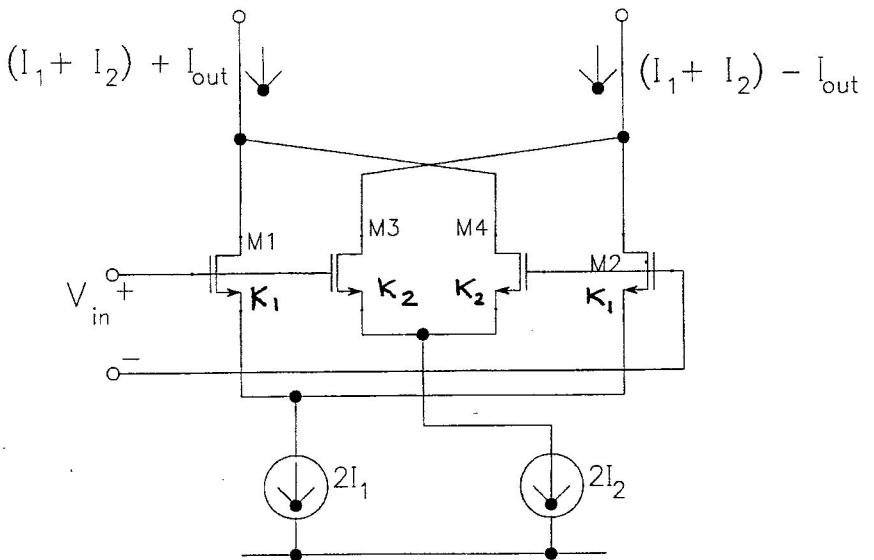
- $K$ 's and (W/L)'s are chosen

$$\frac{k_1^3}{I_1} = \frac{k_2^3}{I_2} \quad i.e. \quad \frac{(W/L)_1^3}{I_1} = \frac{(W/L)_2^3}{I_2}$$

- The total output current is

$$I_{out} = I_{out1} - I_{out2} \approx \left( \sqrt{\frac{k_1 \cdot I_1}{2}} \cdot V_{in} - \frac{1}{16} \cdot \sqrt{\frac{k_1^3}{2 \cdot I_1}} \cdot V_{in}^3 \right) - \left( \sqrt{\frac{k_2 \cdot I_2}{2}} \cdot V_{in} - \frac{1}{16} \cdot \sqrt{\frac{k_2^3}{2 \cdot I_2}} \cdot V_{in}^3 \right)$$

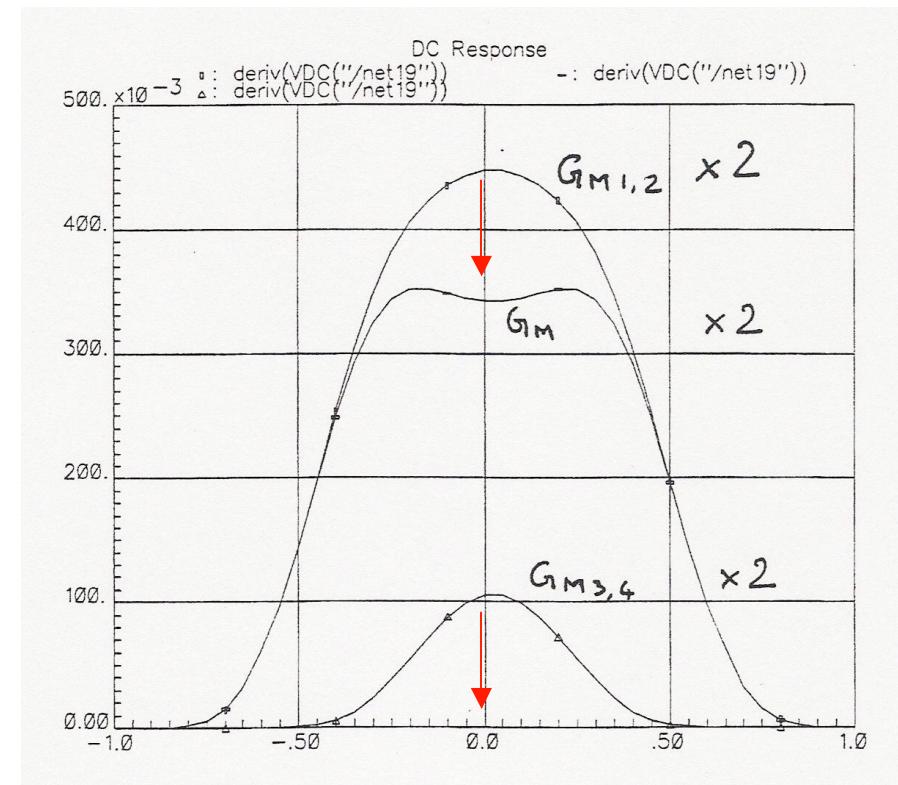
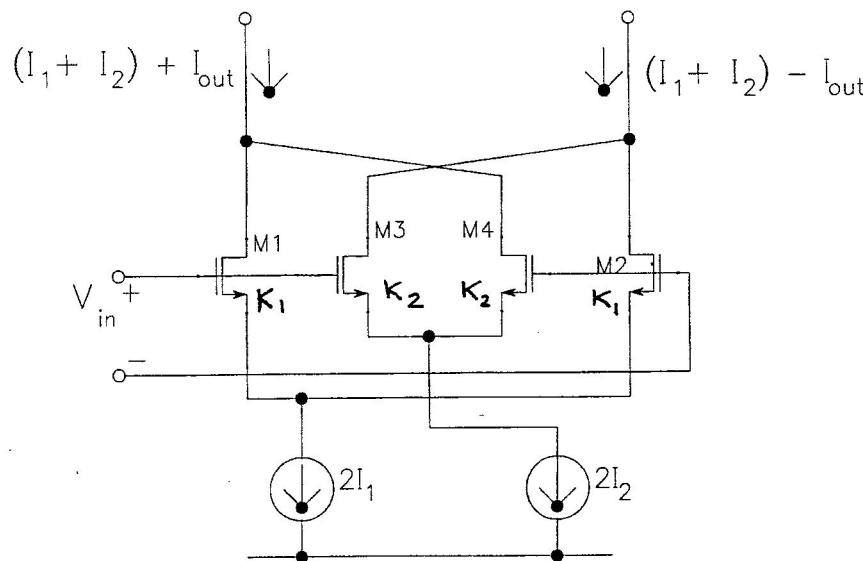
$$I_{out} \approx \left( \sqrt{\frac{k_1 \cdot I_1}{2}} - \sqrt{\frac{k_2 \cdot I_2}{2}} \right) \cdot V_{in} \quad \text{no 3rd order harmonic !!!}$$



# Linearization technique

## Cross coupled structure (III)

$$I_{out} \approx \left( \sqrt{\frac{k_1 \cdot I_1}{2}} - \sqrt{\frac{k_2 \cdot I_2}{2}} \right) \cdot V_{in}$$



# Linearization technique

## Source degeneration

- MOS in saturation region

$$G_m = g_m$$

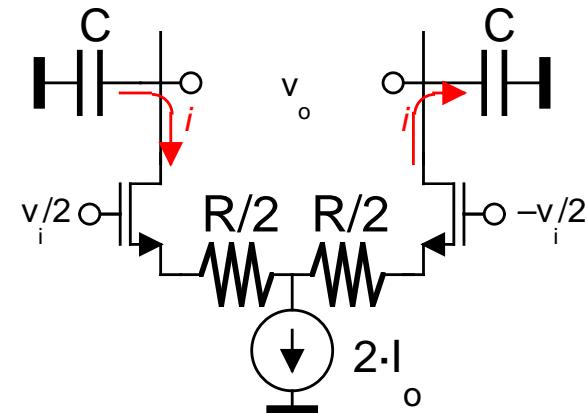
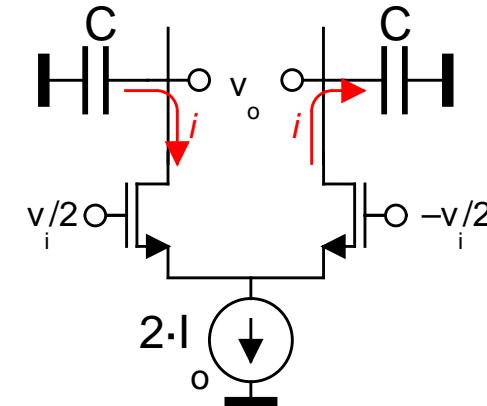
$$THD = \frac{1}{32} \cdot \frac{V_i^2}{V_{ov}^2}$$

- Degenerated MOS

$$G_m = \frac{g_m}{1 + g_m \cdot R}$$

$$\frac{1}{n} = \frac{1}{1 + g_m \cdot R}$$

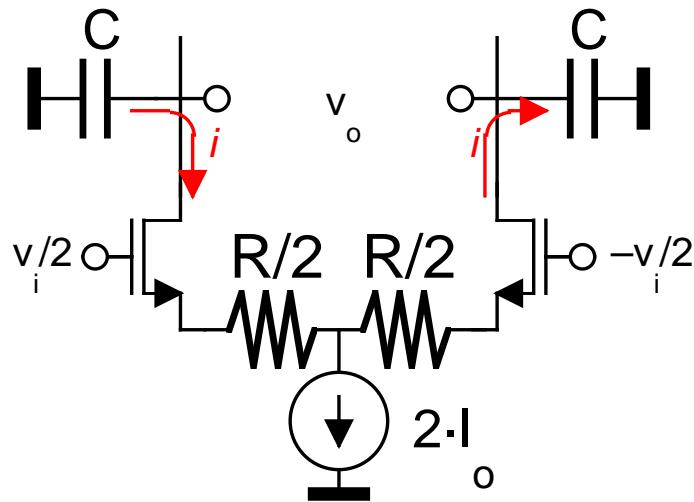
$$THD = \frac{1}{32} \cdot \frac{V_i^2}{(n \cdot V_{ov})^2}$$



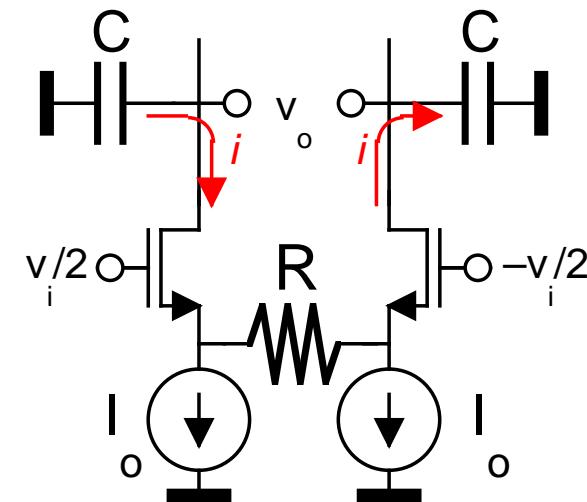
# Gm-C Filter Design

Degenerated MOS – Input linear range

- Sol. 1



- Sol. 2



- ⌚ DC-voltage drop (loss) across  $R/2$
- ⌚ Eventual  $R/2$ 's mismatch

- 😊 More compact
- ⌚ Eventual  $I_o$ 's mismatch



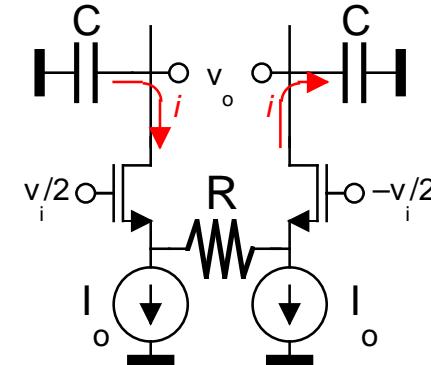
# Linearization technique

## Source degeneration

- Degenerated MOS

$$n = 1 + g_m \cdot R$$

$$THD = \frac{1}{32} \cdot \frac{V_i^2}{(n \cdot V_{ov})^2}$$



- Extra linearity costs:

- Higher noise

$$\overline{V_{n\_in}^2} = 2 \cdot \frac{2}{3} \cdot 4 \cdot k \cdot T \cdot \frac{1}{g_{mo}} + 4 \cdot k \cdot T \cdot R \approx 2 \cdot \frac{2}{3} \cdot 4 \cdot k \cdot T \cdot \frac{1}{g_{mo}} \cdot (n)$$

- Lower Gm-value

$$G_m = \frac{g_m}{1 + g_m \cdot R} = \frac{g_m}{n}$$

- Lower cut-off frequency

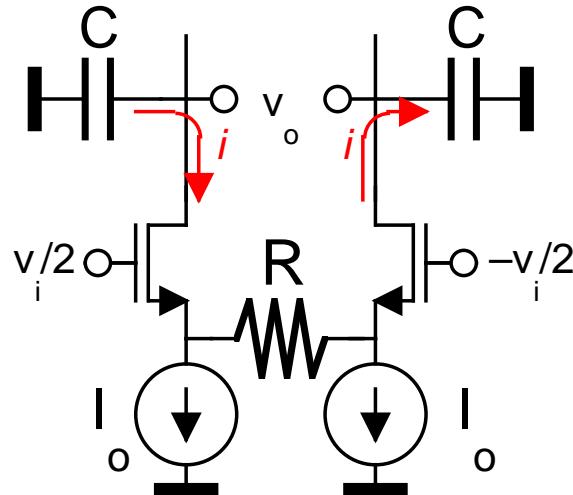
- The same cut-off frequency with larger linearity costs power consumption



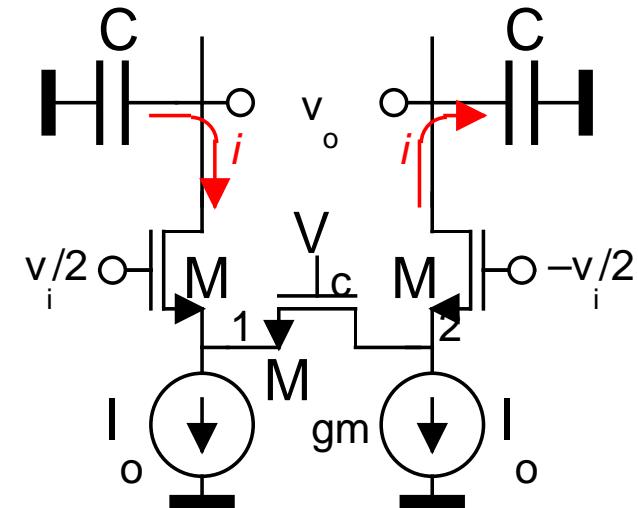
# Linearization technique

## Source degeneration

- Resistive Degeneration



- MOS Degeneration



😊 R is very linear

😢 Only digital tuning

😢 Resistor in CMOS technology

😢 MOS is less linear

▪ (complicate circuits for linearization)

😊 Continuous-tuning

😊 MOS-only solution



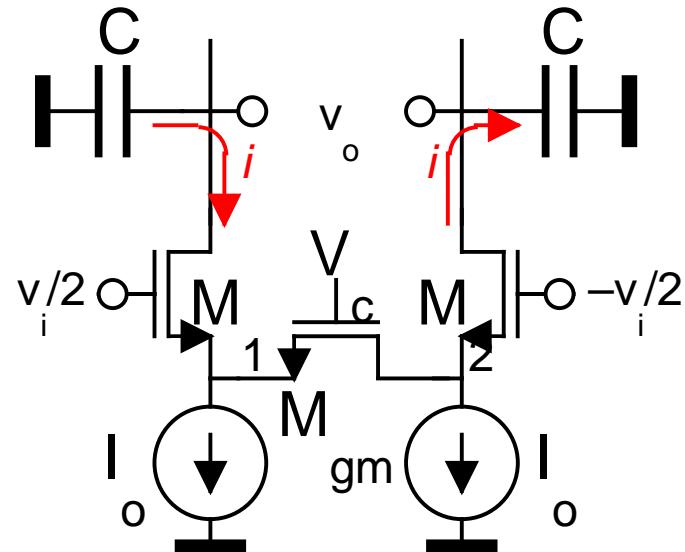
# Linearization technique

## Source degeneration - Triode MOS

- For small values of  $V_{DS}(<<V_{DSsat})$ , MGm is a near ideal resistor in triode

$$I_D = \mu \cdot C_{ox} \cdot \left( \frac{W}{L} \right) \cdot \left[ (V_{GS} - V_{TH}) \cdot V_{DS} - \frac{V_{DS}^2}{2} \right] \approx \mu \cdot C_{ox} \cdot \left( \frac{W}{L} \right) \cdot (V_{GS} - V_{TH}) \cdot V_{DS}$$

$$g_{ds} \approx \mu \cdot C_{ox} \cdot \left( \frac{W}{L} \right) \cdot (V_{GS} - V_{TH}) \approx \mu \cdot C_{ox} \cdot \left( \frac{W}{L} \right) \cdot (V_C - V_S - V_{TH})$$



- Assuming  $G_{mM1\&2} \gg g_{dsMGm}$ ,
  - The overall  $G_m = g_{ds}$
  - $g_{ds}$  is tunable with  $V_C$
  - Tuning does not change bias current and power consumption
  - Increased linear range

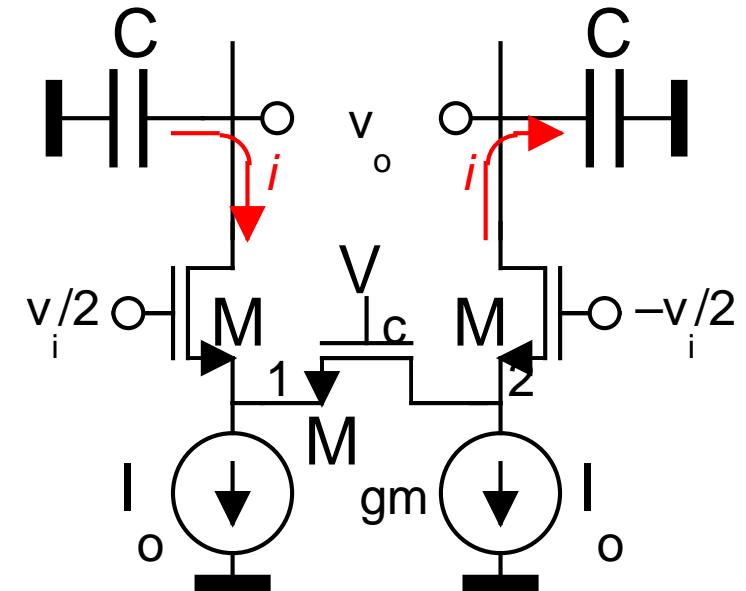


# Linearization technique

## Source degeneration improvements - Triode MOS

- Possible improvements

- Linearity:
  - Two cross-coupled pairs reduce odd-order non-linearities and substrate effects
- Tuning range:
  - For large tuning range, M1&M2 can be replaced by source followers/opamps
  - Two separate degenerating transistors with different bias voltages and adaptive tail current biasing increases the tuning range



- Critical points

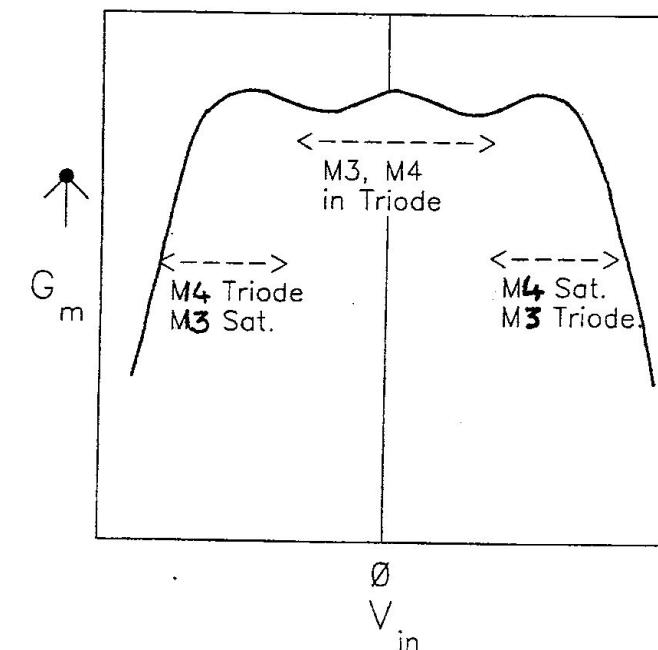
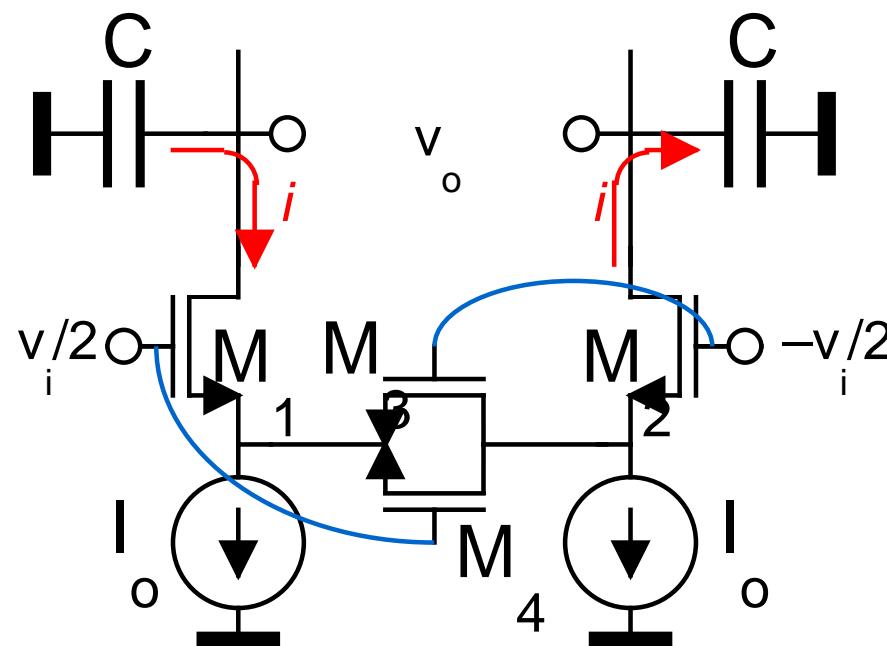
- For large input signal,  $V_{DS}$  increases, resulting in a reduced and non-linear  $G_m$  value
- The signal swing reduces the effective tuning voltage ( $V_{GS}-V_{TH}$ ) of the triode



# Improved Linearization Technique

Triode MOS - Krummenacher solution [JSSC 1998]

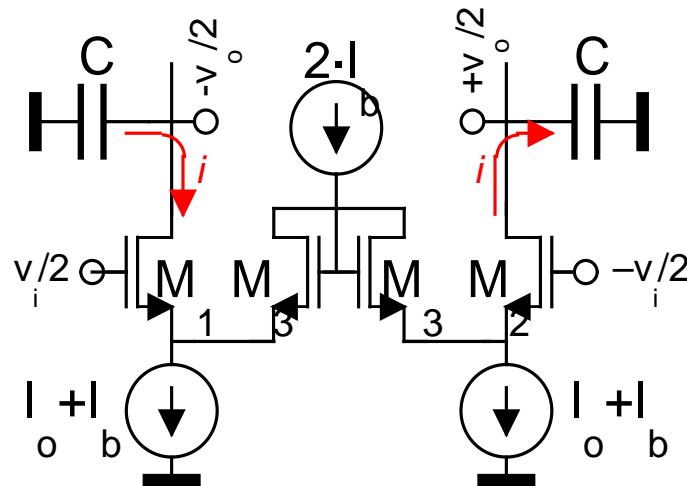
- For small  $V_{in}$ , both  $M_3$ & $M_4$  are in triode region
  - The circuit behaves as the previous linearization technique
- For larger  $V_{in}$ ,  $M_3$  stays in triode region,  $M_4$  enter in saturation
  - The  $G_m$  is determined by the  $g_{ds}$  of  $M_3$
  - The  $G_m$  linearity is increased



# Improved Linearization Technique

## Saturated MOS

- $M_3 \& M_4$  are in saturation region



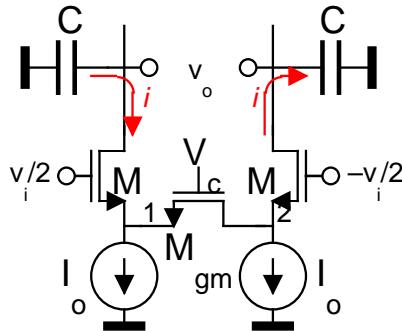
- The degeneration resistance is the  $M_3 \& M_4$  diode impedance ( $1/g_{m3}$ )

$$\frac{g_{m1}}{1 + \frac{g_{m1}}{g_{m3}}}$$



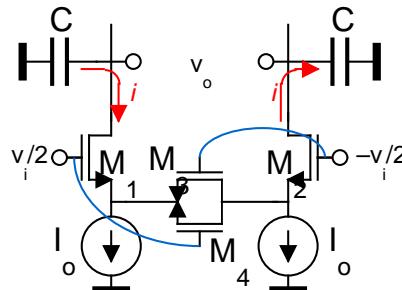
# Gm-C Filter Design

## Linearization techniques comparison



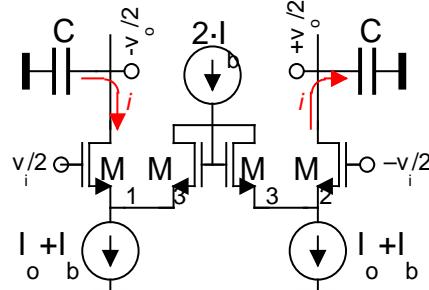
$$R = \frac{1}{\mu \cdot Cox \cdot (V_{GS} - V_{TH})}$$

- High sensitivity to CM input signals
- Large linearity requires large V<sub>GS</sub>
- Large tuning range if V<sub>C</sub> is used



$$\frac{g_{m1}}{1 + \frac{\beta_1}{4 \cdot \beta_3}}$$

- Low sensitive to CM input signals
- Linearity is limited to V<sub>in</sub> < V<sub>Dsat</sub>
- THD ≈ -50dB



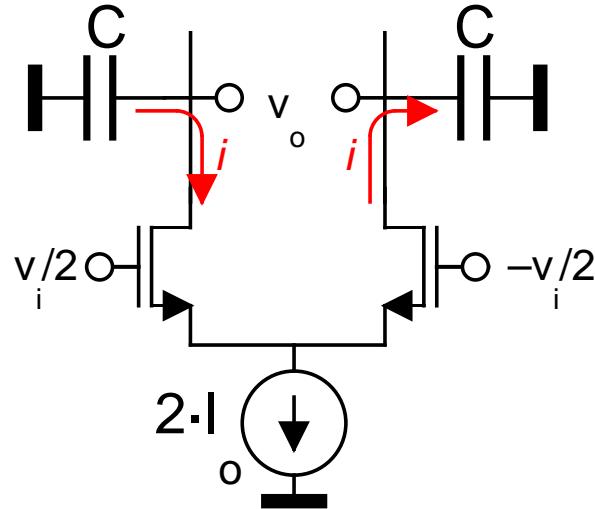
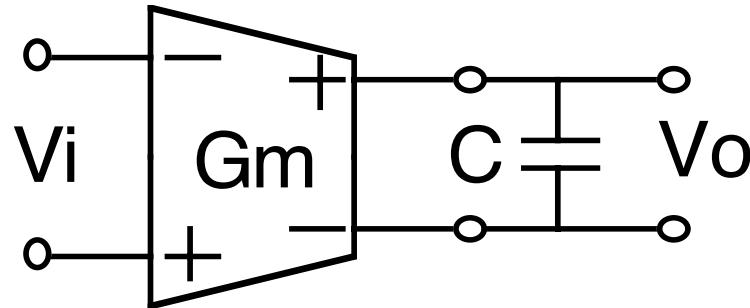
$$\frac{g_{m1}}{1 + \frac{g_{m1}}{g_{m3}}}$$

- Low sensitive to CM input signals
- Limited linearity improvement, HD3 reduces by -12dB
- Larger silicon area



# Gm-C Filter Design

MOS in linear region



$$H(s) = \frac{V_o}{V_i} = \pm \frac{G_m}{s \cdot C}$$

$$I_D = \mu \cdot C_{ox} \cdot \left( \frac{W}{L} \right) \cdot \left[ (V_{GS} - V_{TH}) \cdot V_{DS} - \frac{V_{DS}^2}{2} \right]$$

$$G_m = \mu \cdot C_{ox} \cdot \left( \frac{W}{L} \right) \cdot V_{DS}$$

- Input MOS differential pair devices have to be maintained in linear region
  - Dedicated circuits are needed



# Gm-C Filter Design

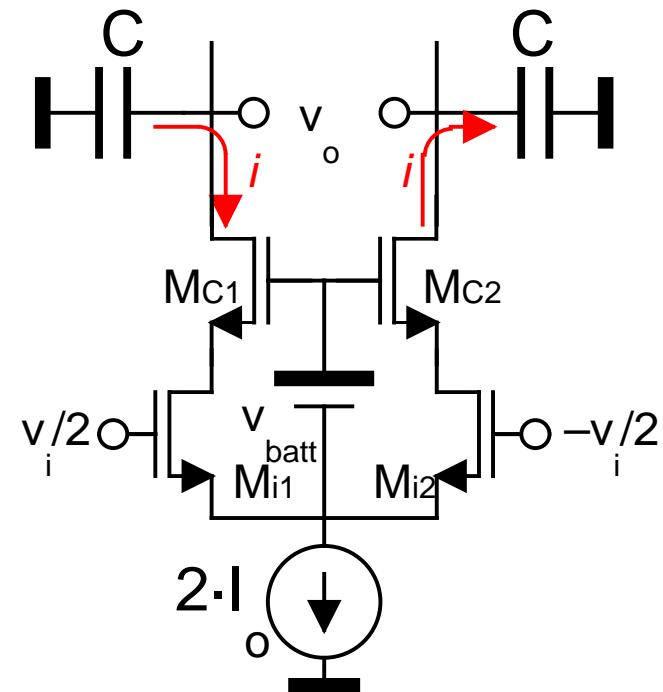
## MOS in linear region – CMOS Open loop configurations

- Transistor  $M_{C1\&2}$  force the  $M_{i1\&2}$  to operate in linear region
- The relatively low impedance at node X1 and X2 makes a certain signal at these nodes

$$r_{oX1} = 1/g_m_{MC1}$$

$$v_{sX1} = v_i \cdot g_m_{Mi1} / g_m_{MC1}$$

- This movements modulates  $V_{DSMi1\&2}$
- This reduces the linear range



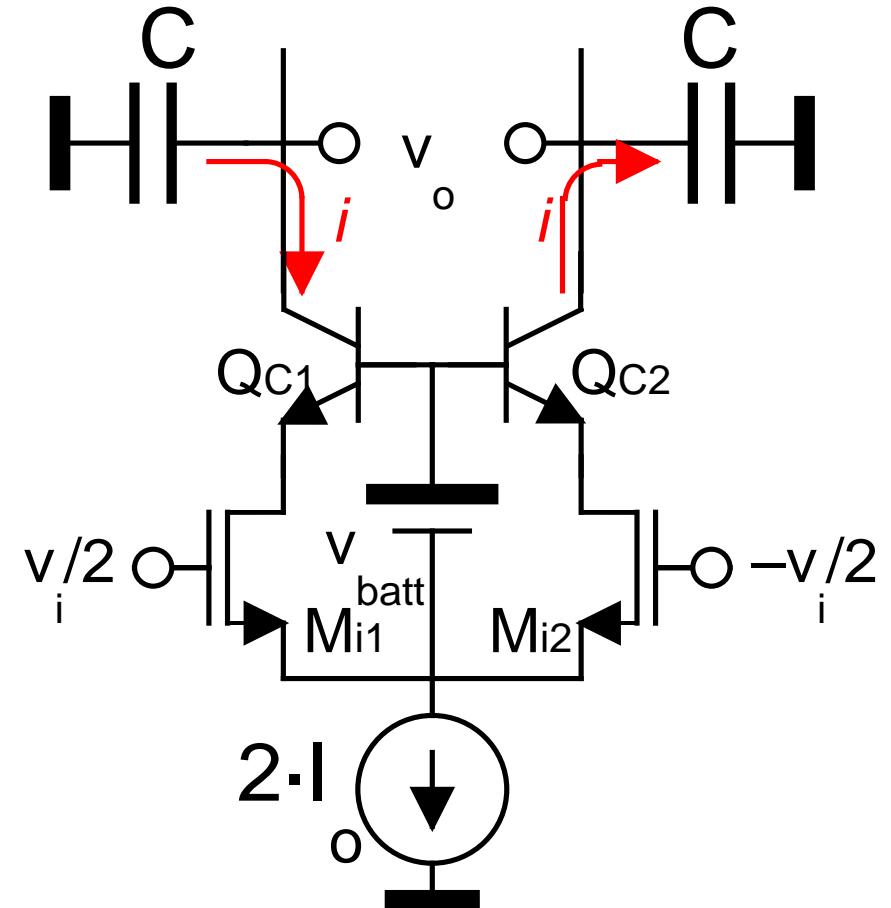
$$G_m = \mu \cdot C_{ox} \cdot \left( \frac{W}{L} \right) \cdot V_{DS}$$



# Gm-C Filter Design

MOS in linear region – BiCMOS Open loop configurations [Alini, JSSC 1992]

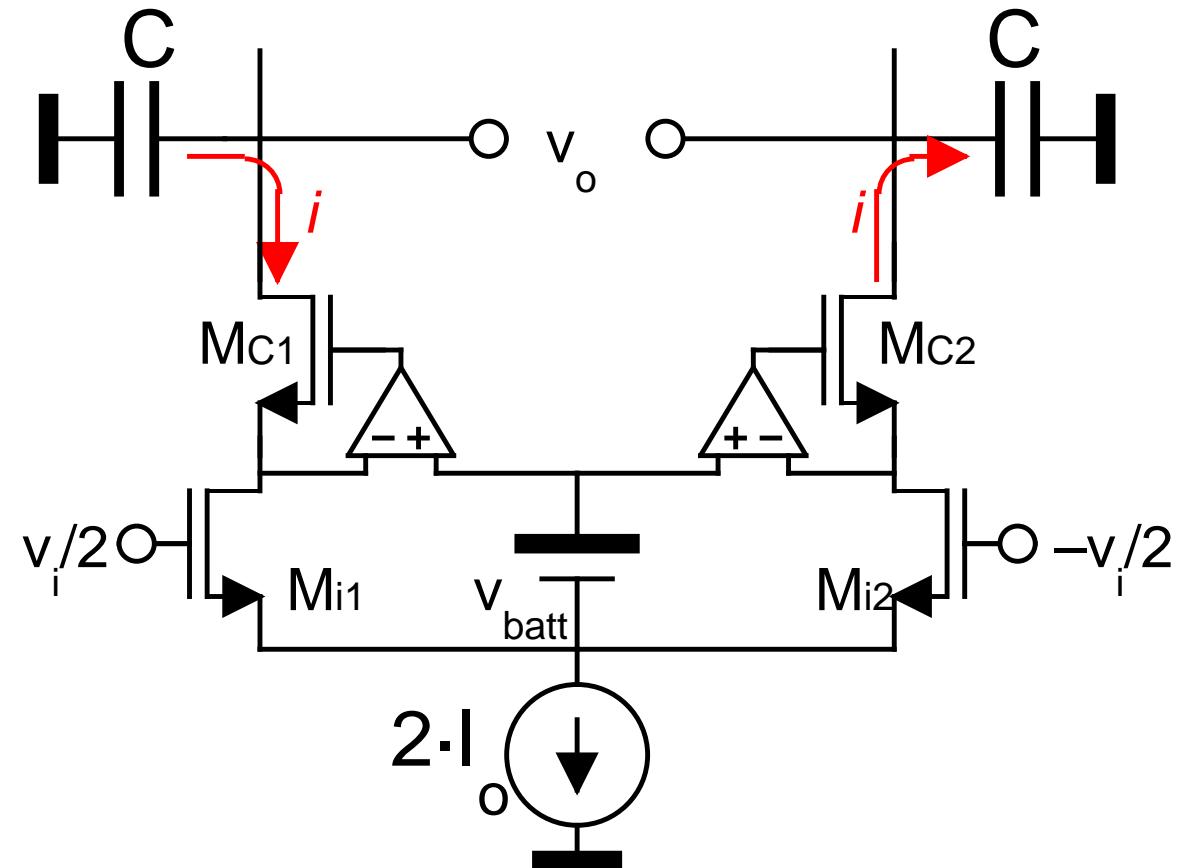
- The lower impedance at the  $Q_{C1\&2}$  emitter
  - reduces the swing of  $V_{DSMi1\&2}$
  - linearizes the structure
- A BiCMOS technology is needed



# Gm-C Filter Design

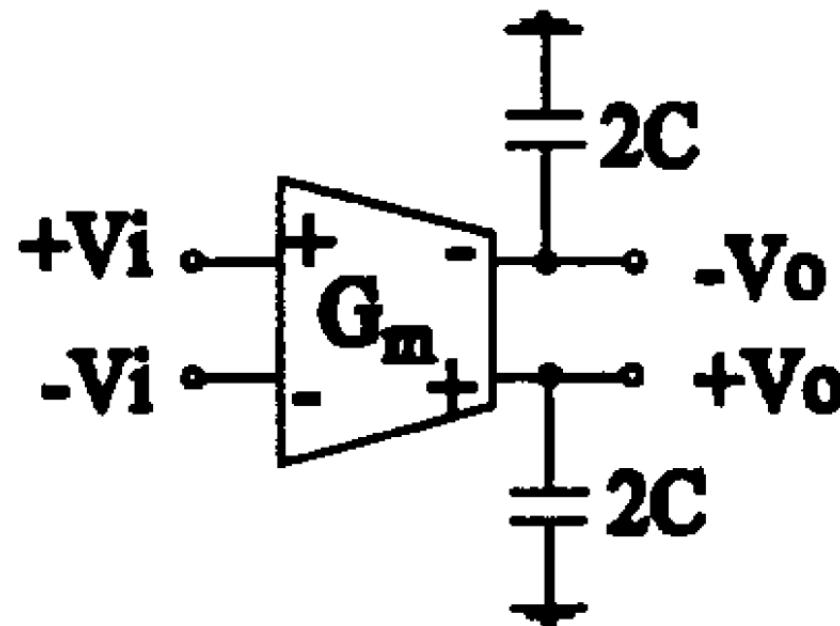
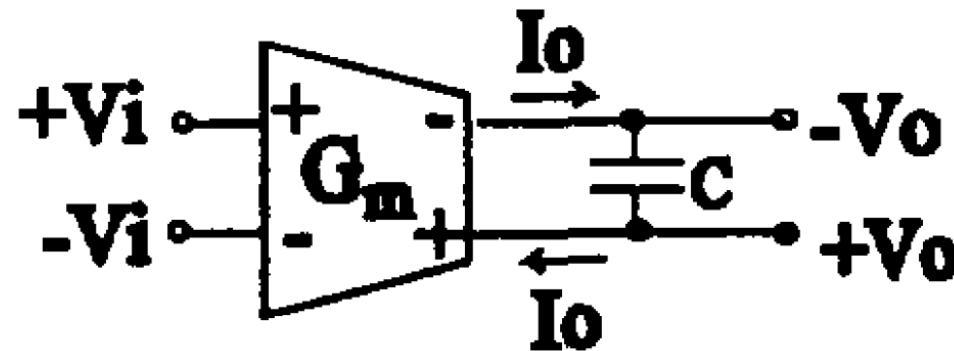
## MOS in linear region – Closed loop configurations

- In CMOS technology a closed loop structure is used to fix  $V_{DS}$



# Gm-C Filter Design

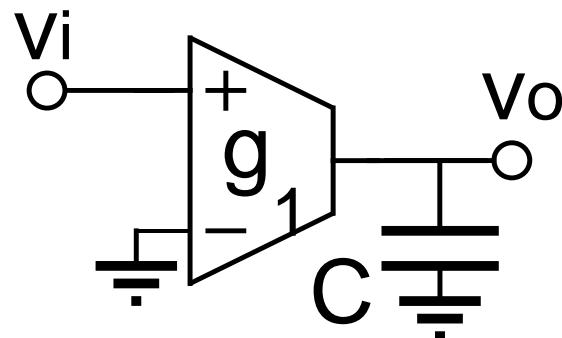
Differential vs. Single-ended Capacitive load



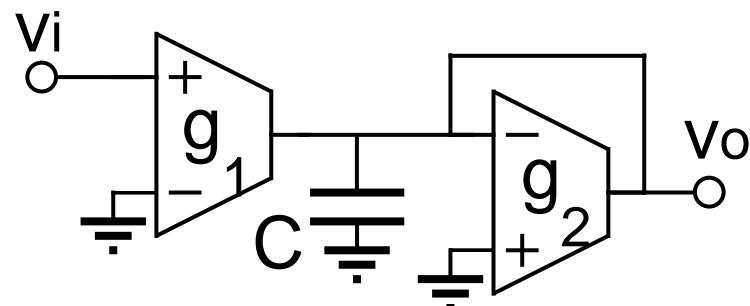
# Gm-C Filters

## Filter architecture

- Basic integrator (for ladder structures)



- 1<sup>st</sup> order cell - I



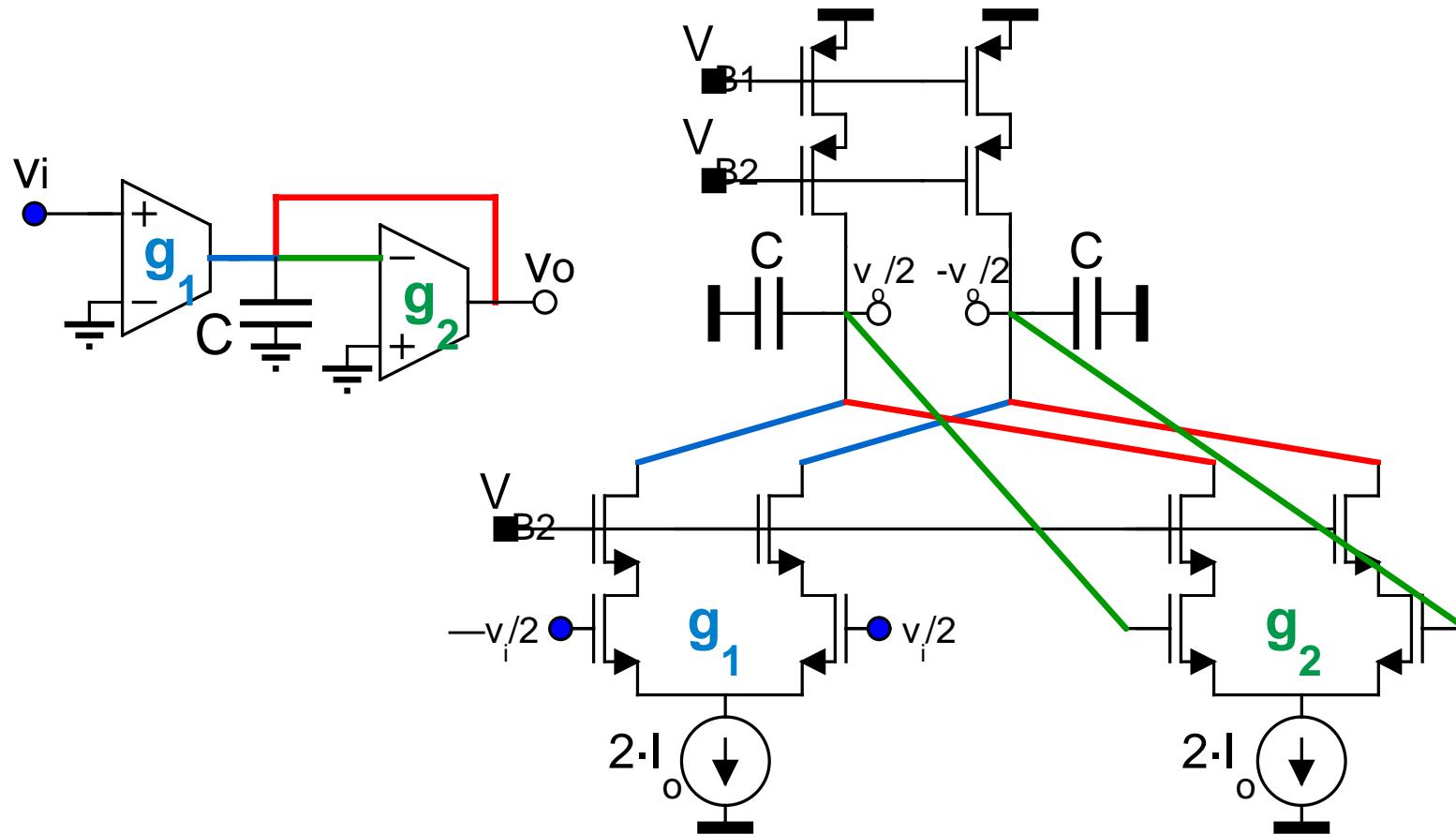
$$H(s) = G_1 \cdot \frac{1}{G_2 + s \cdot C}$$



# Gm-C Filters

## Filter architecture – Transistor Level

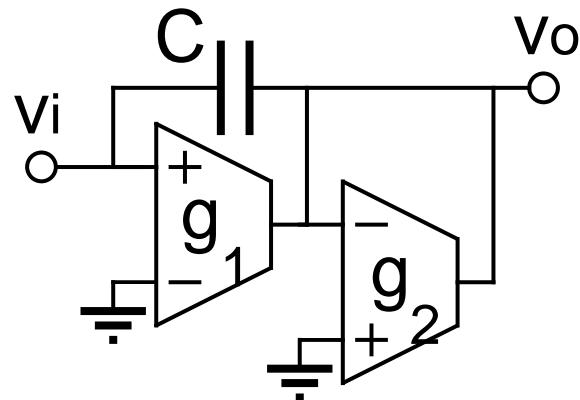
- The top current source is shared



# Gm-C Filters

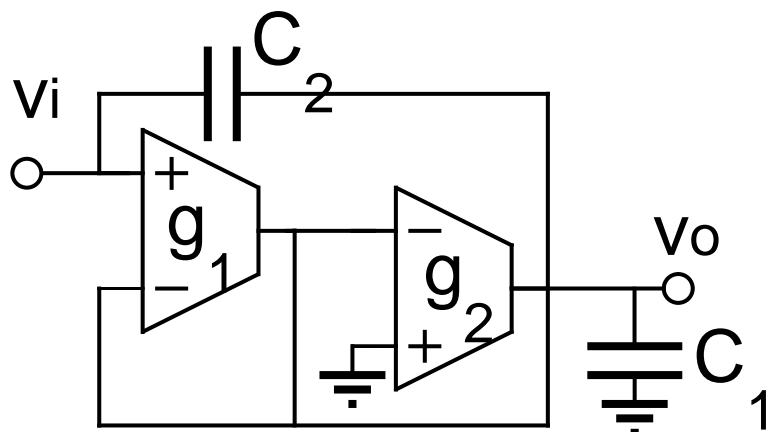
## Filter architecture

- 1<sup>st</sup> order cell - II



$$H(s) = \frac{G_1 + s \cdot C}{G_2 + s \cdot C}$$

- 1<sup>st</sup> order cell - III

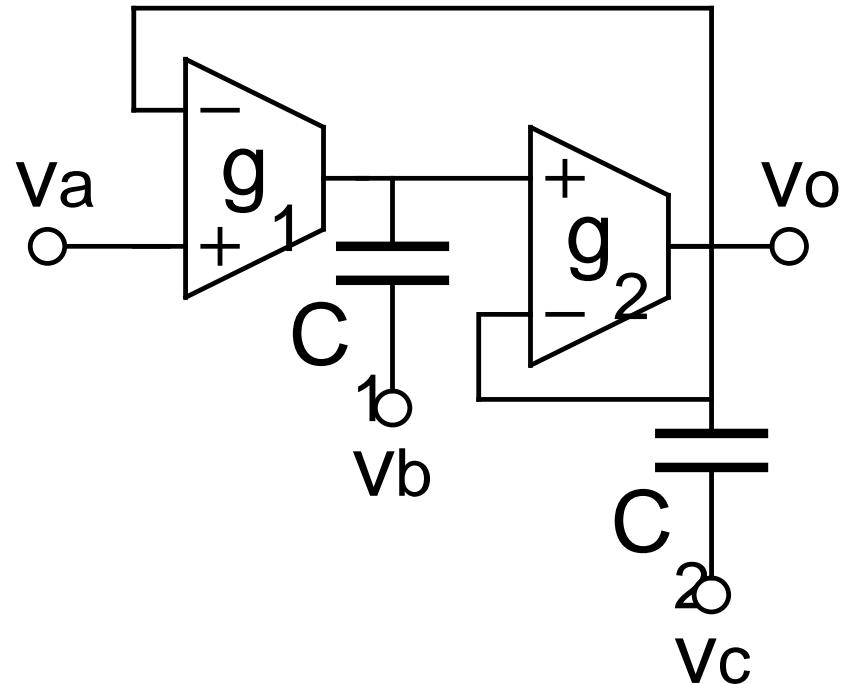


$$H(s) = \frac{G_1 + s \cdot C_2}{(G_1 + G_2) + s \cdot (C_1 + C_2)}$$



# Gm-C Filters

## Filter architecture



$$v_o(s) = \frac{s^2 \cdot C_1 \cdot C_2 \cdot v_c + s \cdot C_1 \cdot g_2 \cdot v_b + g_1 \cdot g_2 \cdot v_a}{s^2 \cdot C_1 \cdot C_2 + s \cdot C_1 \cdot g_2 + g_1 \cdot g_2}$$

$$\omega_o = \sqrt{\frac{g_1 \cdot g_2}{C_1 \cdot C_2}}$$

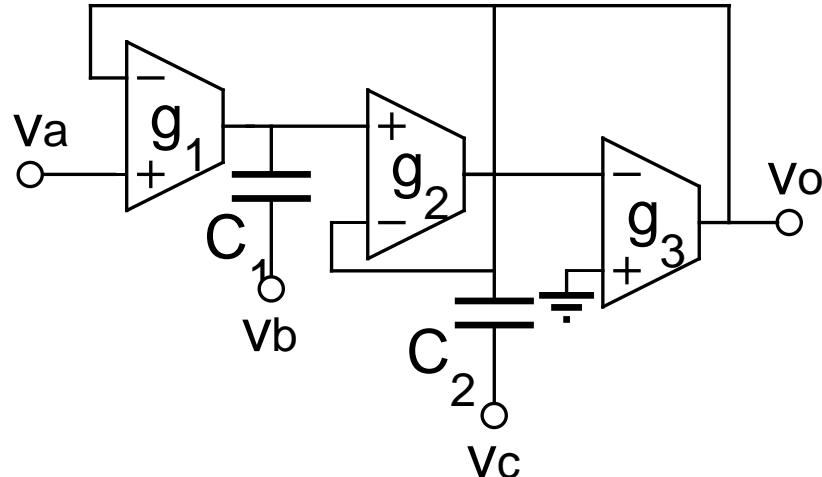
$$Q = \sqrt{\frac{g_1}{g_2} \cdot \frac{C_2}{C_1}}$$

- Programmable frequency response ( $v_a$  lowpass,  $v_b$ , bandpass,  $v_c$  highpass)
- Not practical for fully-differential



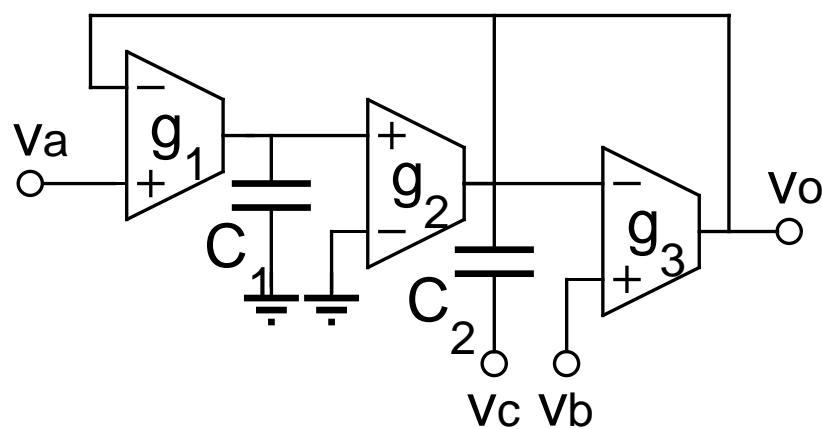
# Gm-C Filters

## Filter architecture



$$\omega_0 = \sqrt{\frac{g_1 \cdot g_2}{C_1 \cdot C_2}}$$

$$Q = \sqrt{\frac{C_2}{C_1}} \cdot \sqrt{\frac{g_1 \cdot g_2}{g_3}}$$



$$v_o(s) = \frac{s^2 \cdot C_1 \cdot C_2 \cdot v_c + s \cdot C_1 \cdot g_3 \cdot v_b + g_1 \cdot g_2 \cdot v_a}{s^2 \cdot C_1 \cdot C_2 + s \cdot C_1 \cdot g_3 + g_1 \cdot g_2}$$

$$\omega_0 = \sqrt{\frac{g_1 \cdot g_2}{C_1 \cdot C_2}}$$

$$Q = \sqrt{\frac{C_2}{C_1}} \cdot \sqrt{\frac{g_1 \cdot g_2}{g_3}}$$



# Gm-C Filters

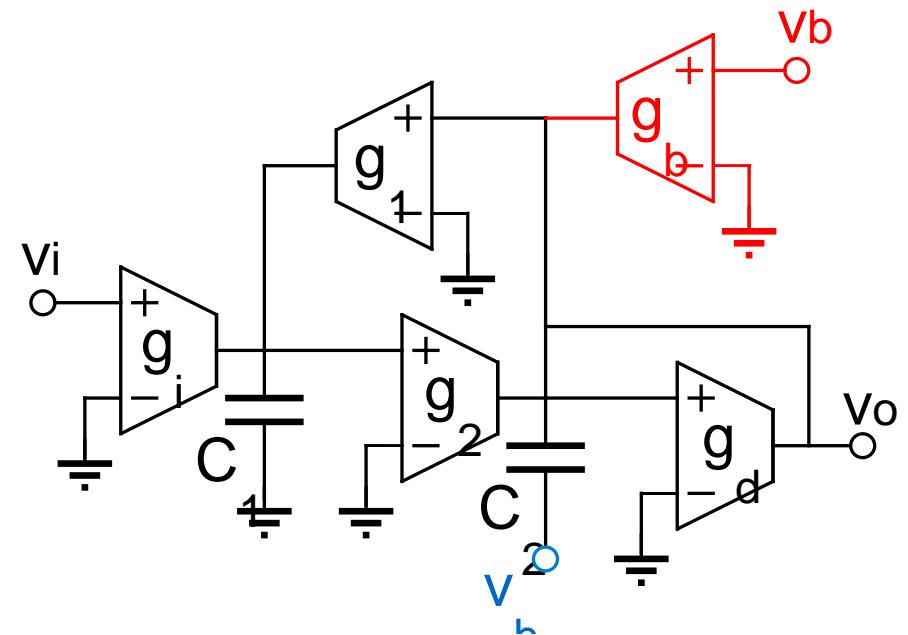
## Filter architecture

- Most popular configuration

$$v_o(s) = \frac{s^2 \cdot C_1 \cdot C_2 \cdot v_h + s \cdot C_1 \cdot g_b \cdot v_b + g_i \cdot g_2 \cdot v_i}{s^2 \cdot C_1 \cdot C_2 + s \cdot C_1 \cdot g_d + g_1 \cdot g_2}$$

$$\omega_o = \sqrt{\frac{g_1 \cdot g_2}{C_1 \cdot C_2}}$$

$$Q = \sqrt{\frac{C_2}{C_1}} \cdot \sqrt{\frac{g_1 \cdot g_2}{g_d}}$$



$$\frac{v_o}{v_i}(0) = \frac{g_i}{g_1} \quad \text{Lowpass DC-Gain}$$

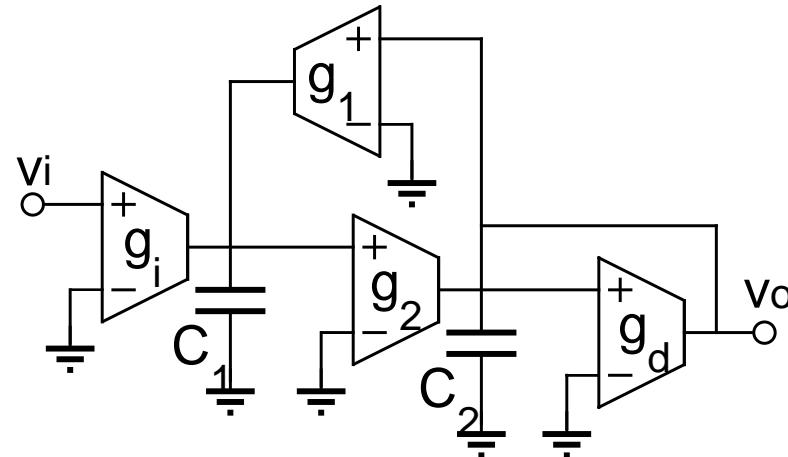
- $g_i$ : input transconductor → Gain control
- $g_1$  &  $g_2$  : loop transconductor →  $\omega_o$ -control
- $g_d$  : dumping transconductor → Q-control



# Gm-C Filters

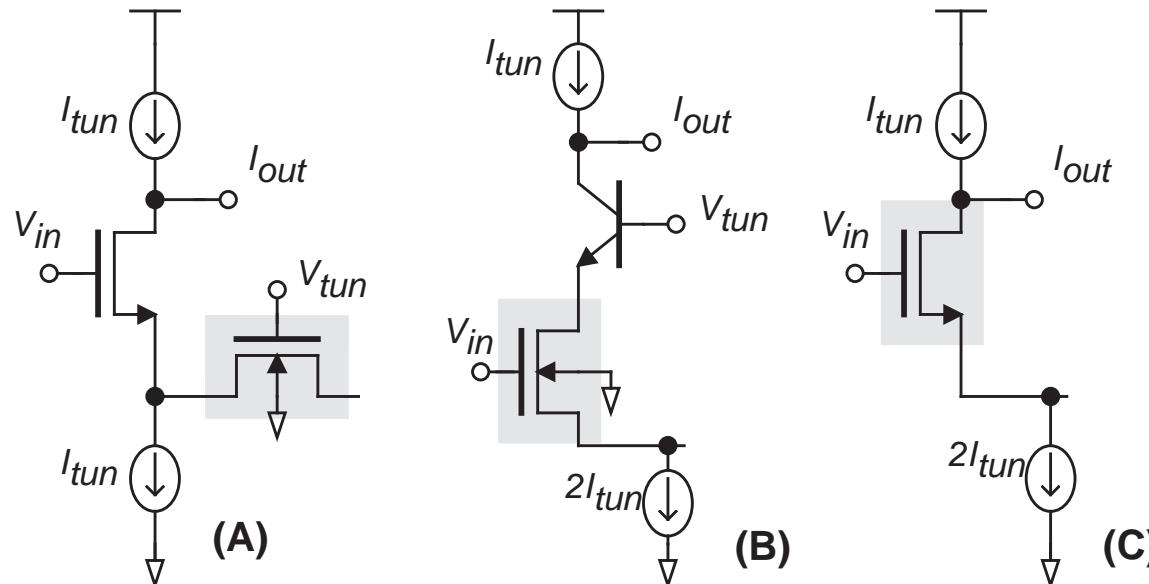
## Main design guidelines

- High-linearity input transconductor
- Same amount of parasitic capacitance for each node (<20%)
- Highly Matched structures for the G1 & G2
- C1 & C2 may be MOS capacitor to track Gm dependence on Cox



# Possible Transconductor Topologies

- Very simple topology to process large-bandwidth signals

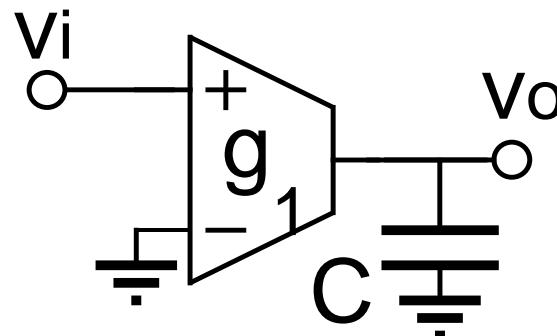


- At moderate tuning, all the circuit have similar DR
- B has the largest swing (for a given THD) or vice versa but loses its advantage in a pure CMOS implementation
- C is the fastest and smallest but has the smallest swing and Max DC-gain variation



# CMOS Gm-C filters

## Frequency Tuning



- Capacitors and  $g_m$  variations (due to temperature and technology) can be compensated by changing the bias current.
- The same can be done to program the filter bandwidth.
- Tuning the transconductor in this way moves the bias point away from its optimum value.
- This degrades the DR and changes the gain by a factor closely related to the overall tuning



# Example

## MOS saturated transconductor with continuous current tuning

- E.g. simulated parameter spread when adjusting the current to keep gm/C constant versus Tech. + Temp. (worst case swing 500mVpp)

Parameter	0.35µm Technology	0.25µm Technology
Current Tuning	5.5 ÷ 1	7 ÷ 1
Overdrive Variation	3.5 ÷ 1	4 ÷ 1
DCgain spread	1.5 ÷ 1	1.8 ÷ 1
Min DCgain	75	50
Min. Power supply	1.9 V	2.0 V

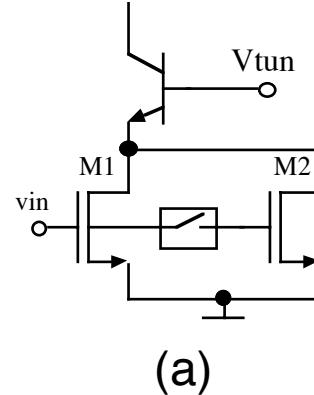
- E.g. in a 0.25µm CMOS technology, a biquad with Q=2 has a  $\Delta Q \approx 10\%$  due to gain variation
- Programming correspondingly increase the spreads
- The same occurs with further technology scaling, making this solution unusable.
- To preserve performance with scaling, reduce continuous tuning



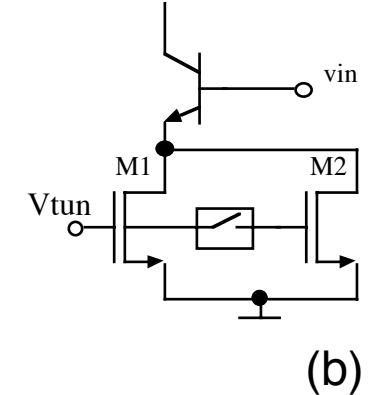
# Low Voltage Transconductors

## Extended Tuning Range: Digital tuning

- Switched MOS technique
- ⌚ (a) The switch is on the signal path !!!!

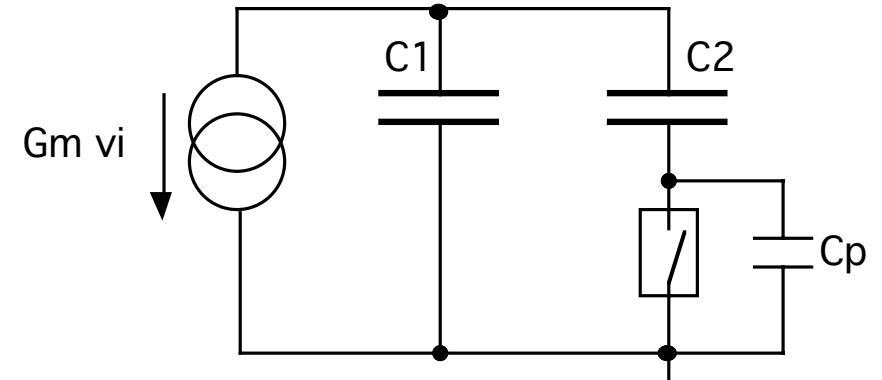


(a)



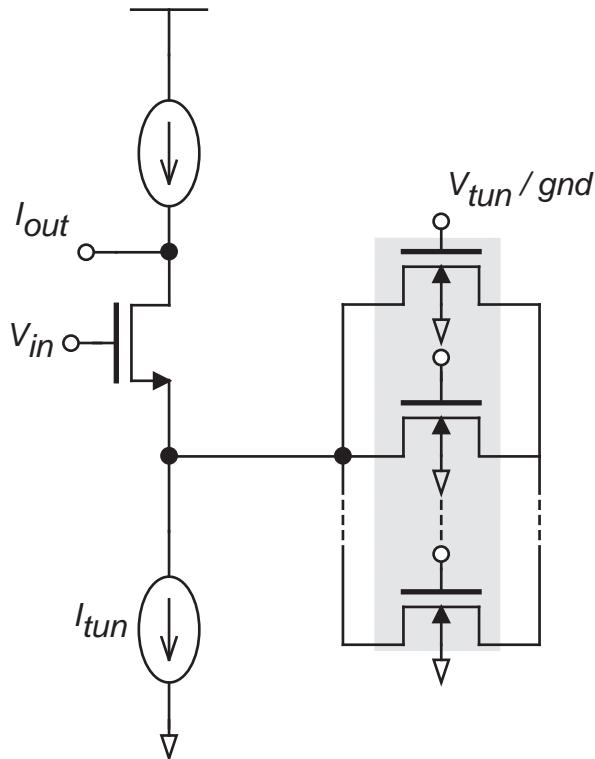
(b)

- Switched Capacitor technique
- ⌚ The parasitic cap. Cp bypasses the switch
- ⌚ The  $r_{on}$  of the switch originates a phase lag



# Design example: disk drive application

- 3.3V 0.35  $\mu\text{m}$  CMOS filter for 300 Mbit/sec PRML HDD

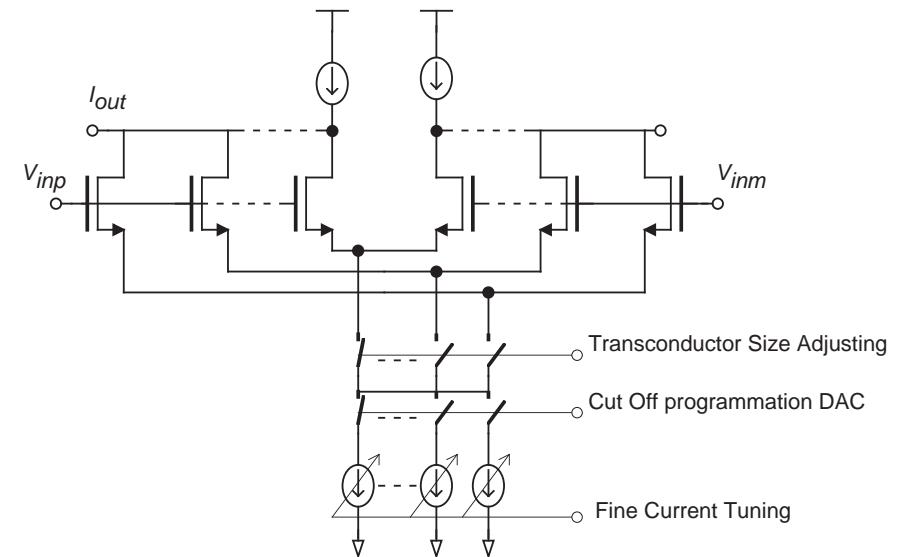


- 5:1 frequency range broken in different regions each corresponding to a different size of the transconductor.
- Discrete tuning used **only** for cut-off programmability.
- The maximum pole frequency is over 160 MHz.



# Saturated MOS transconductor with discrete tuning

- Saturated MOS transconductor is fastest, simplest and most suitable for low-voltage but unusable with continuous current tuning
- => Use discrete tuning also to compensate Tech. and Temp. spreads
- Example: spread compensation + (2÷1) programming (Max swing 500mVpp) with a 4 pairs structure in a 0.25 $\mu$ m CMOS technology



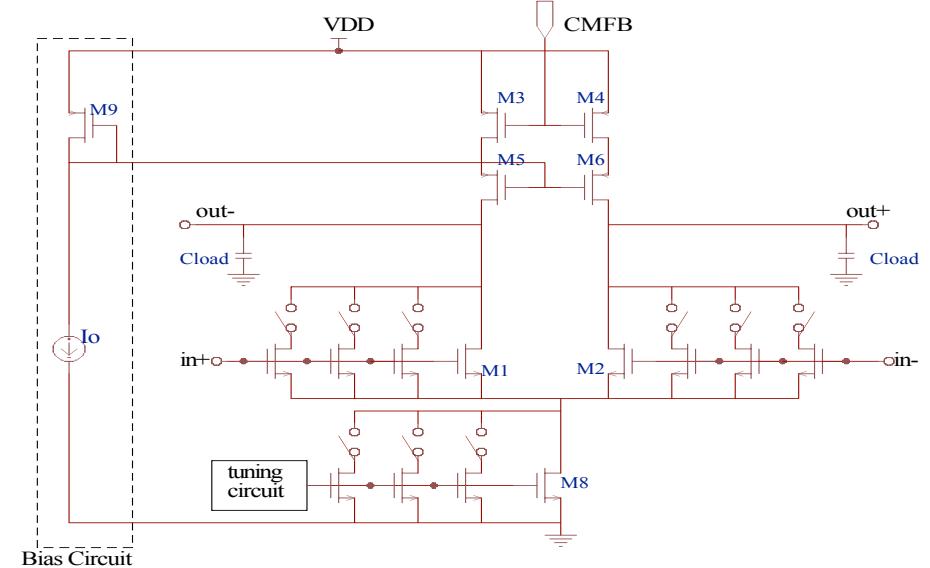
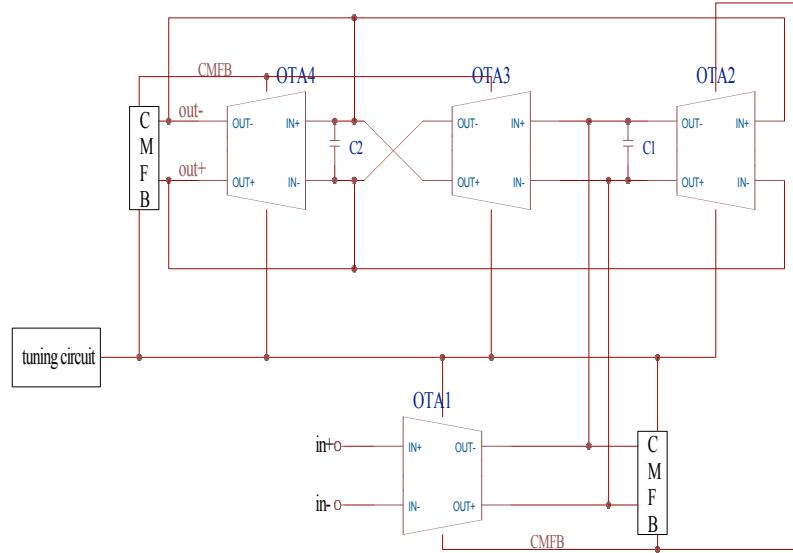
Parameter	Continuous tuning	Discrete (digital) tuning
Current Tuning	7 ÷ 1	2.5 ÷ 1
Overdrive Variation	4 ÷ 1	1.5 ÷ 1
DCgain spread	1.8 ÷ 1	1.3 ÷ 1
Min DCgain	50	70
Min. Power supply	2.0 V	1.6 V



# Tuning strategy

- Capacitance are tuned adjusting the reference current during trimming
- Programming is performed changing the reference current
- Spreads are adjusted in a coarse discrete way changing the transconductor size and in a fine way changing the reference current
  - Discrete gm tuning can be implemented using an A/D converter and some DSP
  - The controlling signal value is stored in a register and is constant between calibration cycles.
  - Fine current calibration is active during normal operation.





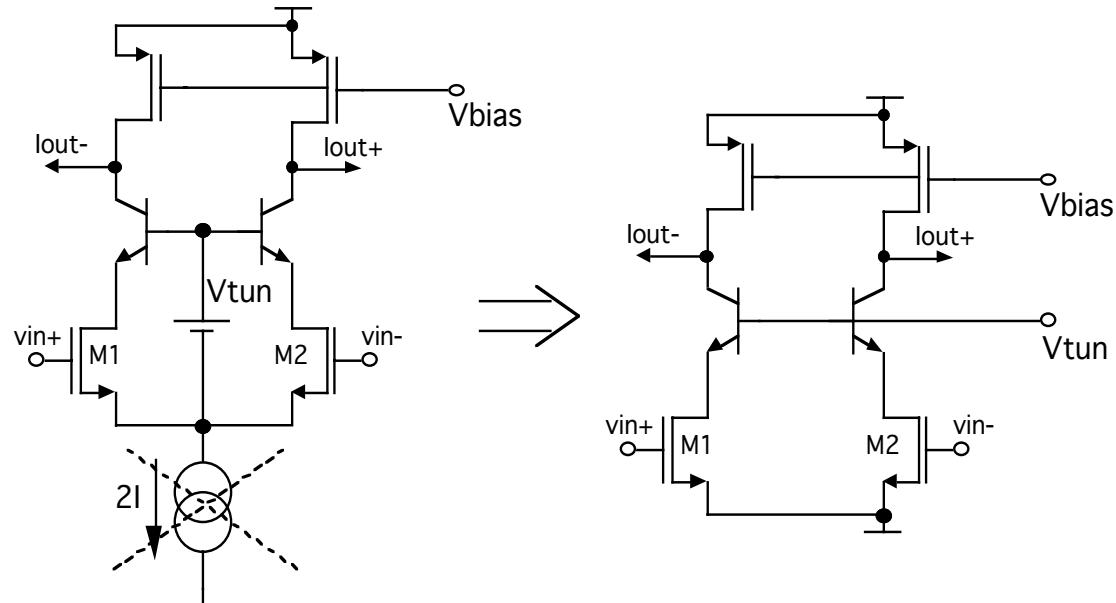
# Gm-C Filters

## Low-voltage solutions

- Eliminate the voltage drop of the current source by using pseudo-differential structures
  - (two single-ended structures in parallel and operated with complementary signals)

☺ Avoid the voltage drop of current source

- ☺ 1 Input CM rejection
- ☺ 2 Linearity at low power
- ☺ 3 Output CM feedback
- ☺ 4 Dc-gain



### • Solutions

- ☺ 1 Feedforward technique
- ☺ 2 Proper current summing
- ☺ 3+4 Use of dumped integrator  
(Precise gain concept)



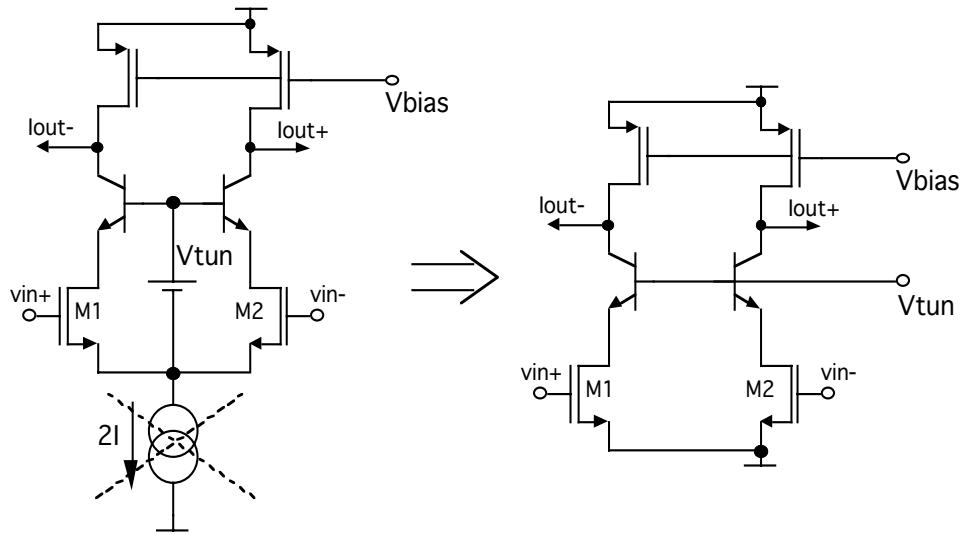
# Gm-C Filters

## Pseudo-Differential Low-Voltage Transconductors [Rezzi-TCAS95]

- Fully-differential structure
  - ☺ A single  $V_{tun}$  for each transconductor
  - ☺ Minimum CM voltage  $V_{CMmin} \approx 1.5V$

$$V_{CMmin} = V_{dsmax} + V_{cesat} + V_{gen} + V_{signal}$$

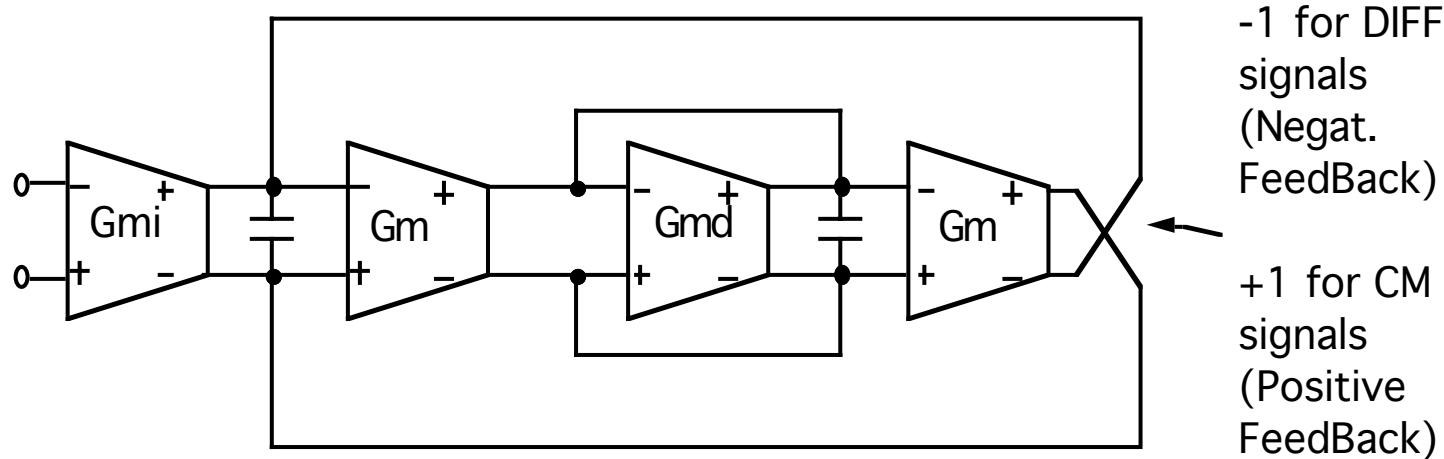
- Pseudo-Differential
  - ☺ Intrinsic rejection of the CM input signals
  - Pseudo-Differential
    - ☺ Easy to bias and easy to tune ( $V_{tun}$  can be shared among different transconductors)
    - ☺ Minimum CM voltage  $V_{CMmin} = V_{dsmax} + V_{cesat} + V_{signal} \approx 1V$
    - ☺ **No rejection of CM input signals** (CMRR=1) (instability in feedback structures)



# Pseudo-Differential Low-Voltage Transconductors

## ***Effect of non-zero input CM signals***

- A cancellation of the common-mode signal is mandatory to avoid positive feedback
    - Example of CM positive feedback: Differential biquadratic cell

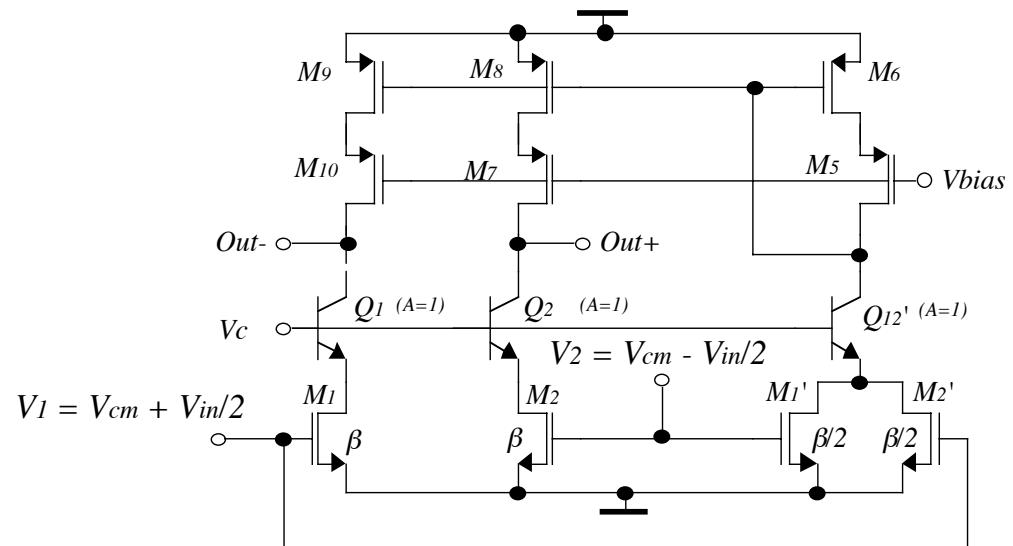
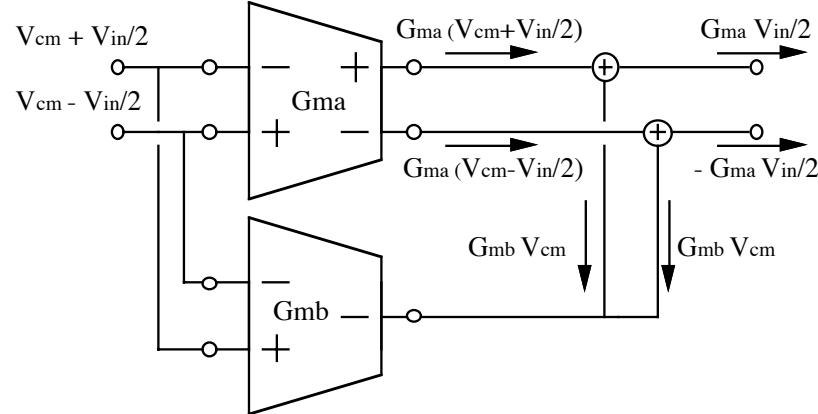


- The feedback is negative for the differential signal while it is positive for CM
    - Fully differential  $\Rightarrow G_{loop} \ll 1 \Rightarrow$  The system is stable
    - Pseudo-differential  $\Rightarrow G_{loop} > 1 \Rightarrow$  The system is not stable

# Pseudo-Differential Low-Voltage Transconductors

## ☺ 1 - Input CM signals Feed-forward cancellation

- The input CM signal is sensed and subtracted at the output node

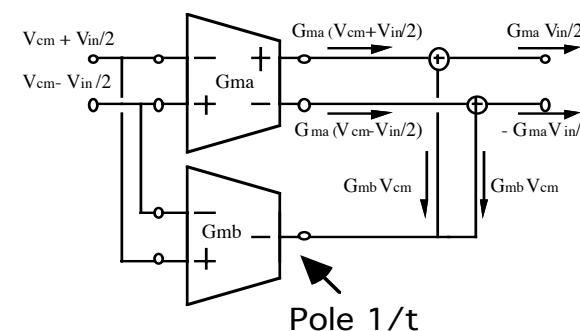
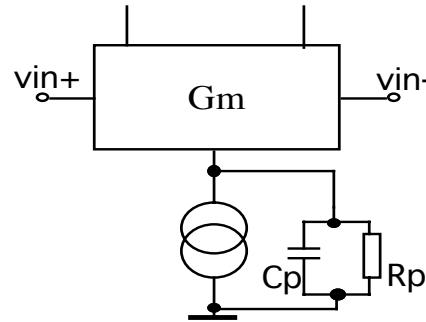


- Auto-biasing circuit



# Pseudo-Differential Low-Voltage Transconductors

## *Common Mode Rejection Ratio Performance*



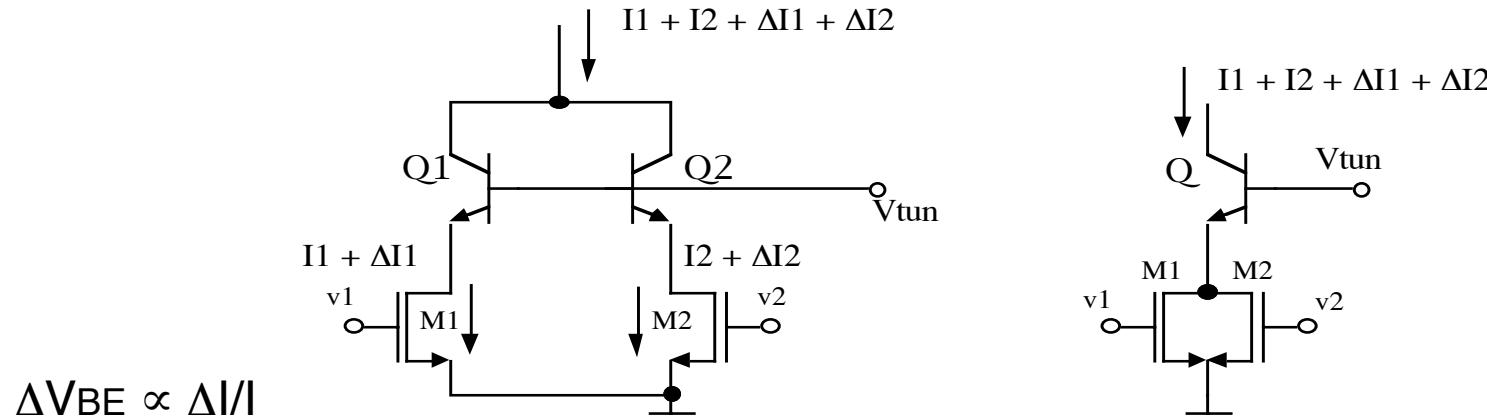
- Low frequency  $\approx G_m \cdot R_p \gg 1$  (offset and matching)
- High frequency  $\approx \frac{1 + s C_p / G_m}{s C_p / G_m} \approx \frac{1 + s\tau}{s\tau}$
- For a load capacitor
- $C_L \Rightarrow \omega = G_m / C_L \approx \frac{C_L}{C_p} \approx \frac{C_L}{G_m \tau}$
- In the PD structures the HF CMRR depends on the speed  $\tau$  of the current mirror
- If  $\tau$  is sufficiently small, PD solution may be better than the fully differential ones
- At low frequency, the performances of the fully differential structures are generally better



# Pseudo-Differential Low-Voltage Transconductors

## ☺ 2 - Linearity Performances

- The transconductor THD depends mainly on the V<sub>DS</sub> variation due to the V<sub>BE</sub> modulation.



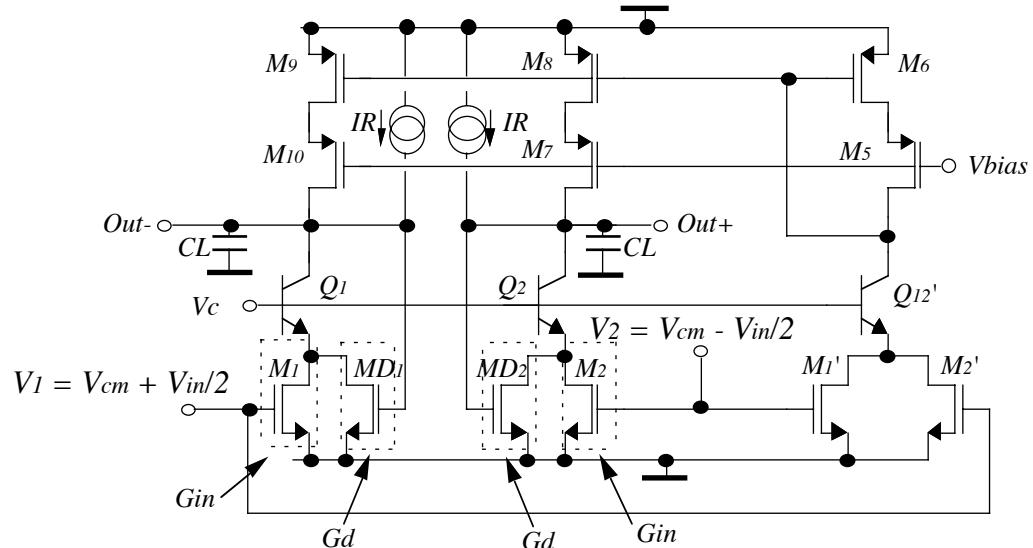
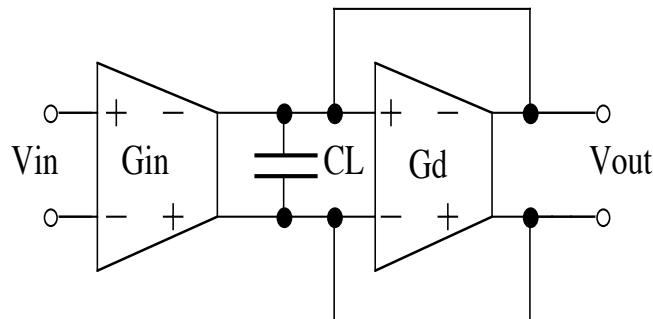
- % Modulation of Q1 =  $\Delta I_1/I_1$
- % Modulation of Q2 =  $\Delta I_2/I_2$
- If  $\Delta I_1$  and  $\Delta I_2$  are not in phase, the % modulation of Q is lower than each % of Q1 and Q2
- The scheme 2 shows a higher linearity at the same current level
  - (the same linearity at lower current level)



# Pseudo-Differential Low-Voltage Transconductors

## ☺ 3+4 - Dumped integrator

- A dumped integrator is obtained just adding two devices (MD1 and MD2)

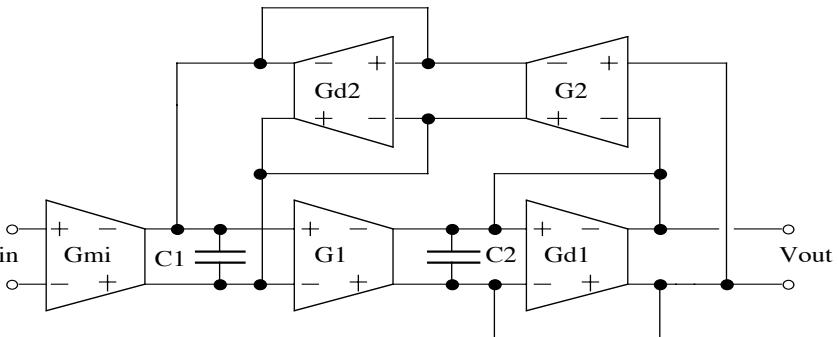
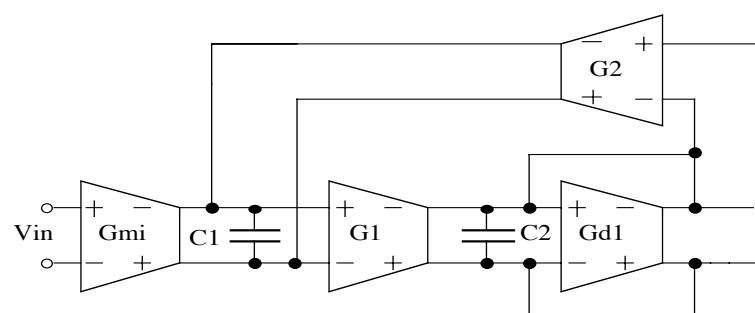


- The dumping transconductor set the output common mode voltage (as a CMFB)
- The Biquadratic Cell uses a doubled-dumped structure for setting the CM voltage at both the nodes
- Dumped integrator means operating with finite-gain transconductor

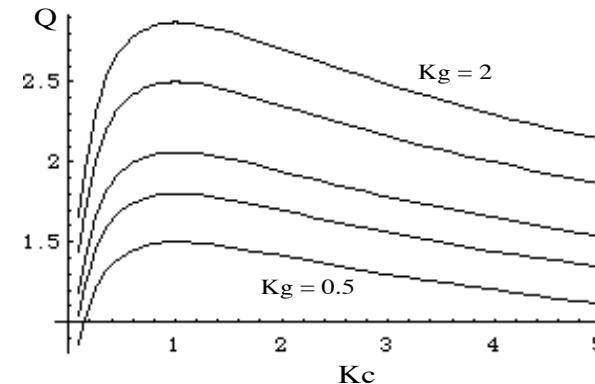
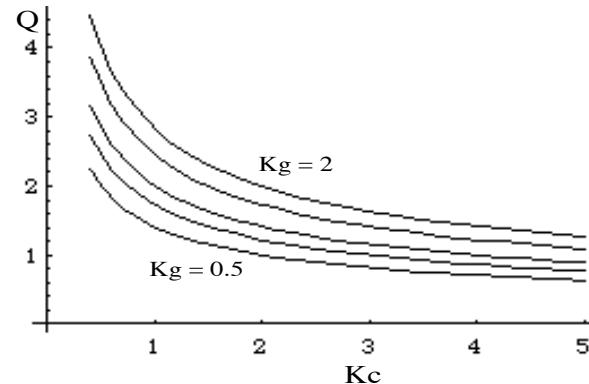


# Pseudo-Differential Low-Voltage Filters

*Performance sensitivity comparison: Q vs. capacitor ratio accuracy*



- Single dumping      Double dumping

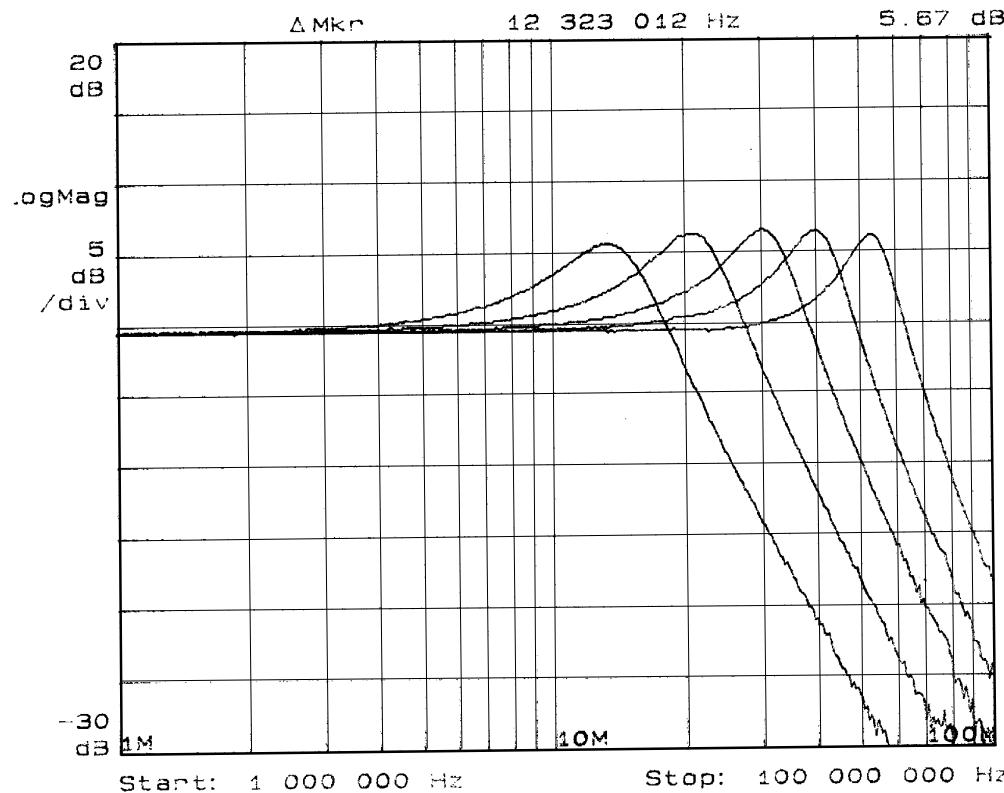


- The double-dumped structures exhibits a low sensitivity of  $Q$  vs.  $k_c \approx 1$



# Pseudo-Differential Low-Voltage Filter performance

## Frequency response with tuning



- A 12-55MHz tuning range is achieved
  - The  $\pm 0.4$ dB peak-deviation is due to the parasitic pole effects (phase error)





*Dipartimento di Ingegneria dell' Innovazione  
Universita' degli Studi di Lecce*

*Andrea Baschirotto*

*andrea.baschirotto@unile.it*

---

## **Analog Filters for Telecommunications**

*Universita' degli Studi di Bologna*

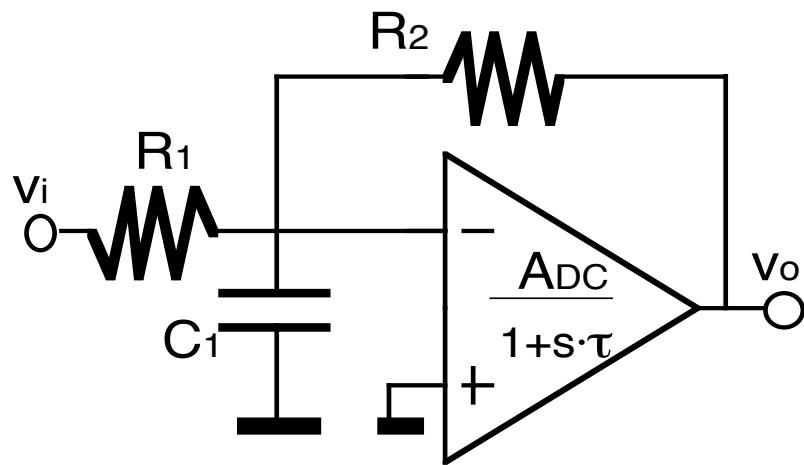
*June, 16<sup>th</sup>-17<sup>th</sup>, 2005*

## **Active-Gm-RC Filters**



# The Active-Gm-RC Filter

## The Low-Pass Cell



- The opamp has a single-pole frequency response (in the frequency range of interest):

$$A(s) = \frac{A_{DC}}{1 + s \cdot \tau} = \frac{\omega_u \cdot \tau}{1 + s \cdot \tau}$$

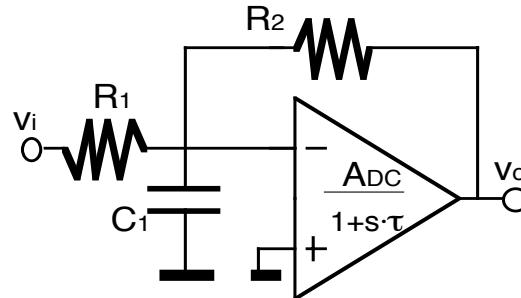
$1/\tau$  is the 1<sup>st</sup>-pole angular frequency  
 $A_{DC}$  is the DC-gain  
The unity gain angular frequency, ( $\omega_u$ ) is

$$\omega_u = \frac{A_{DC}}{\tau}$$

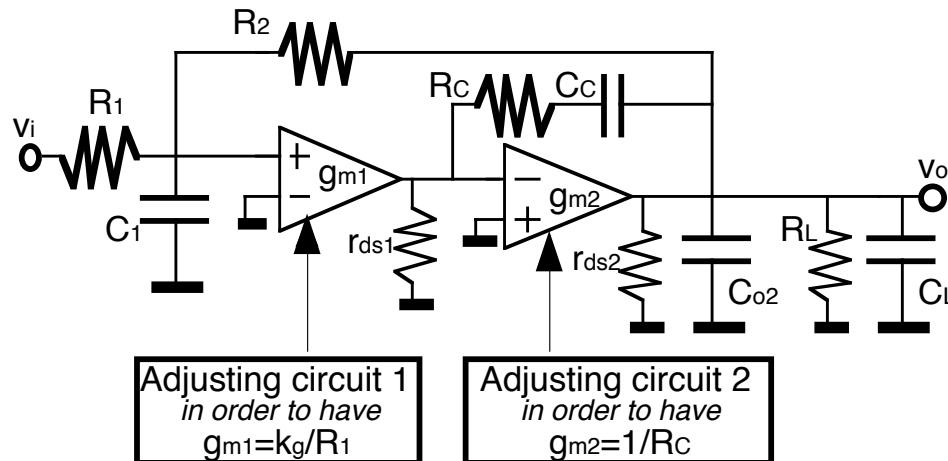


# The Active-Gm-RC Filter

## The Low-Pass Cell



- A possible implementation

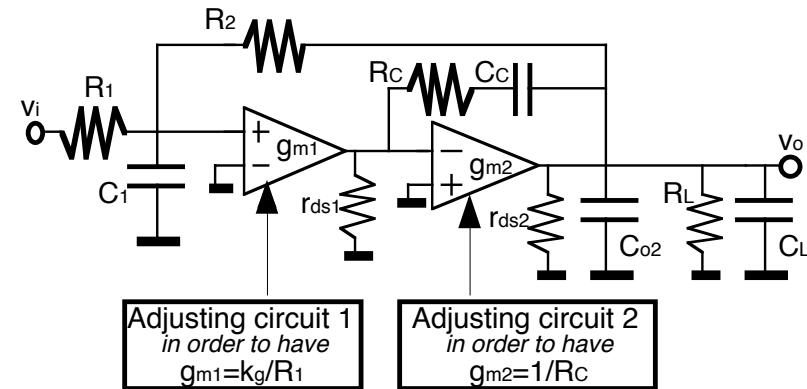
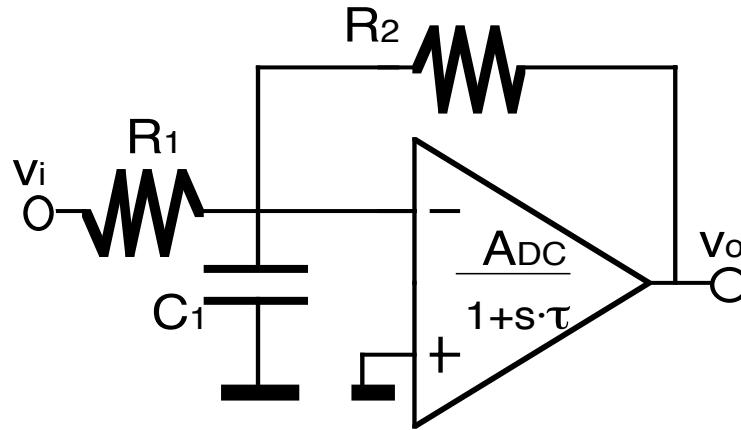


- A two-stage opamp topology
- An input stage (the input transconductance  $g_{m1}$  and the load resistance  $r_{ds1}$ )
- An output stage (the output transconductance  $g_{m2}$  and the load resistance  $r_{ds2}$ )
- A Miller compensation network (resistor  $R_C$  and capacitor  $C_C$ )
- External load ( $R_L$  and  $C_L$ )



# The Active-Gm-RC Filter

## The Low-Pass Cell



$$A_{DC} = g_{m1} \cdot R_{o1} \cdot g_{m2} \cdot R_{o2}$$

- The adjusting circuit sets

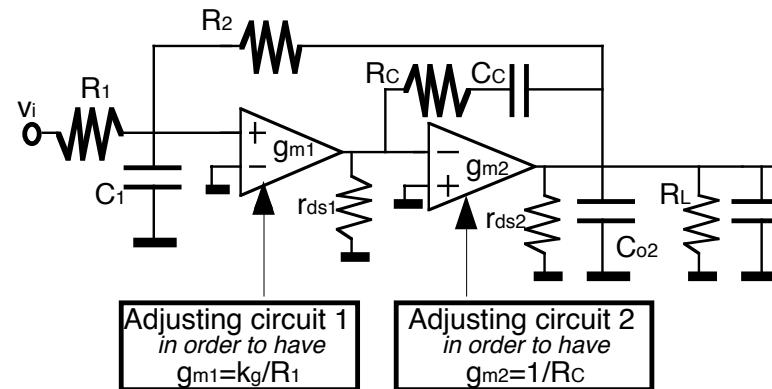
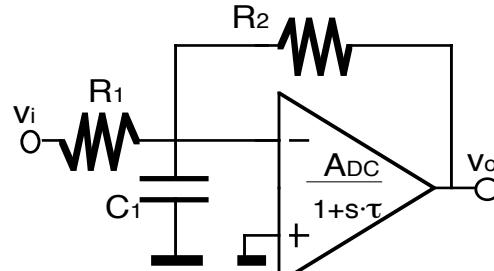
$$g_{m1} = 1/(k_g \cdot R_1)$$

- For the filter frequency response ( $H_{LP}$ ), the adjusting circuit transfers dependence on the opamp frequency response parameters ( $g_{m1}$ , &  $C_C$ ) → dependence on parasitic component values ( $R_1$ ,  $R_2$ , &  $C_1$ )



# The Active-Gm-RC Filter

## The Low-Pass Cell



$$\omega_U = \frac{g_{m1}}{C_C}$$

$$A_{DC} \gg R_1 \cdot C_1 \cdot \omega_U$$

$$A_{DC} \gg R_2 \cdot C_1 \cdot \omega_U$$

$$A_{DC} \gg 1 + \frac{R_2}{R_1}$$

- The low-pass transfer function is:

$$H_{LP}(s) = -\frac{\frac{g_{m1}}{C_1 \cdot R_1 \cdot C_C}}{s^2 + s \cdot \left( \frac{R_1 + R_2}{C_1 \cdot R_1 \cdot R_2} \right) + \frac{g_{m1}}{C_1 \cdot R_2 \cdot C_C}} = -\frac{\frac{1}{k_g \cdot R_1^2 \cdot C_1 \cdot C_C}}{s^2 + s \cdot \left( \frac{R_1 + R_2}{C_1 \cdot R_1 \cdot R_2} \right) + \frac{1}{k_g \cdot R_1 \cdot R_2 \cdot C_1 \cdot C_C}}$$

- The cell parameters are:

$$k_{LP} = \frac{R_2}{R_1}; \quad f_{LP} = \frac{1}{2 \cdot \pi} \cdot \sqrt{\frac{1}{k_g \cdot R_1 \cdot R_2 \cdot C_1 \cdot C_C}}; \quad Q_{LP} = \frac{1}{1 + k_{LP}} \cdot \sqrt{\frac{R_2}{k_g \cdot R_1} \cdot \frac{C_1}{C_C}}$$



# Active-Gm-RC filters

## Numerical design example

- 4<sup>th</sup> order UMTS&WLAN reconfigurable filter

	UMTS		WLAN	
	1 <sup>st</sup> cell	2 <sup>nd</sup> cell	1 <sup>st</sup> cell	2 <sup>nd</sup> cell
$f_{LP}$ [MHz]	3.39	3.02	19.27	17.19
$Q_{LP}$	0.806	0.522	0.806	0.522
$k_{LP}$	1.26	1.26	1.26	1.26
$f_u$ [MHz]	6.17	3.56	35.08	20.27
$f_u/f_{LP}$	1.82	1.18	1.82	1.18

- The opamp unity-gain-frequency ( $f_u$ ) is comparable to the filter cut-off frequency ( $f_{LP}$ )



# Active-Gm-RC filters

## Key advantages (I)

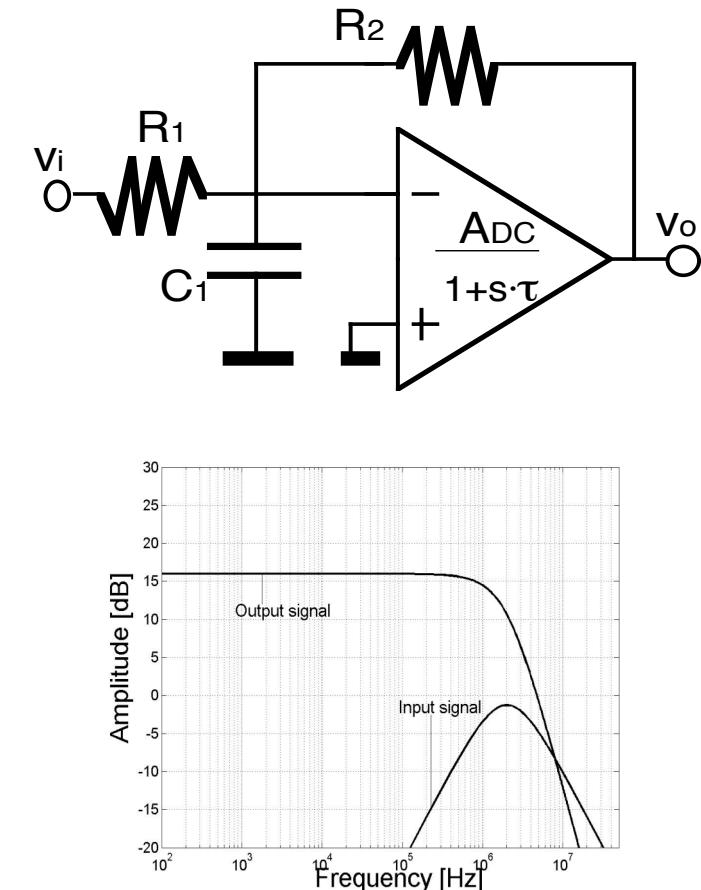
- Low power consumption
  - key target for portable terminals
  - a single opamp is used to synthesize a 2<sup>nd</sup> order transfer function
    - halving the power consumption compared with standard two-opamp Active-RC biquad cells;
- Small-bandwidth opamp requirement
  - the opamp frequency response is used to synthesize the filter frequency response.
  - the opamp is designed to feature a frequency response comparable with the filter pole
  - this reduces the power consumption
    - a standard closed loop structure (Active-RC/MOSFET-C) needs  $f_u/f_{LP} > 50 \div 100$  and requires a larger power consumption



# Active-Gm-RC filters

## Key advantages (II)

- Large linear range
  - In-band Signals
    - The closed loop operation guarantees large linearity
  - Out-of-band Signals
    - The larger signal part is processed by passive linear elements ( $R_1$ ,  $R_2$  and  $C_1$ )
    - The smaller part is processed by the non-linear opamp stages
- In telecom systems the out-of-band linearity is crucial (and in some cases, more important than in-band linearity) due to the higher level out-of-band blockers

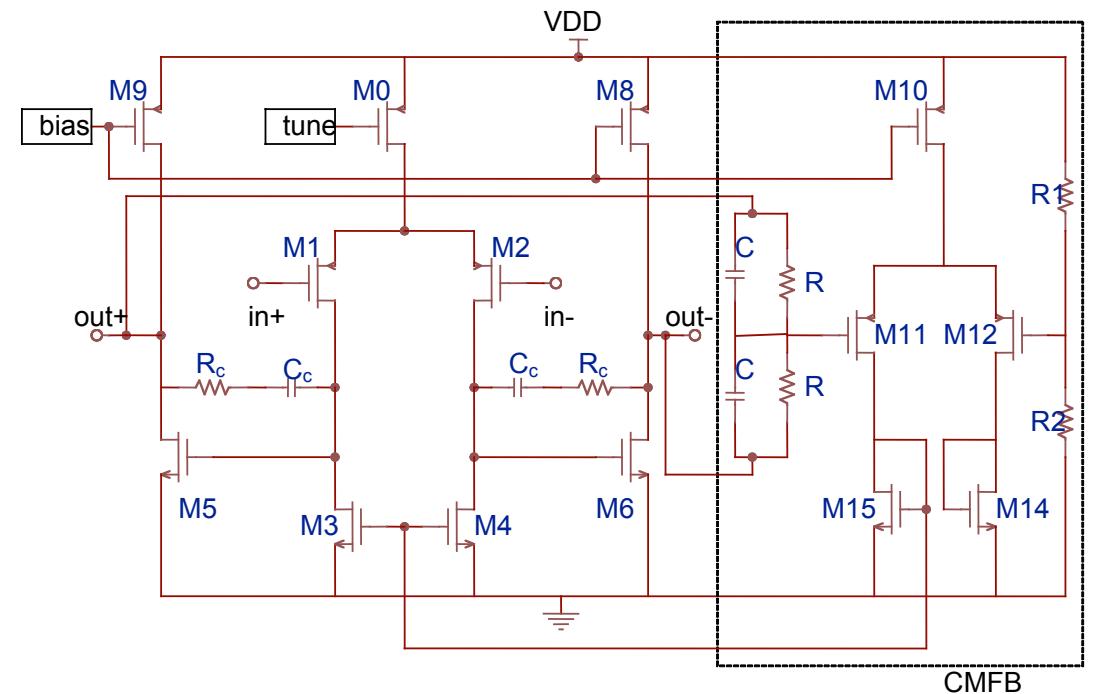
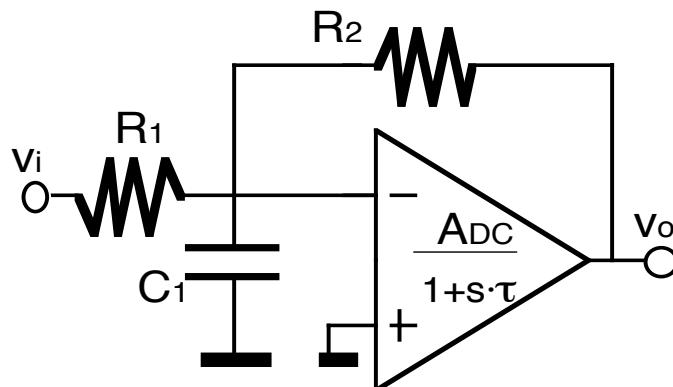


# Active-Gm-RC filters

## Opamp implementation

- Two stage topology

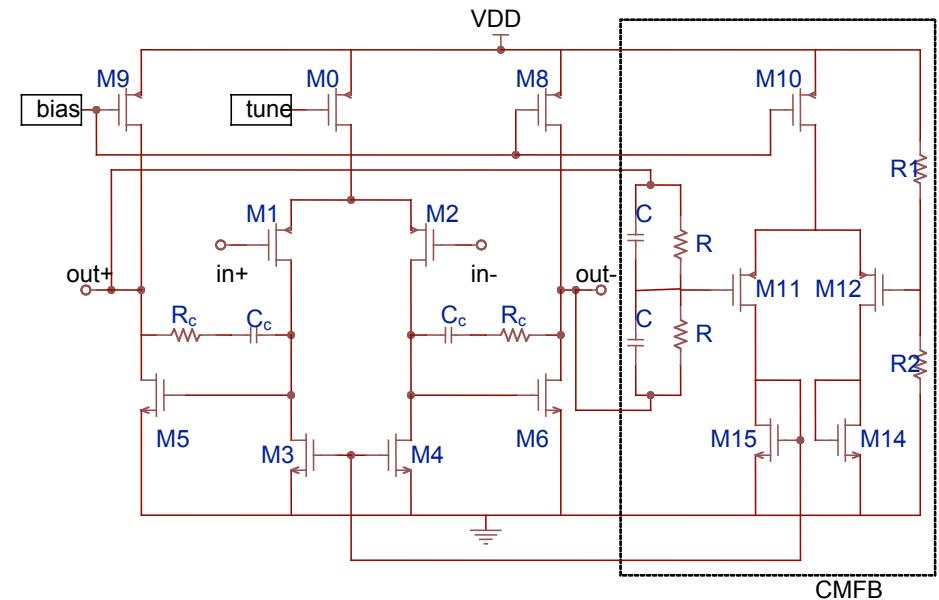
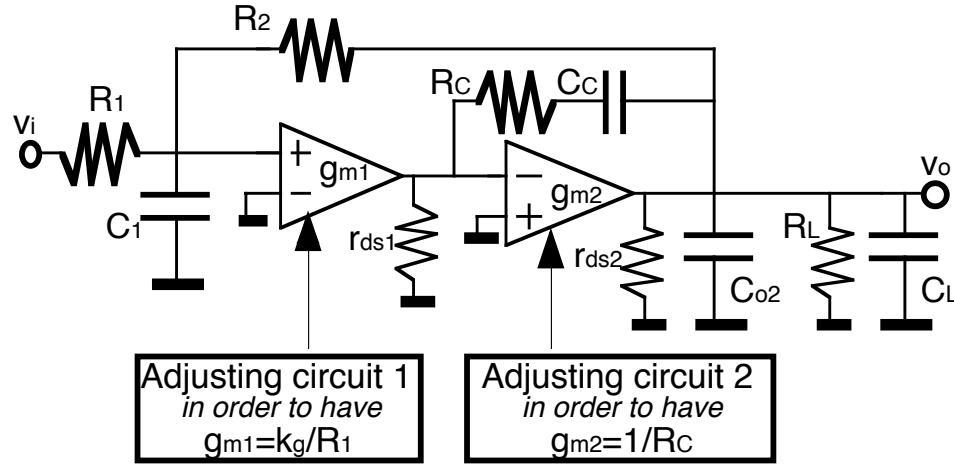
- An input stage made by the transconductance  $g_{m1}$  and the resistance  $R_{o1}$
- A compensation resistance  $R_C$  and capacitance  $C_C$
- An output stage made by the transconductance  $g_{m2}$  and the load resistance  $R_{o2}$
- A common-mode feedback circuit is designed with an additional differential pair



# Active-Gm-RC biquadratic cell

## Second order singularities

- The influence of the op-amp 2<sup>nd</sup> pole on the overall cell structure frequency response



- For the frequency response of the adopted op-amp, the second pole angular frequency is:

$$\omega_{p2} = \frac{g_{m5}}{C_{\text{load}}}$$



# The Active Gm-RC Biquadratic Cell

## The output stage bias circuit

$$\omega_{p2} = \frac{g_{m5}}{C_{load}}$$

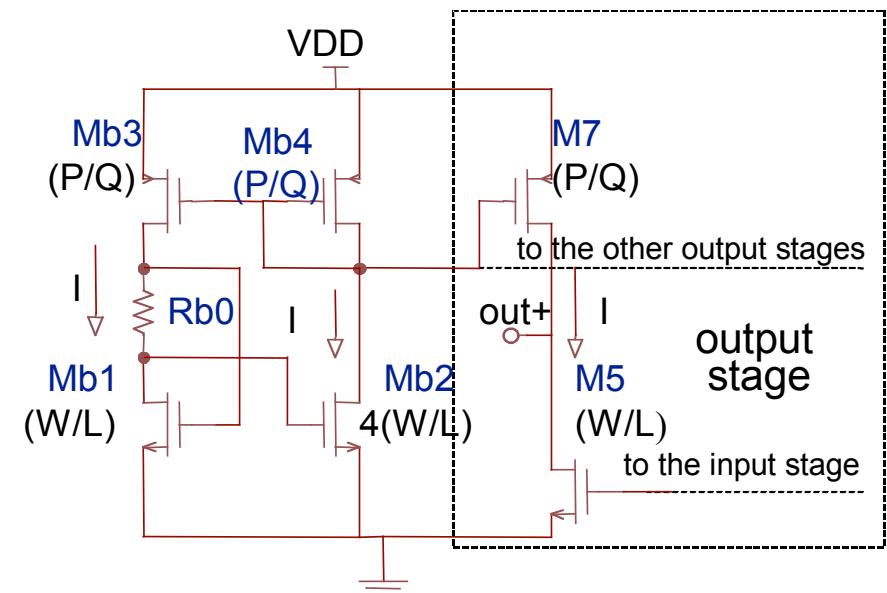
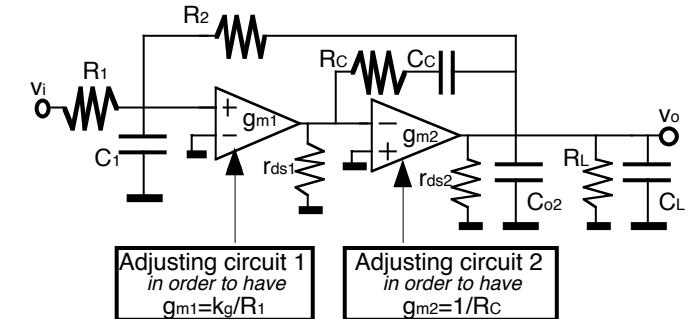
- The resistance  $R_C$  and the capacitance  $C_C$  introduce a zero:

$$\omega_z = \frac{1}{C_C \left( \frac{1}{9m_5} - R_C \right)}$$

- $g_{m5}$  must be equal to  $1/R_C$
  - An output stage bias circuit correlates
- $$g_{m5} = 1/R_C$$
- The op-amp behaves like a single pole circuit

The output stage DC-gain,  $A_{DC-OUT}$  is:

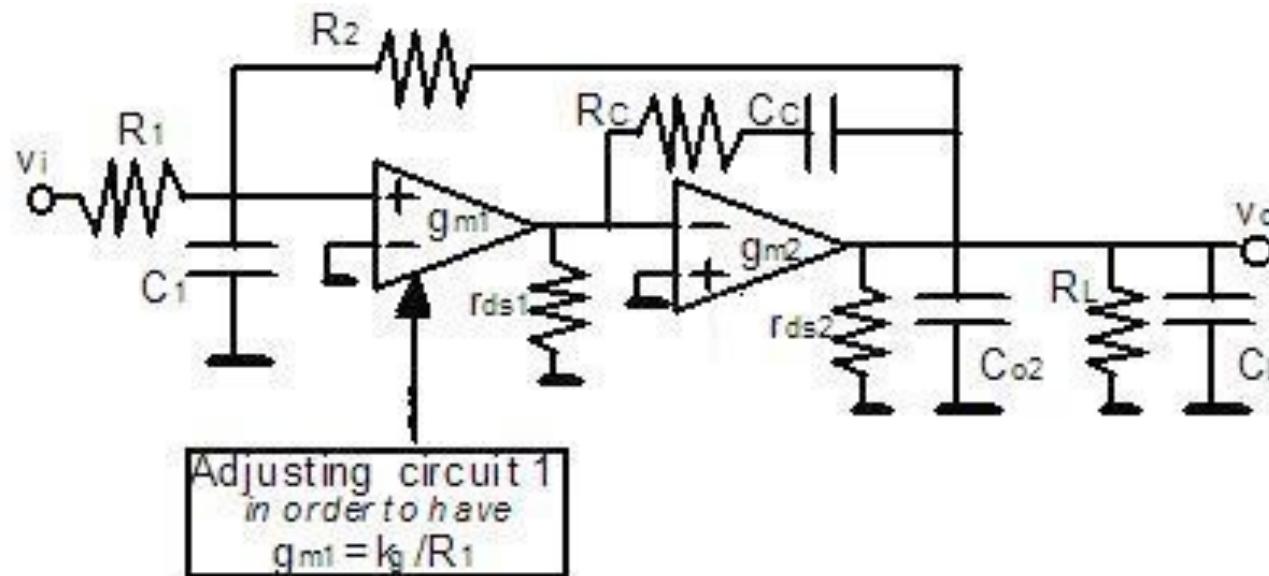
$$A_{DC-OUT} = -g_{m5} \cdot R_{o2} = -\frac{R_{o2}}{R_{b0}}$$



# Active-Gm-RC filters

## Linearity performance (I)

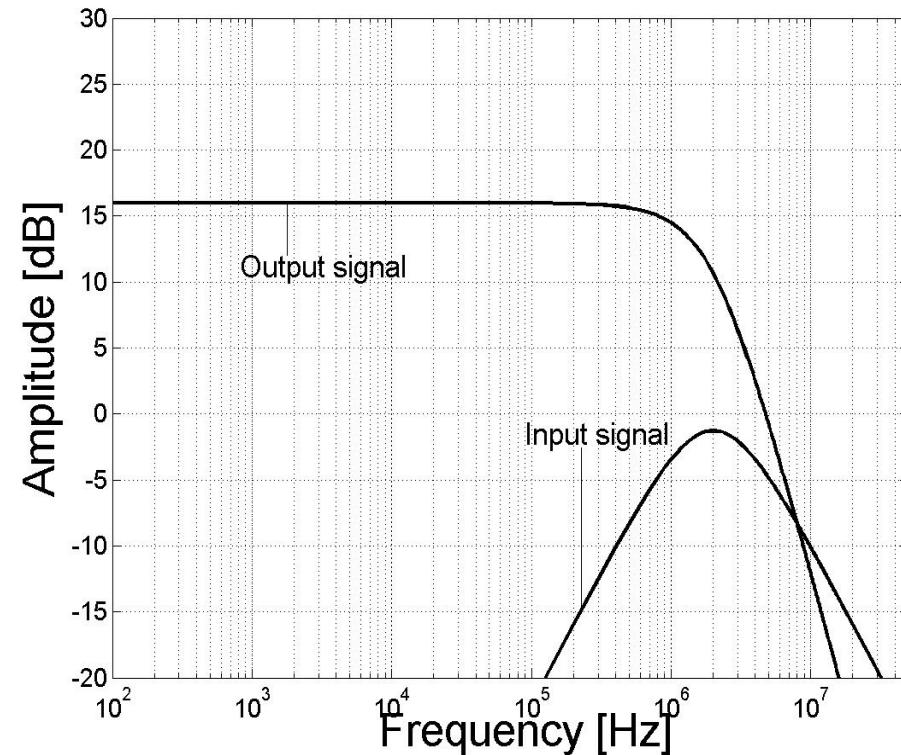
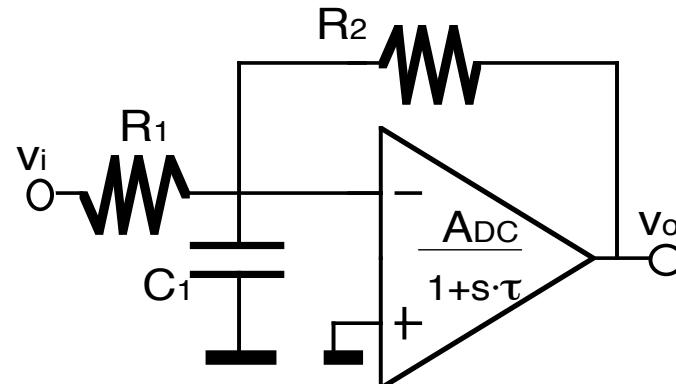
- The main source of non-linearity can be found in the op-amp performance
  - the input stage transconductance non-linearity
  - the output stage current swing limitation



# Active-Gm-RC filters

## Linearity performance – Input stage

- At frequency lower than the pole frequency
  - Increasing the input signal frequency increases the opamp input signal amplitude
  - The opamp open-loop gain decreases with a single pole roll-off



# Active-Gm-RC filters

## Linearity performance – Input stage

- When the signal frequency overcomes the filter pole frequency
  - the output signal amplitude decreases with the square law of the frequency due to the two-pole roll-off of the 2<sup>nd</sup> order frequency response
  - the opamp input signal decreases with a linear law
- $HD_{3in}(s)$  is the input device overdrive voltage:
$$HD_{3in}(s) = \frac{1}{32} \cdot \frac{V_{in}^2}{V_{ov1}^2} \cdot \frac{|H_{LP}(s)|^2}{|A(s)|^3} \cdot |H_{LP}(3 \cdot s)|$$
  - $V_{in}$  is the input signal amplitude, and
  - the input device overdrive voltage ( $V_{ov1} = V_{GS1} - V_{TH}$ ) controls  $HD_{3in}$ .
- $A(s)$  is the opamp transfer function
- $HD_{3in}(s)$  is frequency-dependent with a band-pass frequency behavior
  - **in the filter band**, it increases with frequency increase.
    - This limitation dominates for in-band higher frequency input signal.
  - **out of the filter band** this non-linear behavior reduces and the filter linearity tends to increase



# Active-Gm-RC filters

## Linearity performance – Output stage

- At low frequencies
  - the opamp gain is very large and a very small signal is present at the opamp input nodes, since it behaves as virtual ground.
  - the input stage exhibits a good linear behavior, and the output stage contribution to the distortion is dominant
  - to minimize  $HD_{3out}$ , the output stage DC-gain ( $A_{DCout}$ ) has to be as large as possible because, at parity of output signal level, the output stage driving signal, that determines the harmonics amplitude, is lower.

$$A_{DCout} = g_m 2 \cdot R_{out}$$

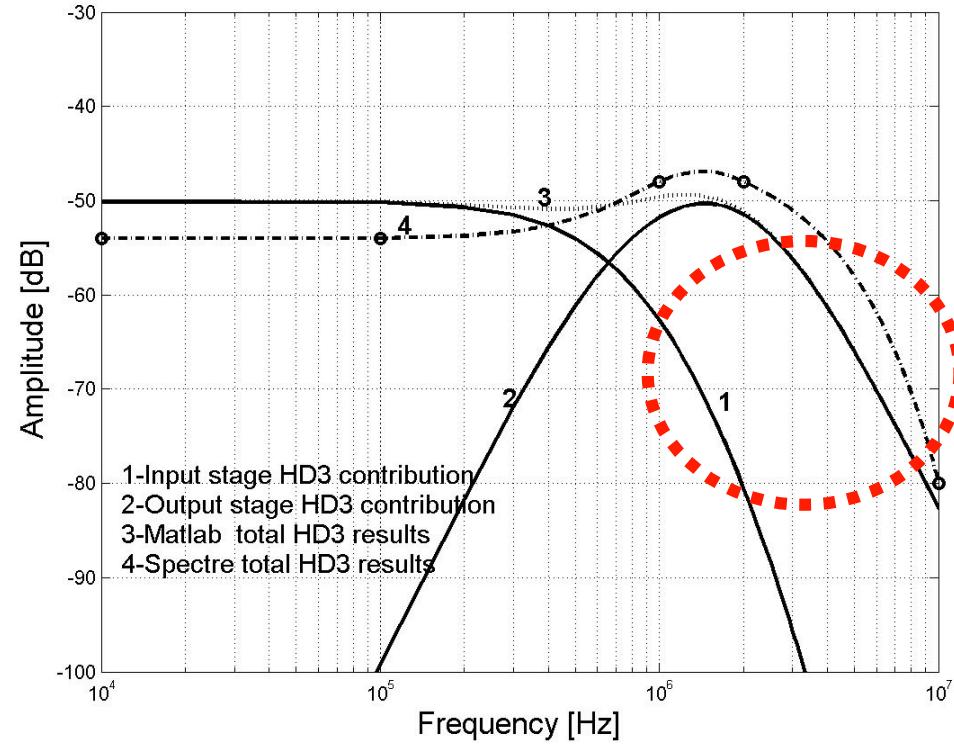
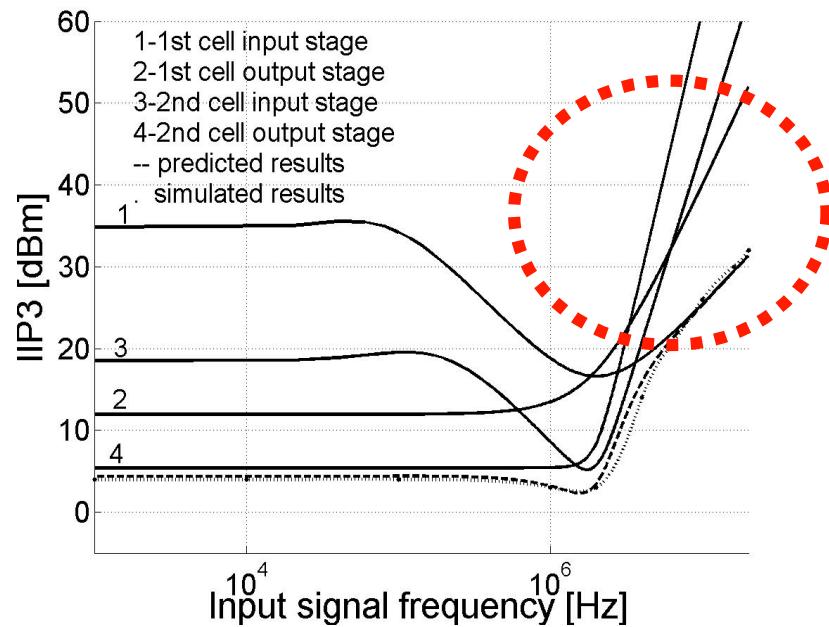
- The 3<sup>rd</sup> order harmonic distortion factor for output stage configuration is:

$$HD_{3out}(s) = \frac{1}{24} \cdot \frac{V_{in}^2}{(n \cdot V_t)^2} \cdot \frac{|H_{LP}(s)|^2}{|A_{DCout}|^3} \cdot |H_{LP}(3 \cdot s)|$$



# Active-Gm-RC filters

## Linearity performance (II)



# Active-Gm-RC filters

## Noise performance

- The noise performance is determined by the thermal noise of the resistances  $R_1$  and  $R_2$  and the op-amp input referred noise
- The total op-amp input referred noise is due to the thermal noise of the input transistors, the input referred noise of the entire fully differential cell can be calculated as follows:

$$IRN = \sqrt{8 \cdot kT \cdot \left( R_1 + \frac{R_2}{K_{LP}^2} + \frac{8}{3g_{m1}} \left( 1 + \frac{R_1}{R_2} \right)^2 \left( 1 + \frac{Q_{LP}^2}{3} \right) \right)}$$

- Indicating  $K_G = 1/(g_{m1} R_1)$ , the input referred noise calculation can be simplified as follows:

$$IRN = \sqrt{8 \cdot kT \cdot R_1 \cdot \left( 1 + \frac{1}{K_{LP}} + \frac{8 \cdot K_G}{3} \left( \frac{K_{LP} + 1}{K_{LP}} \right)^2 \left( 1 + \frac{Q_{LP}^2}{3} \right) \right)}$$



# Active-Gm-RC filters

## Signal-to-Noise Ratio

- By designing the cell in order to present a constant in-band linearity performance, the cell dynamic range & SNR, can be approximately evaluated as follow, for a -40dB HD3 level:

$$\text{SNR} = \frac{25 \cdot (K_{LP} + 1)^2 \cdot V_{ov}^2}{8 \cdot k \cdot T \cdot K_{LP}^2 \cdot \left[ 1 + \frac{1}{K_{LP}} + \frac{8}{3} \cdot K_G \cdot \left( \frac{K_{LP} + 1}{K_{LP}} \right)^2 \cdot \left( 1 + \frac{Q_{LP}^2}{3} \right) \right] \cdot \omega_{LP}}$$



# Active Gm-RC Filters

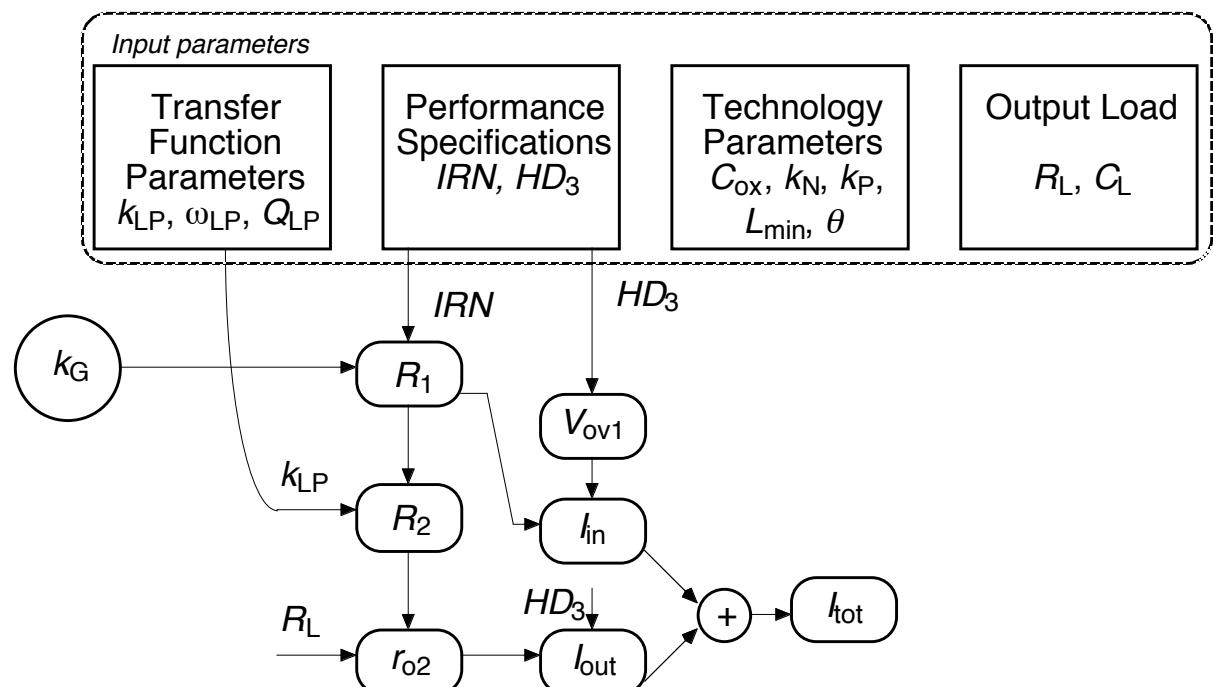
## Methodology Description

- A design methodology is possible
  - for speed-up the design
  - for preliminary system evaluation

- The method is divided in two steps:

**Step 1:** the power consumption minimization provides a current optimisation procedure oriented to power consumption minimization;

**Step 2:** the Component size design calculates the sizes of MOS transistors and of the feedback network parameters



# Active Gm-RC Filters

## Methodology Description

- Noise performance

$$IRN = \sqrt{8 \cdot kT \cdot R_1 \cdot \left( 1 + \frac{1}{K_{LP}} + \frac{8 \cdot K_G}{3} \left( \frac{K_{LP} + 1}{K_{LP}} \right)^2 \left( 1 + \frac{Q_{LP}^2}{3} \right) \right)}$$

- For a required IRN, R1 is given by:

$$R_1(k_G) = \frac{IRN^2}{8 \cdot k \cdot T \cdot \left( 1 + \frac{1}{k_{LP}} + \frac{8 \cdot k_G}{3} \cdot \left( 1 + \frac{1}{k_{LP}} \right)^2 \cdot \left( 1 + \frac{Q_{LP}^2}{3} \right) \right)}$$

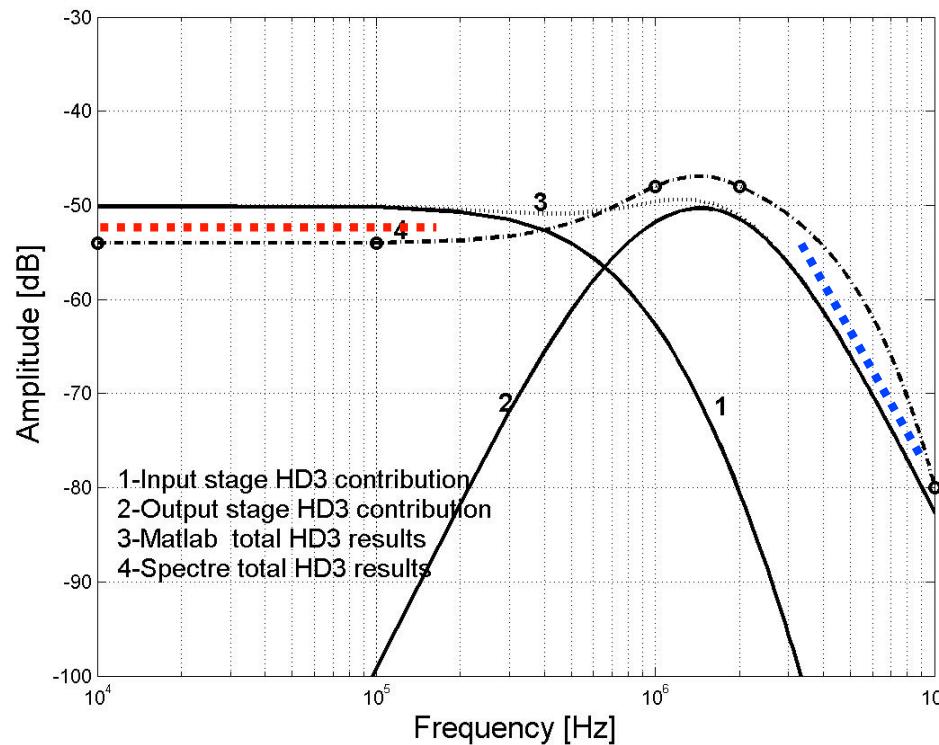


# Active Gm-RC Filters

## Methodology Description

- Linearity (HD3)

Typical HD3 vs. frequency



- At **low frequencies** the main contribution is due to output stage
- At **high frequency** the input stage distortion dominates
- → Both stages are designed to have the same  $HD3$  value

$$HD3_{in}(\omega_{LP}) = HD3_{out}(0) = HD3_{spec}$$

- $HD3_{spec}$  is the in input data specification



# Active Gm-RC Filters

## Methodology Description

- Input-stage Linearity (HD3)

$$HD_{3in}(s) = \frac{1}{32} \cdot \frac{V_{in}^2}{V_{ov1}^2} \cdot \frac{|H_{LP}(s)|^2}{|A(s)|^3} \cdot |H_{LP}(3 \cdot s)|$$

- The input device overdrive  $V_{ov1}$

$$V_{ov1} = \sqrt{\frac{V_s^2}{32 \cdot HD3_{dB} \cdot \sqrt{1 + 64 \cdot Q_{LP}^2}}} \cdot \left( \frac{k_{LP}}{1 + k_{LP}} \right)^3$$

- Since  $I_{in} = \frac{V_{ov1} \cdot g_{m1}}{2}$  and  $g_{m1} = \frac{1}{k_G \cdot R_1}$ , the input stage current level ( $I_{in}(k_G)$ ) is:

$$I_{in}(k_G) = \frac{V_{ov1}}{k_G \cdot R_1(k_G)}$$



# Active Gm-RC Filters

## Methodology Description

- Output-stage Linearity (HD3)

$$HD_{3out}(s) = \frac{1}{24} \cdot \frac{V_{in}^2}{(n \cdot V_t)^2} \cdot \frac{|H_{LP}(s)|^2}{|A_{DCout}|^3} \cdot |H_{LP}(3 \cdot s)|$$

- Similarly the output stage current level can be obtained
- The output stage has to deliver to the resistive load connected to the output node
  - The total resistive load  $R_{out}(k_G)$  is given by the parallel of the effective load ( $R_L$ , given in the specifications) and of the feedback resistance ( $R_2(k_G) = k_{LP} \cdot R_1(k_G)$ ).
- $R_{out}(k_G)$  can be written as:

$$R_{out}(k_G) = \frac{k_{LP} \cdot R_1(k_G) \cdot R_L}{k_{LP} \cdot R_1(k_G) + R_L}$$

- The output stage current level is obtained:

$$I_{out}(k_G) = \frac{k_{LP}}{R_{out}(k_G)} \cdot \sqrt[3]{\frac{1}{24} \cdot \frac{V_{in}^2 \cdot n \cdot V_t}{HD3}}$$

$$A_{DCout} = \frac{k_{LP}}{n \cdot V_t} \cdot \sqrt[3]{\frac{1}{24} \cdot \frac{V_{in}^2 \cdot n \cdot V_t}{HD3}}$$



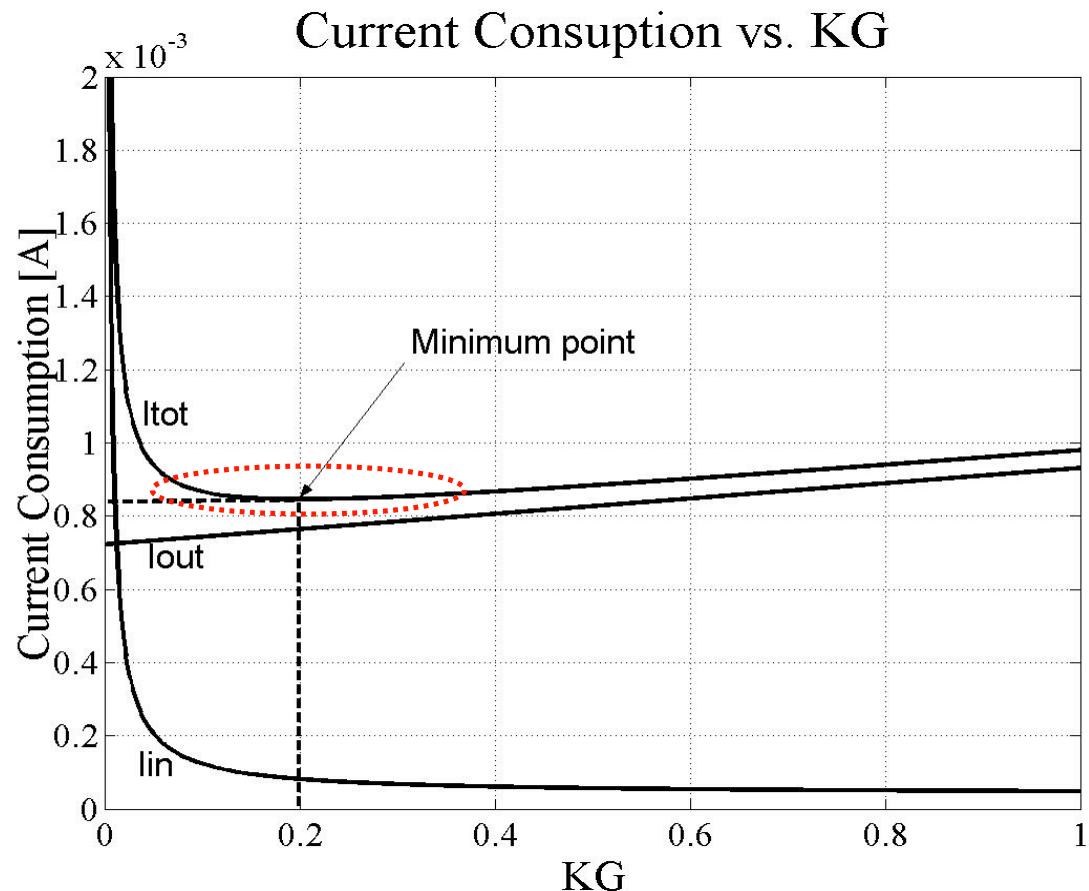
# Active Gm-RC Filters

## Methodology Description

- The total current  $I_{tot}$  is a function of  $k_G$ :

$$I_{tot} = I_{in}(k_G) + I_{out}(k_G) = f(k_G)$$

- There is a set of values of  $k_G$  for which the current remains very close to the minimum value
- $k_G$  is selected in this set of values in order to optimize other design parameters (e.g. matching and layout)



# Active Gm-RC Filters

## Methodology Description

- Once that the  $k_G$  value is selected
- The passive network parameters will be:

$$R_2 = k_{LP} \cdot R_{1\_min}$$

$$C_1 = \frac{Q_{LP} \cdot (k_{LP} + 1)}{R_{1\_min} \cdot \omega_{LP} \cdot k_{LP}}$$

$$C_C = \frac{Q_{LP} \cdot (k_{LP} + 1)}{k_{Gmin} \cdot R_{1\_min} \cdot \omega_{LP} \cdot Q_{LP} \cdot (1 + k_{LP})}$$

- It is now possible to derive input and output transistors sizing ( $g_{m1} = \omega_U \cdot C_C$ )

- The input device sizes are:

$$\left(\frac{W}{L}\right)_{in} = \frac{g_{m1}}{2 \cdot V_{ov1} \cdot k_{xp}}$$

- The output device sizes are:

$$\left(\frac{W}{L}\right)_{out} = \frac{I_{out\ min}}{2 \cdot (n \cdot V_t)^2 \cdot k_{xn}}$$

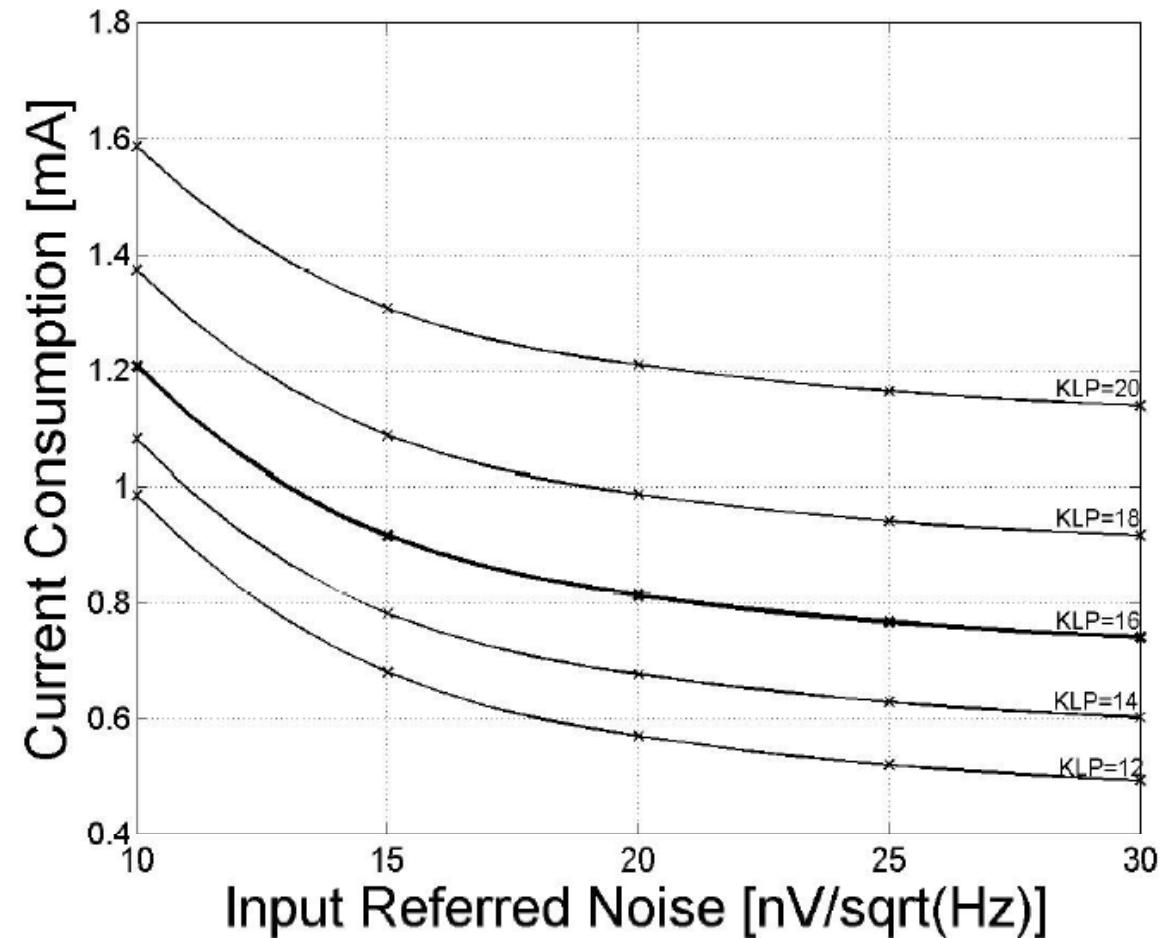


# Active Gm-RC Filters

## System evaluation

- The tool-box allows to make parametrical current consumption evaluation
- Example I

I (IRN & DC-Gain)

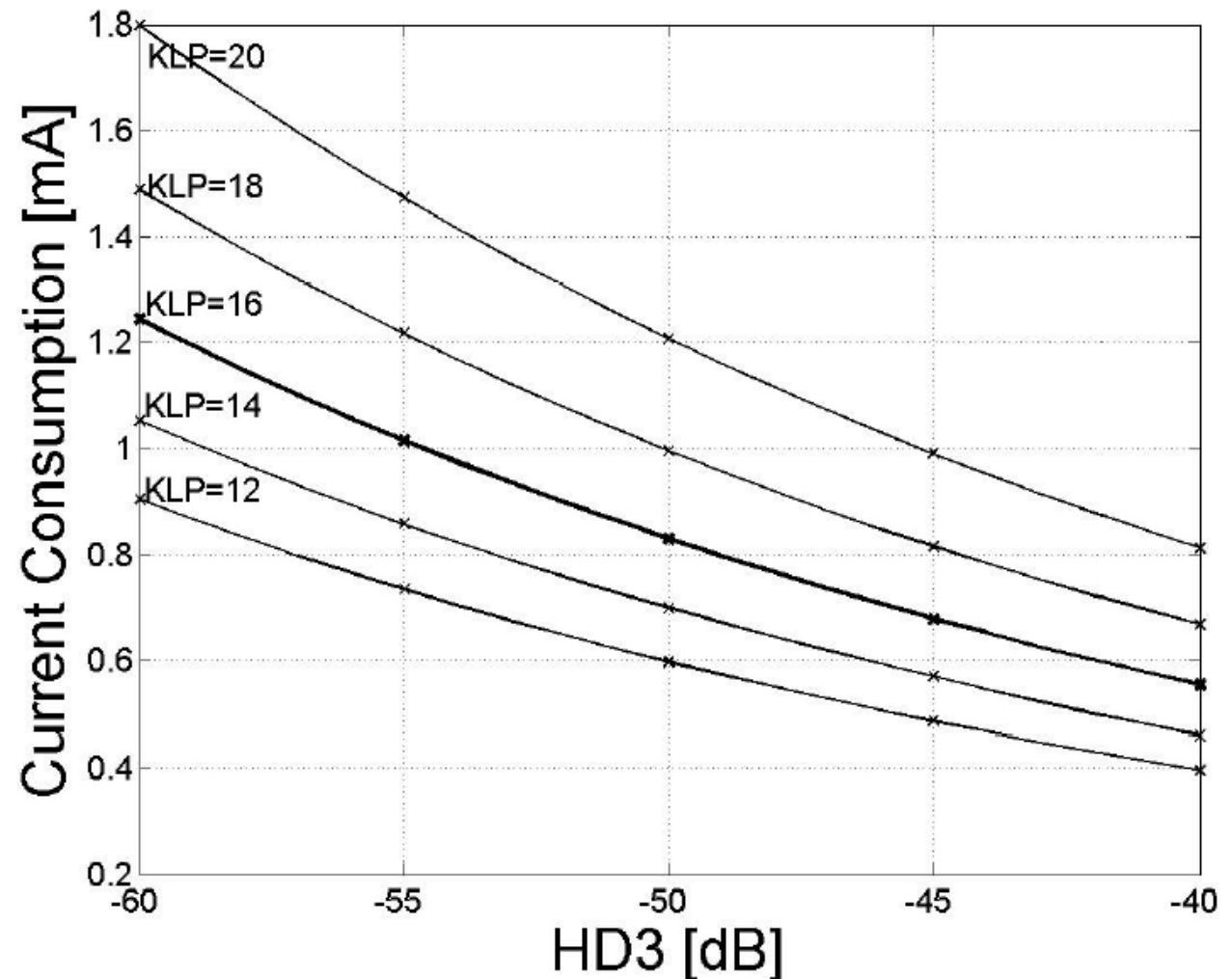


# Active Gm-RC Filters

## System evaluation

- Example II

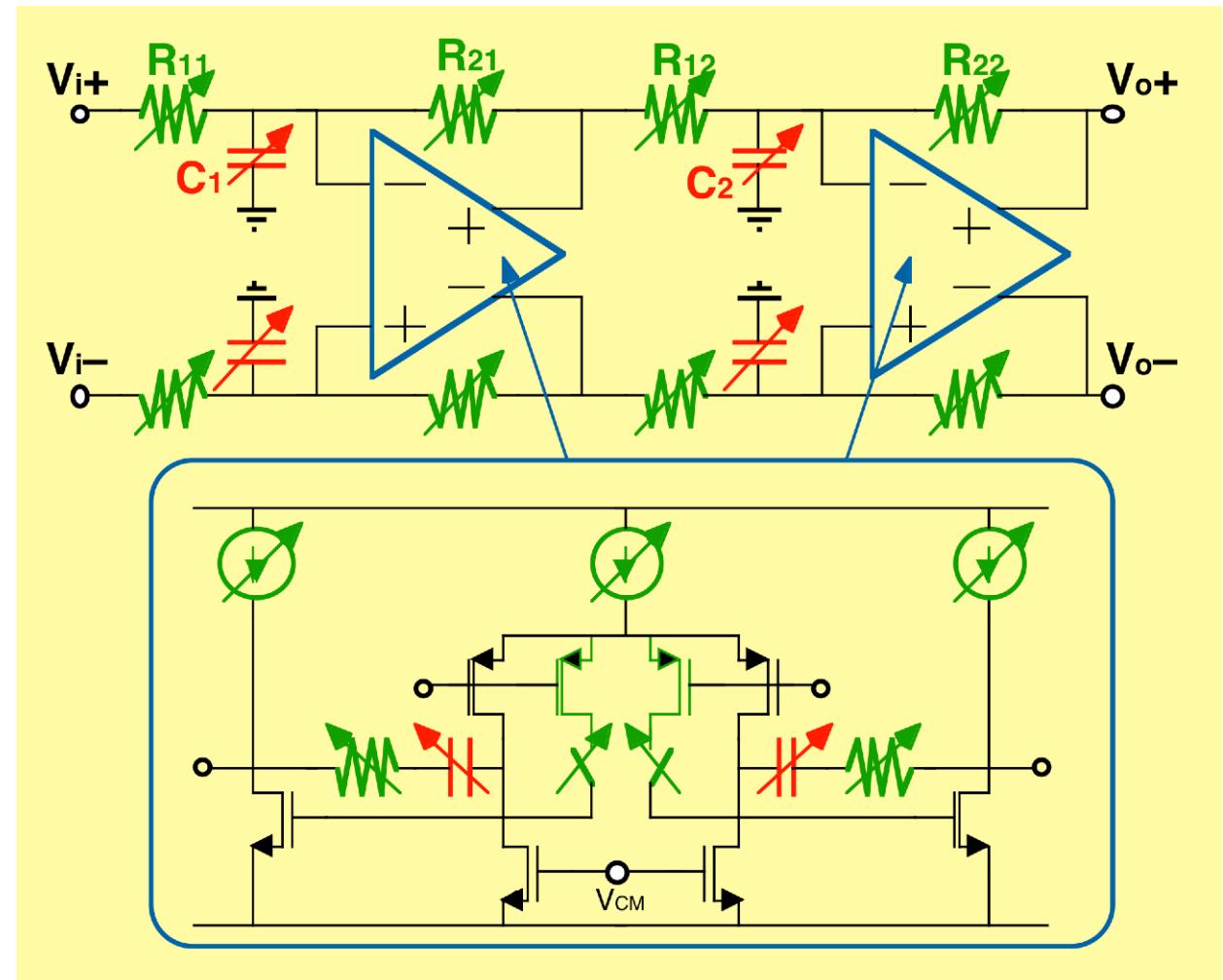
I (HD3 & DC-Gain)



# Active-Gm-RC cell

Design example (D'Amico, ESSCIRC2005)

- Reconfigurable filter
  - Red control
    - 4-bit for Technology spread compensation
  - Green control
    - 1-bit for UMTS/WLAN selection



# Active-Gm-RC Filters

Design example (D'Amico, ESSCIRC2005) : 4<sup>th</sup> order Bessel Filter

	UMTS	WLAN
Technology	0.13 $\mu$ m CMOS @ <b>1.2V</b>	
Die area occupation		2.8mm <sup>2</sup>
f <sub>-3dB</sub>	2.11MHz	11MHz
f <sub>-3dB</sub> Programmable Range	[1.45-3.6] MHz	[5.87-19.44] MHz
Programmable $\Delta f_{-3dB}$ step	135kHz	850kHz
DC-gain	4dB	4dB
Input-referred noise	36 $\mu$ V <sub>rms</sub>	36 $\mu$ V <sub>rms</sub>
In-band IIP3	<b>21dBm</b>	<b>21dBm</b>
Out-of-band IIP3	<b>31dBm</b>	n.a.
1dbCP ( $f_i=f_o/3$ )	11dBm	10.6dBm
THD=-40dB ( $f_i=f_o/3$ )	1.8V <sub>pp</sub>	1.8V <sub>pp</sub>
Power consumption	3.4mW	14.2mW

*Large in-band linearity  
(1dB<sub>CP</sub> @  $\pm 1.1$ V<sub>p</sub> output voltage) w.r.t. the supply voltage (1.2V)*

*Larger out-of-band linearity*





*Dipartimento di Ingegneria dell' Innovazione  
Universita' degli Studi di Lecce*

*Andrea Baschirotto*

[andrea.baschirotto@unile.it](mailto:andrea.baschirotto@unile.it)

---

## Analog Filters for Telecommunications

*Universita' degli Studi di Bologna*

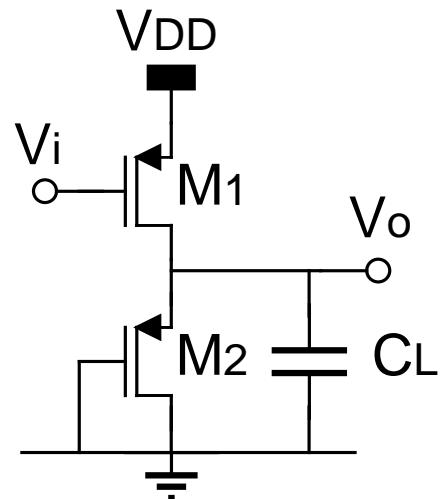
*June, 16<sup>th</sup>-17<sup>th</sup>, 2005*

## Gm-Gm-C Filters



# Basic Gm-Gm-C filter

1<sup>st</sup> order cell



$$H(s) = \frac{V_o}{V_i} = -\frac{g_{m1}}{g_{m2}} \cdot \frac{1}{1 + s \cdot C_L / g_{m2}}$$

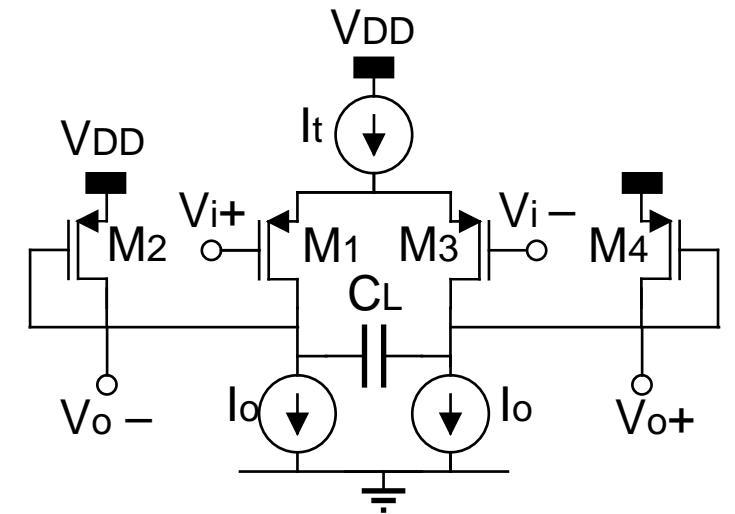
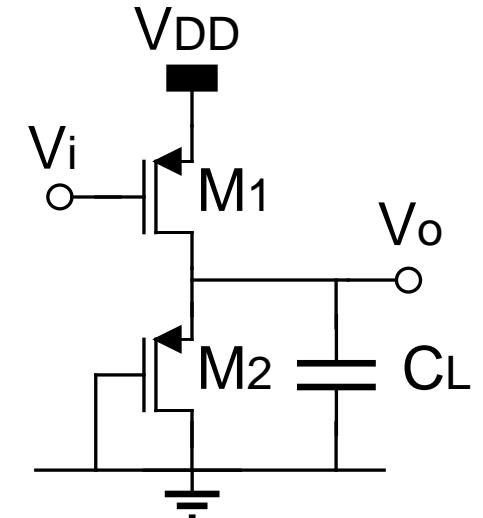
- MOS devices (M1 and M2) operates in saturation region



# Basic Gm-Gm-C filter

## 1<sup>st</sup> order cell – Key advantages

- Low-power consumption:
  - the same bias current is shared between the driver ( $M_1$ ) and the load ( $M_2$ ) device
- Accurate frequency response:
  - no non-dominant poles are present since only one node is present, and it corresponds to the desired pole
- No body effect
  - no threshold voltage variation, due to body effect occurs since only PMOS devices with  $V_{SB}=0$  are present
- In the fully-differential version, absence of CMFB circuit
  - the output DC voltage is fixed by the  $V_{GS}$  of transistors  $M_5$  and  $M_6$
  - this avoids additional power consumption

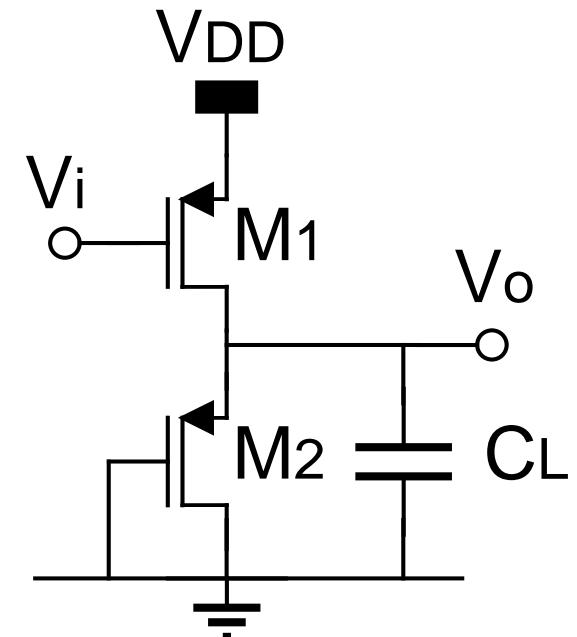


# Basic Gm-Gm-C filter

## 1<sup>st</sup> order cell – Key advantages

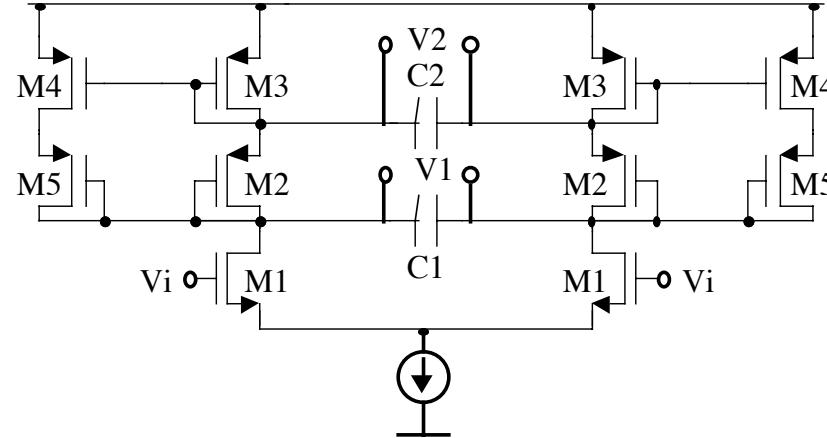
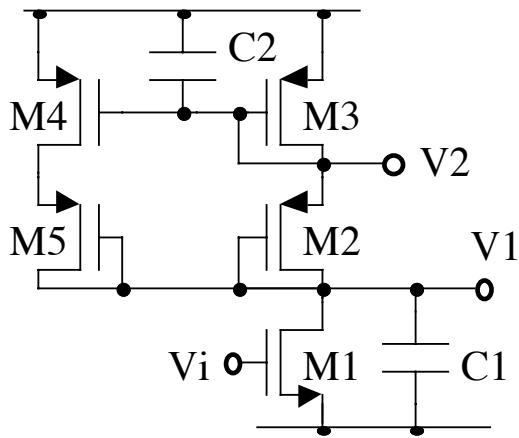
- Medium/High-linearity:

- Driver device (M1) and load device (M2) are of the same type (PMOS)
- Their characteristics are largely non linear,
- BUT *the driver non-linearity* ( $g_{m1}$ ) *is compensated by the opposite load non-linearity* ( $\approx 1/g_{m2}$ )
- → large linear range can be achieved even with a reduced device overdrive.
- Ex.: for a differential version, with  $V_{ov}=V_{GS}-V_{TH}=V_{ov}\approx 450\text{mV}$ , a THD=-50dB for a 800mVpp input signal @25MHz results.
  - In other solutions this result should be achieved by using a much larger  $V_{ov}$ .
- → A smaller current and so a lower power is required



# Basic Gm-Gm-C filter

2<sup>nd</sup> order cell



$$H_2(s) = \frac{V_2}{V_i} = -\frac{G_1 \cdot G_2}{s^2 \cdot C_1 \cdot C_2 + s \cdot (C_1 \cdot (G_3 + G_2) + C_2 \cdot G_2) + G_2 \cdot (G_3 + G_4)}$$

$$H_1(s) = \frac{V_1}{V_i} = -\frac{G_1 \cdot (G_2 + G_3 + sC_2)}{s^2 \cdot C_1 \cdot C_2 + s \cdot (C_1 \cdot (G_3 + G_2) + C_2 \cdot G_2) + G_2 \cdot (G_3 + G_4)}$$

- The MOS output impedance have been neglected since they should be much higher than node 1 and 2 impedance given by  $1/G_m$



# Basic Gm-Gm-C filter

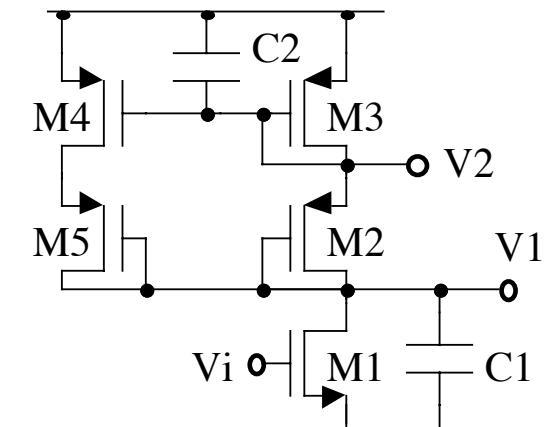
## 2<sup>nd</sup> order cell

$$H_2(s) = \frac{V_2}{V_i} = -\frac{G_1 \cdot G_2}{s^2 \cdot C_1 \cdot C_2 + s \cdot (C_1 \cdot (G_3 + G_2) + C_2 \cdot G_2) + G_2 \cdot (G_3 + G_4)}$$

- Assuming  $G_2=G_3$  (the same aspect ratio with same current),  $G_4=A \cdot G_3$  and  $C_2=k \cdot C_1$

$$\omega_o = \frac{G_2}{C_1} \cdot \sqrt{\frac{1+A}{k}} \quad Q = \frac{\sqrt{k \cdot (1+A)}}{1+2 \cdot k}$$

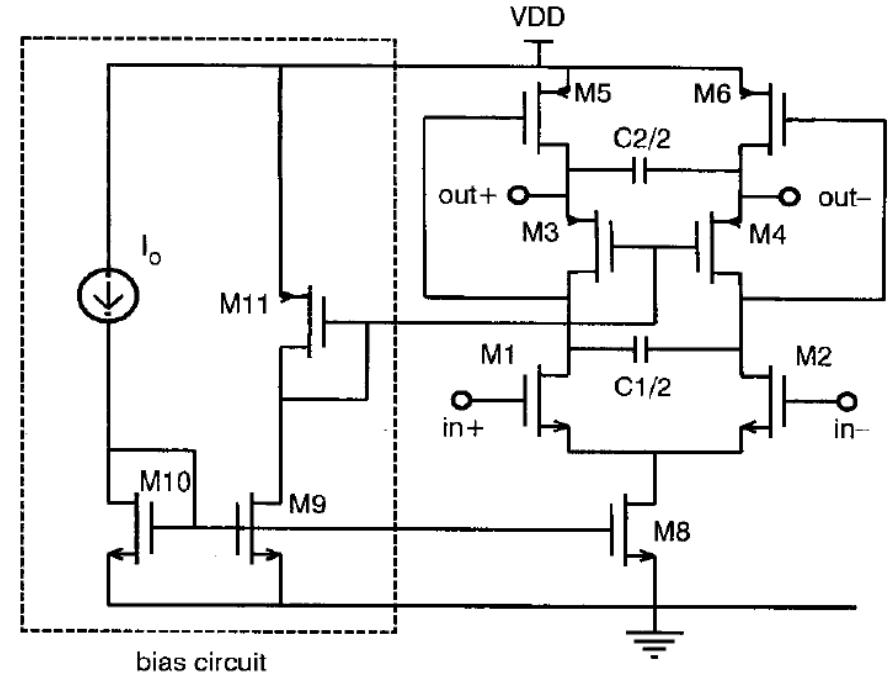
- The  $\omega_o$  depends from  $G_2 \rightarrow$  it can be tuned by the dc current level (quadratic law)
- The  $Q$  value depends only from aspects ratio  $\rightarrow$  it is constant w.r.t. tuning variation.
- $\omega_o$  and  $Q$  depend only from PMOS device aspect parameters  $\rightarrow$   
they are independent from technology variations
- M5 improves improve bias condition matching and consequently  
the current mirror accuracy between M3 and M4 is increased



# Basic Gm-Gm-C filter

## 2<sup>nd</sup> order cell – II version

- For  $g_{m3} \gg g_{ds5}$  and  $g_{m5} \gg g_{ds1}$



$$H(s) = \frac{V_o}{V_i} = - \frac{G_{m1}/G_{m3}}{s^2 \cdot C_1 \cdot C_2 / (G_{m3} \cdot G_{m5}) + s \cdot (C_1/G_{m5}) + 1}$$

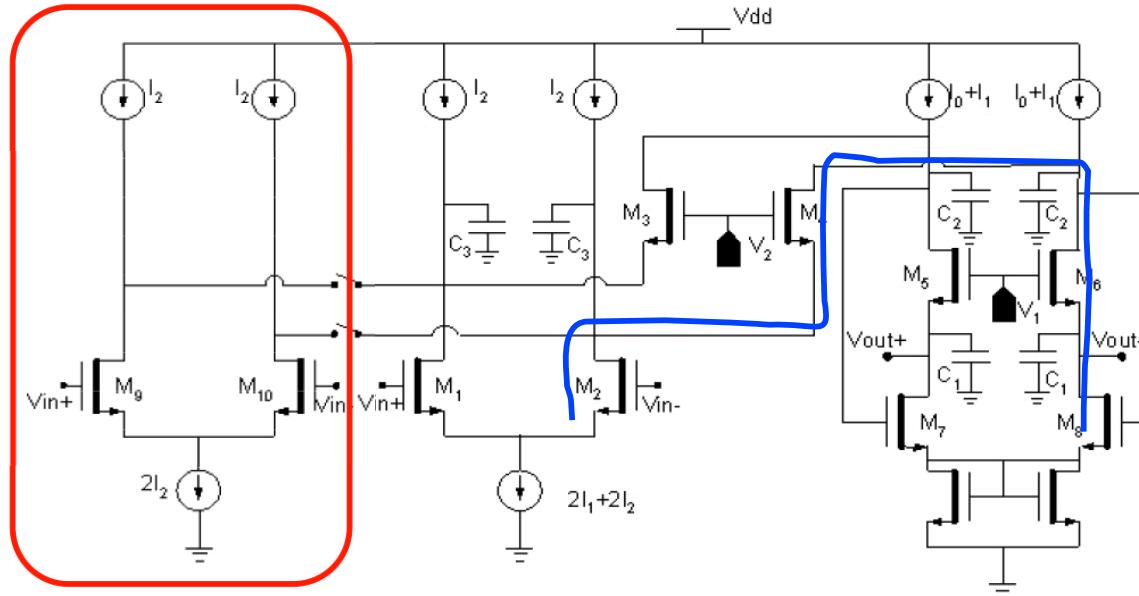
$$\omega_o = \sqrt{\frac{G_{m3} \cdot G_{m5}}{C_1 \cdot C_2}} \quad Q = \sqrt{\frac{G_{m5} \cdot C_2}{G_{m3} \cdot C_1}}$$



# Basic Gm-Gm-C filter

3<sup>rd</sup> order cell – II version

Additional input stage  
for gain control



Only NMOS  
transistor in the  
signal path

$$\frac{V_{out}}{V_{in}} = \frac{\frac{g_{m1}}{g_{m5}}}{s^3 \frac{C_1 C_2 C_3}{g_{m3} g_{m5} g_{m7}} + s^2 \left( \frac{C_1 C_2}{g_{m3} g_{m7}} + \frac{C_3 C_2}{g_{m5} g_{m7}} \right) + s \left( \frac{C_1}{g_{m3}} + \frac{C_2}{g_{m7}} \right) + 1}$$

$$\omega_1 = -\frac{g_{m3}}{C_1} \quad \omega_{2/3} = \sqrt{\frac{g_{m5} \cdot g_{m7}}{C_2 \cdot C_3}} \quad Q_{2/3} = \sqrt{\frac{C_3 \cdot g_{m7}}{C_2 \cdot g_{m5}}}$$

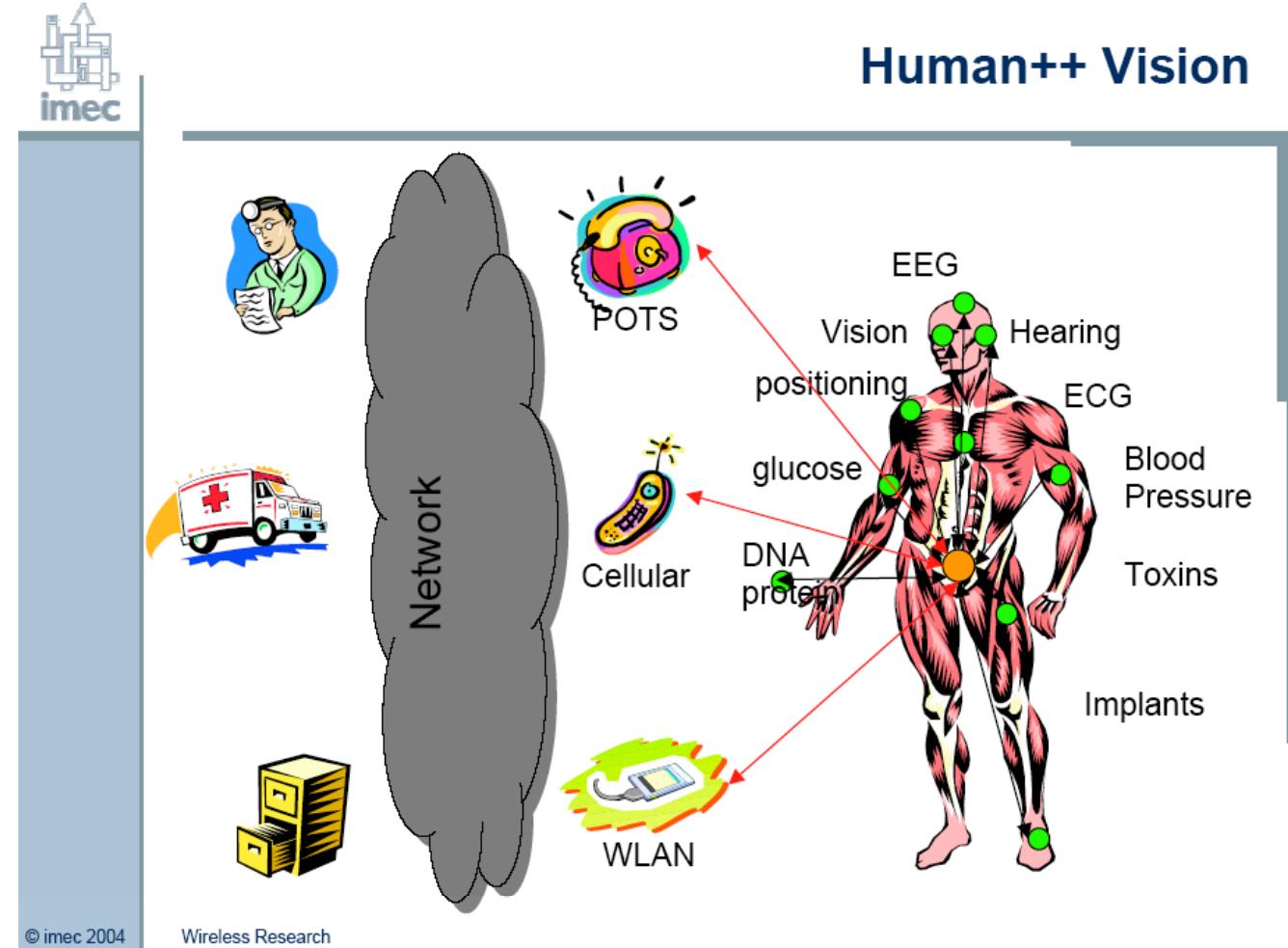
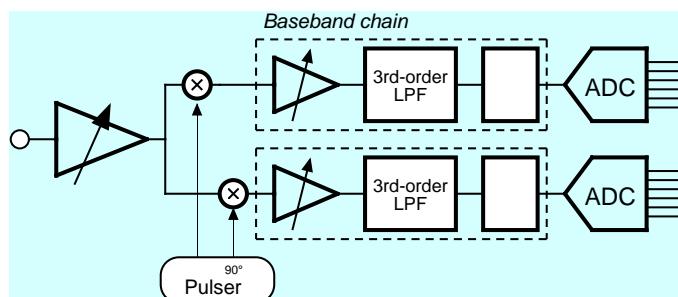


# Basic Gm-Gm-C filter

## 3<sup>rd</sup> order cell – II version – Application

- Ultra-Wide-Band (UWB) receiver for Wireless Body Area Network (WBAN)

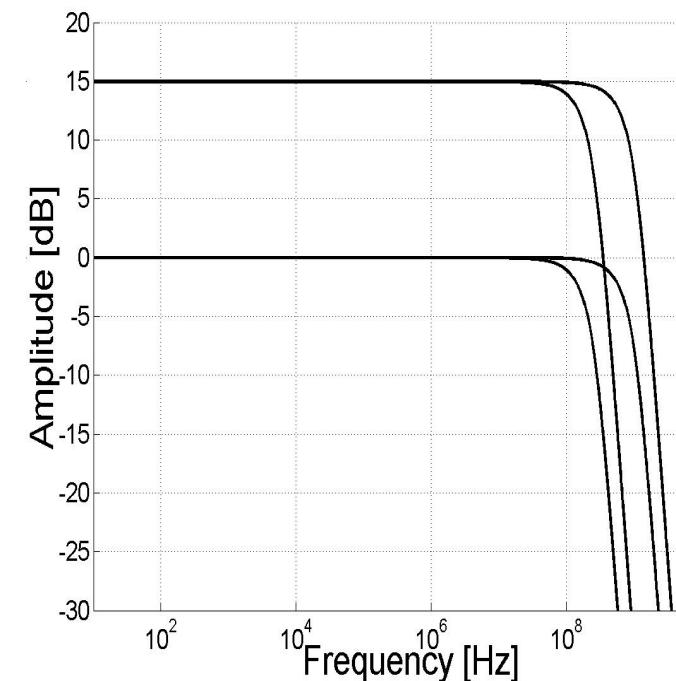
- Requirements:
- Very large bandwidth ( $\approx$  1GHz)
- Low Dynamic Range (25-30 dB)
- Low power consumption



# Basic Gm-Gm-C filter

## Simulated performance

Case	I	II	III	IV
$f_o$ [MHz]	250		1000	
DC-Gain [dB]	0	15	0	15
IR-Noise Level [ $\text{nV}/\sqrt{\text{Hz}}$ ]	18	4.5	10	2.5
IR-In-band Noise [ $\mu\text{V}_{\text{rms}}$ ]	285	71	320	80
THD@100mVpp [dB]	-30	-30	-32	-37
SNR [dB]	45	53	44	53
Power consumption [mW]	0.21	1.2	0.59	3.2





*Dipartimento di Ingegneria dell' Innovazione  
Universita' degli Studi di Lecce*

*Andrea Baschirotto*

*andrea.baschirotto@unile.it*

---

## **Analog Filters for Telecommunications**

*Universita' degli Studi di Bologna*

*June, 16<sup>th</sup>-17<sup>th</sup>, 2005*

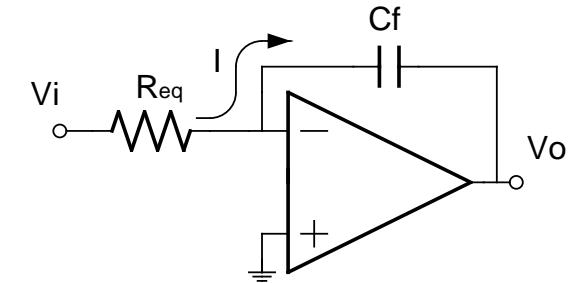
## **Tuning circuits**



# Active filters draw-backs

- An active filter is made of op-amps, resistors and capacitors
- The accuracy of the filter is determined by the accuracy of the realized time constants

$$\left(\frac{\delta\tau}{\tau}\right)^2 = \left(\frac{\delta R}{R}\right)^2 + \left(\frac{\delta C}{C}\right)^2$$

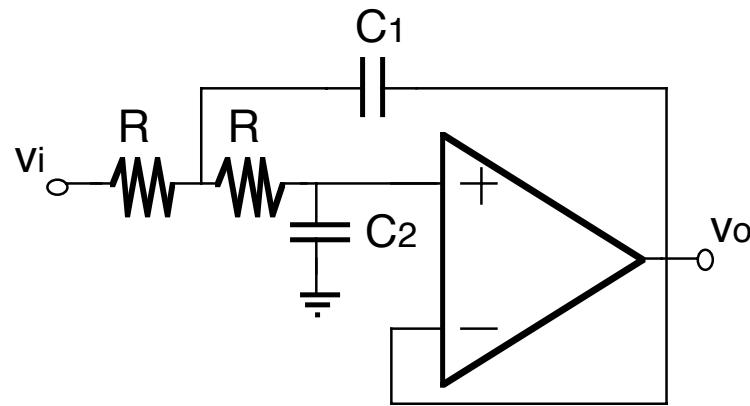


- Capacitors and resistors are realized by uncorrelated technological steps
- In CMOS technology  $\frac{\delta R}{R} \approx 40\%$ , and  $\frac{\delta C}{C} \approx 30\%$   
 $\Rightarrow \frac{\delta\tau}{\tau} \approx 50\%$ , unacceptable for most of the applications
- Problems for a fully integrated realization
  - Accuracy
  - Large capacitors and resistors values
- Example:
  - For 70 nm oxide thickness  $1 \text{ pF} \rightarrow 2000 \mu\text{m}^2$ ;
  - $10\text{pF}$  is a large capacitance
  - To get  $\tau = 0.1\text{msec}$ ,  $R=10M\Omega$



# Tuning circuits

- Continuous-Time (CT) filters strongly require a tuning system to align their frequency response
  - Pole frequency ( $\omega_0$ )
    - to compensate for component variations from their nominal values (due to technological spread, aging, temperature, etc.)
    - to align the filter frequency response to different target frequency responses as required, for instance, by a multi-standard telecommunication terminal
  - Pole quality factor ( $Q$ )
- Ex.: Sallen&Key Low-pass Biquadratic cell

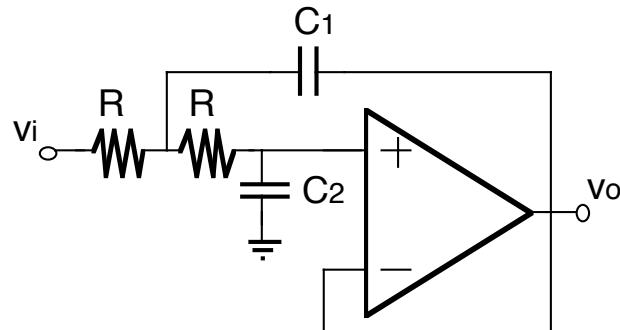


$$H(s) = \frac{1}{1 + 2 \cdot R \cdot C_2 \cdot s + R^2 \cdot C_1 \cdot C_2 \cdot s^2}$$

$$\omega_0 = \frac{1}{\sqrt{C_1 \cdot C_2 \cdot R}} \quad Q = \frac{1}{2} \cdot \sqrt{\frac{C_1}{C_2}}$$



# Tuning circuits



$$H(s) = \frac{1}{1 + 2 \cdot R \cdot C_2 \cdot s + R^2 \cdot C_1 \cdot C_2 \cdot s^2}$$

- $\omega_o$  depends on parameter **absolute value** spread

$$\omega_o = \frac{1}{\sqrt{C_1 \cdot C_2} \cdot R}$$

=>  $\omega_o$ -tuning is needed

- $Q$  depends on parameter **matching** spread

$$Q = \frac{1}{2} \cdot \sqrt{\frac{C_1}{C_2}} \quad \Rightarrow \quad \frac{\delta Q}{Q} = \frac{1}{2} \cdot \frac{\delta C}{C}$$

In telecom ZIF-receiver low- $Q$  filter are used

=>  $Q$ -tuning is typically not needed (for the integrated component matching)

**Only  $\omega_o$ -tuning circuits will be presented**

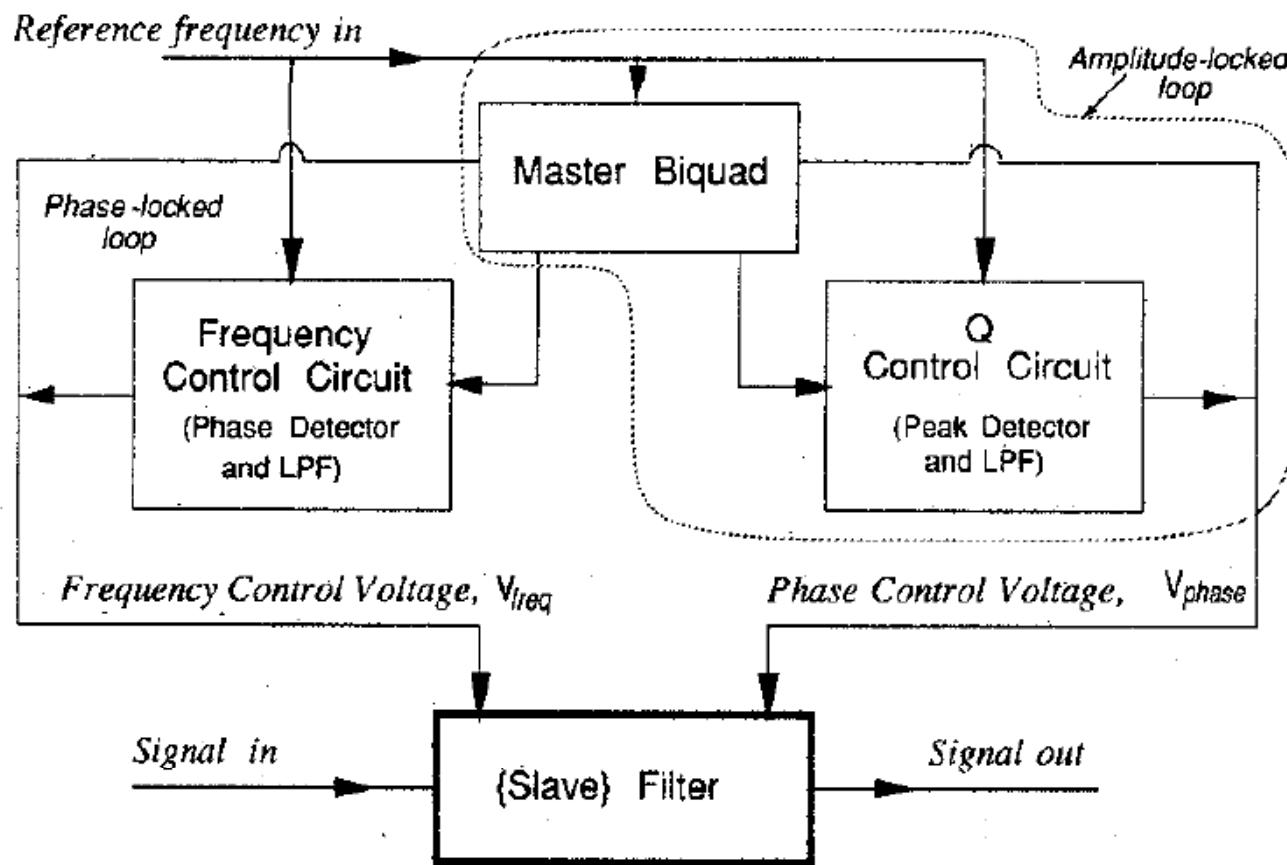


# $\omega_o$ - and Q- Tuning circuits

- Two concurrent tuning loops

Synchronization

Stability



# Tuning techniques

- Several tuning techniques have been proposed in the literature
- They can be described and compared in terms of the following parameters:
  - Frequency response accuracy:
    - Strongly dependent on the tuning circuit implementation
    - In pure analog tuning systems this could be limited by typical analog circuit non-idealities (gain, offset, etc.)
    - In mixed signal solutions the accuracy is limited also by the number of bit used in the digital part
  - Time for tuning:
    - Important when the filter frequency response has to be aligned for different frequency response targets in a short time
    - Ex.: commuting between different communication standards
  - Interactions with filter performance:
    - Filter performances should be independent of tuning circuit operation.



# Tuning systems

## Master-Slave approach

- A slave filter processes the input signal
- A master filter for tuning purpose is matched with the slave circuit
- In the master a time constant is adjusted to compensate for any freq-resp deviation
  - One or more component values are adjusted by means of a tuning control signal
  - The control signal is passed to the matched slave filter
    - The slave frequency response is adjusted to process the true input signal
- The master-slave tuning scheme is effective only if a good matching between the master and the slave circuits is possible
  - When the matching is critical the Master-Slave approach isn't useful



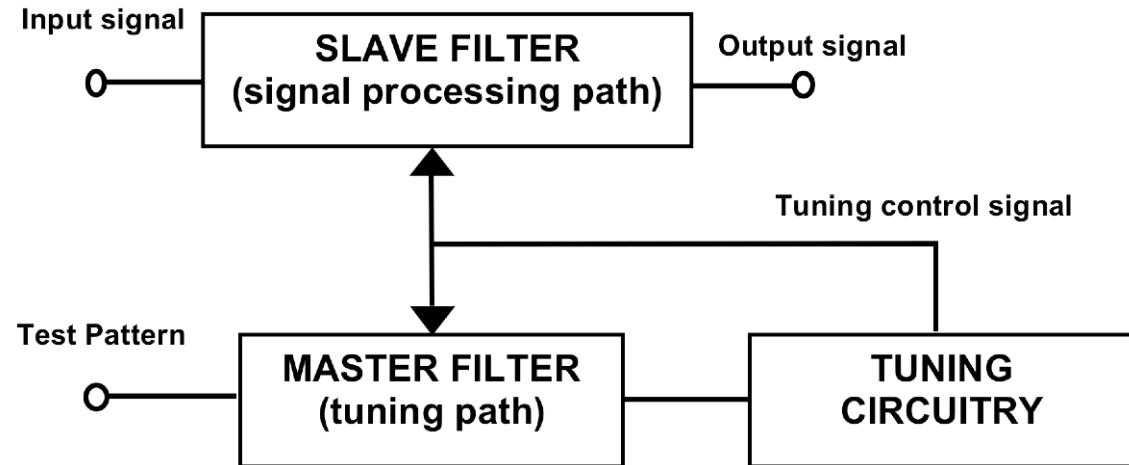
# Tuning systems

## Master-Slave approach

- The control signal of the time constant in the master circuit can be either

Analog

Digital



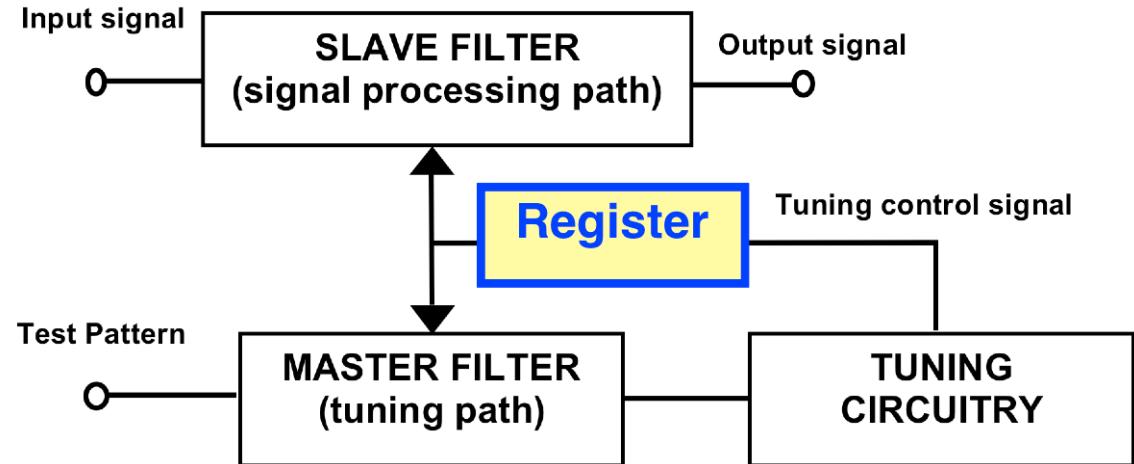
- An analog control signal allows a continuous control of the time constant with an analog control voltage  
This is the case of gm-C or MOSFET-C filters
  - large not-quantized accuracy
  - no distributed clock, etc.
  - the tuning system is continuously active (increasing the power consumption)  
since storing a high accuracy analog control voltage would be difficult



# Tuning systems

## Master-Slave approach

- A digital word is employed to switch on or off a set of analog unit element devices



- In active-RC filters, the value of the resistor and/or capacitor can be properly adjusted.
  - :( The accuracy of the tuning system is correlated to the quantization of the component whose value has to be adjusted.  
The number of bits of the control word corresponds to the achievable accuracy
  - : The control signal can be stored in a register  
→ the complete tuning circuit can be disabled during standard operation

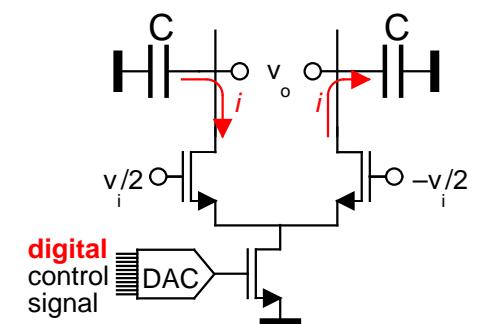
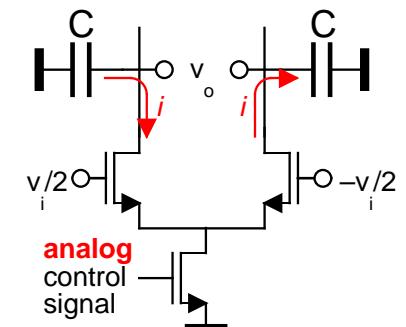
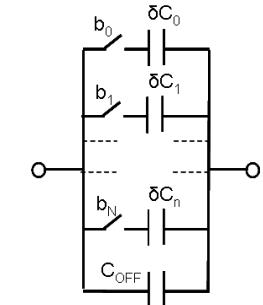


# Tuning systems

## Control signal vs. filter topology

- A CT filter can be tuned by a digital control of the capacitor
- A MOSFET-C or Gm-C filter requires an analog control signal

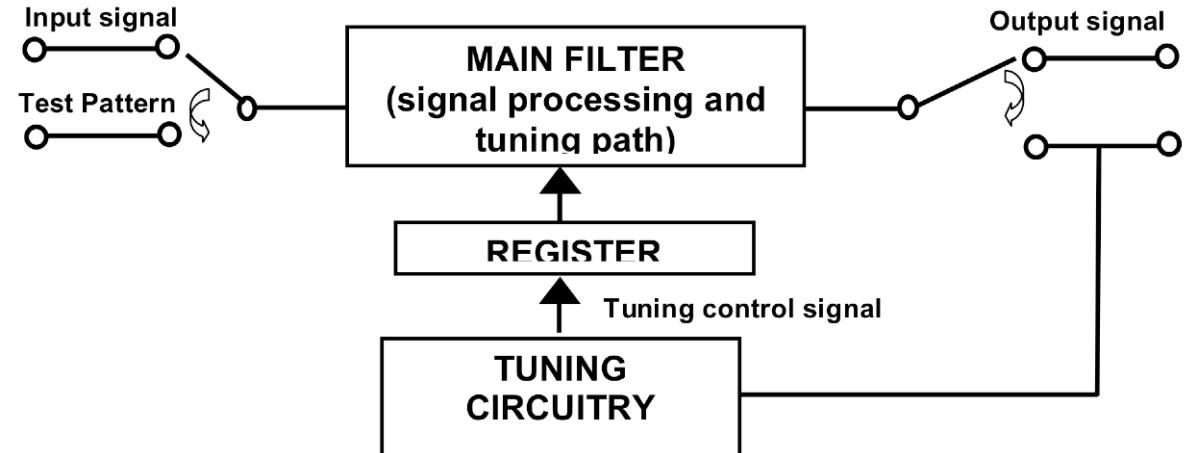
Using a digital control signal requires a DAC



# Tuning systems

## Self-calibration approach

- The transfer function of the main filter is directly controlled
- No matching problem

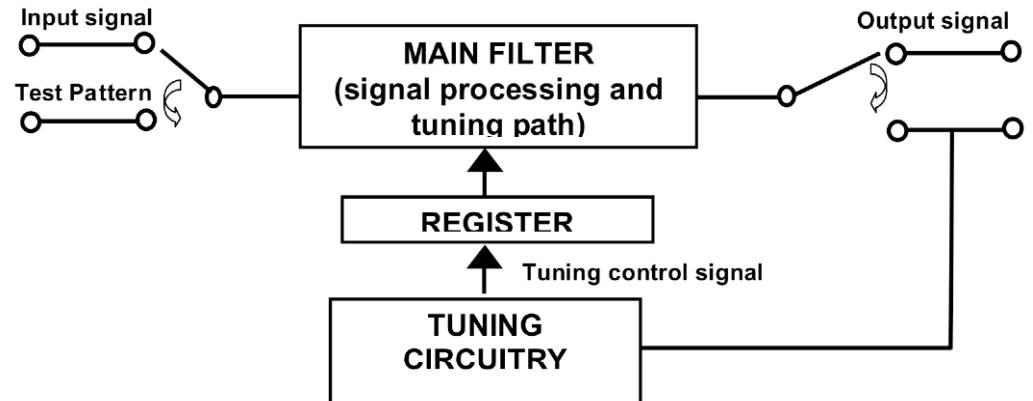
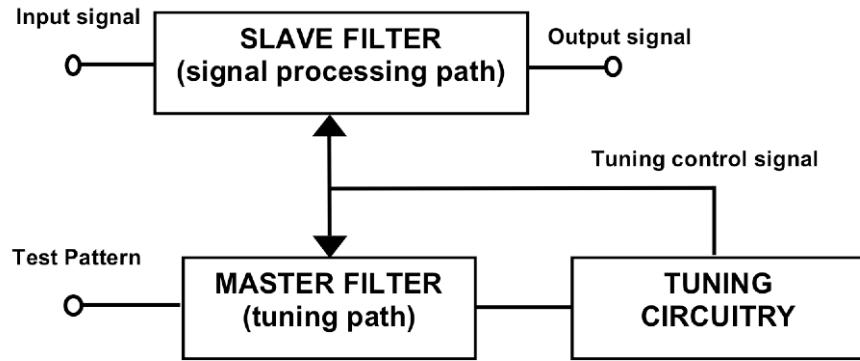


- The main filter can operate in two separate configurations:
  - Calibration      A test pattern signal is applied the output voltage is processed to elaborate the control signal  
The control signal is stored (better a digital value !!!)
  - Signal processing      The control signal adjusts the filter frequency response
    - ☺ Accuracy does not depend on the master-slave matching
    - ☹ A specific timing scheme is required
    - ☹ During calibration, the signal cannot be processed



# Tuning systems

## Key choices



- Several tuning algorithms are proposed in the literature
- The main parameters for their comparison are:
  - kind of input signal pattern and complexity of its generation circuitry
  - control of a single parameter of the frequency response (gain, pole frequency, etc.) or of the complete frequency response behavior
  - error detection circuit complexity and required accuracy
  - control algorithm circuit complexity and required accuracy



# Tuning systems

## Possible approaches

- Trimming + DC-tuning
- Switched-capacitor based
- Time-constant-locking
- Integrator-based tuning
- 1<sup>st</sup>-order filter based tuning
- Phase-Locked Filters & Oscillators



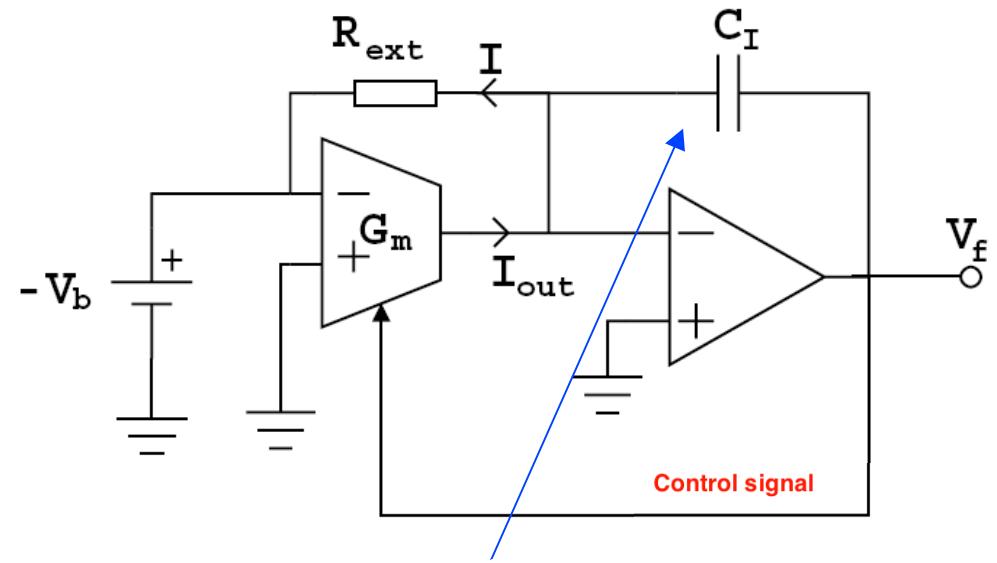
# Tuning systems

## Trimming + DC-tuning

- The capacitors are adjusted with a factory trimming
- The resistors are tuned with a control loop with an external resistor ( $R_{ext}$ )
- The control signal (analog or digital) is passed to the main filter
- In steady state

$$V_b / R_{ext} = I = I_{out} = V_b \cdot G_m$$

$$R_{ext} = 1/G_m$$



- 😊 Simple input pattern (dc-voltage)
- 😢 Factory trimming
- 😢 External resistor

- $C_I$  is filtering the error:  
Trade off: cap-size  
vs. settling time



# Tuning systems

## Switched-capacitor based

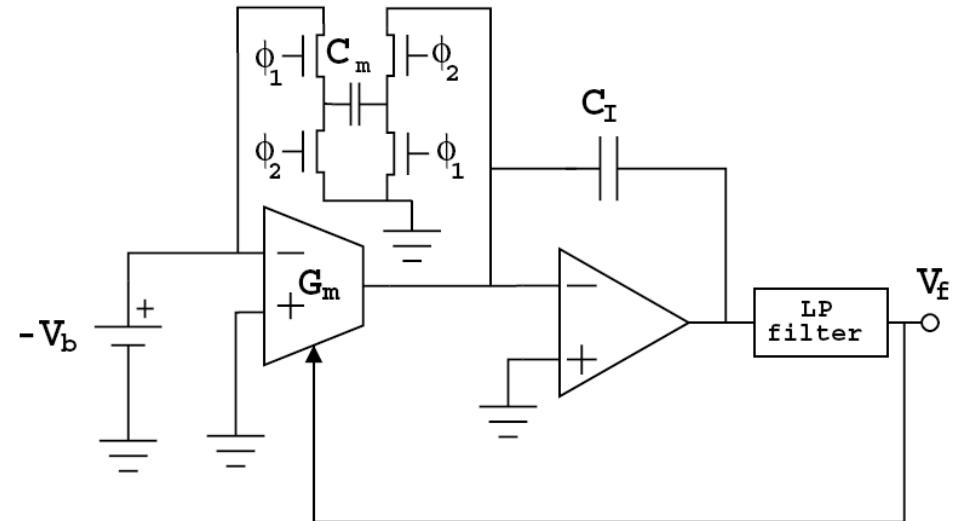
- In steady state

$$V_b / R_{SC} = I = I_{out} = V_b \cdot G_m$$

$$R_{SC} = 1 / (T_s \cdot C_m)$$

$$V_b \cdot T_s \cdot C_m = I = I_{out} = V_b \cdot G_m$$

$$T_s = C_m / G_m$$



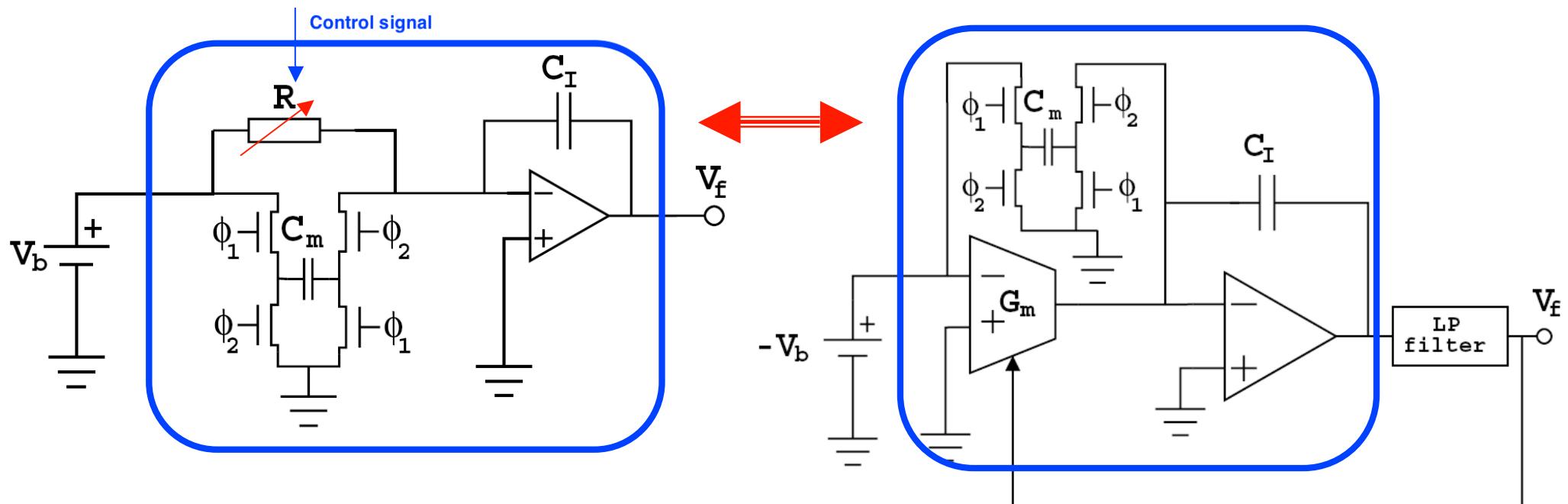
- The time constant  $C_m/G_m$  is correlated to the sampling period
- 😊 Simple input pattern (dc-voltage)
  - ☹ A clock signal is needed (😊 but it is available in the system – ex. ADC clock)
- 😊 No external components & no factory trimming
- ☹ Higher opamp bandwidth (it has to settle at any time slot)



# Tuning systems

## Switched-capacitor based

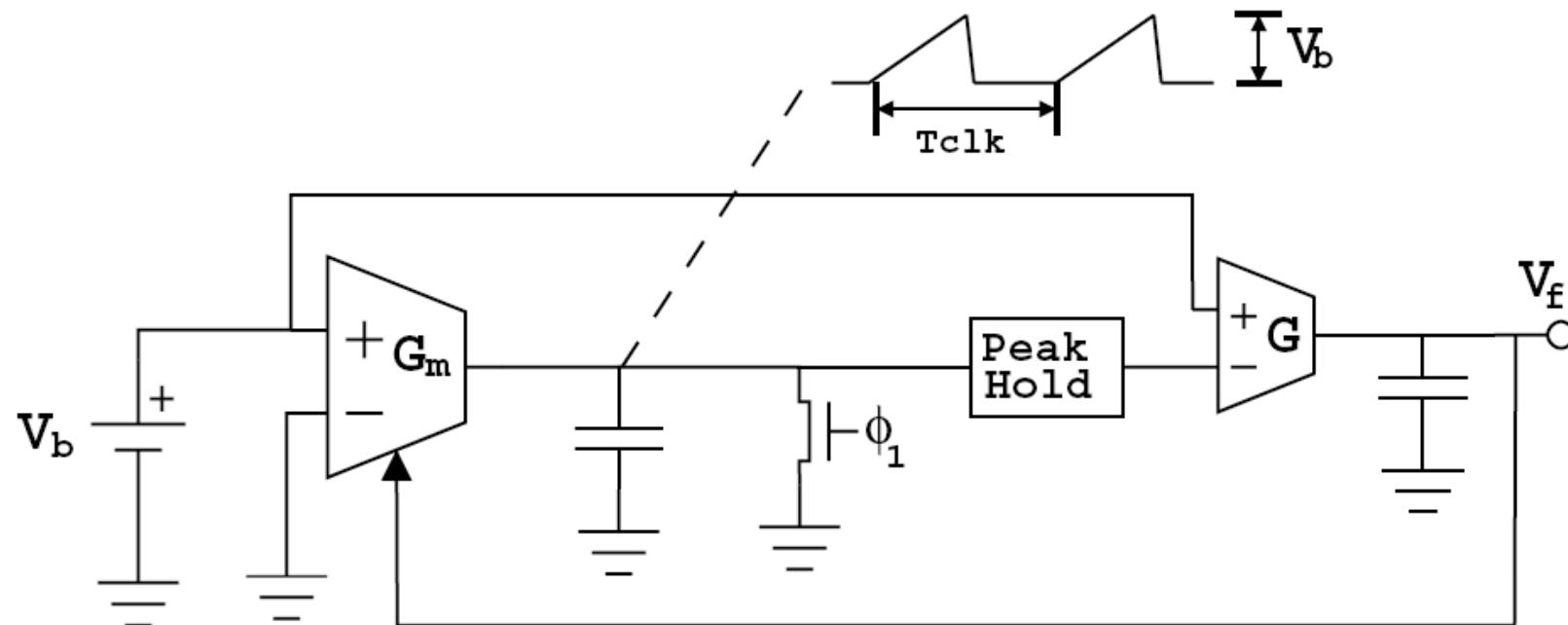
- The same concept can be done using an array of R
  - The control signal is digital



# Tuning systems

## Time-constant-locking

- The time-constant is locked to the reference clock
- Capacitor C is charged with a current given by the transconductor
- The peak reached during  $\frac{1}{2}$  clock cycle is compared to  $V_b$



# Tuning systems

## Integrator-based tuning

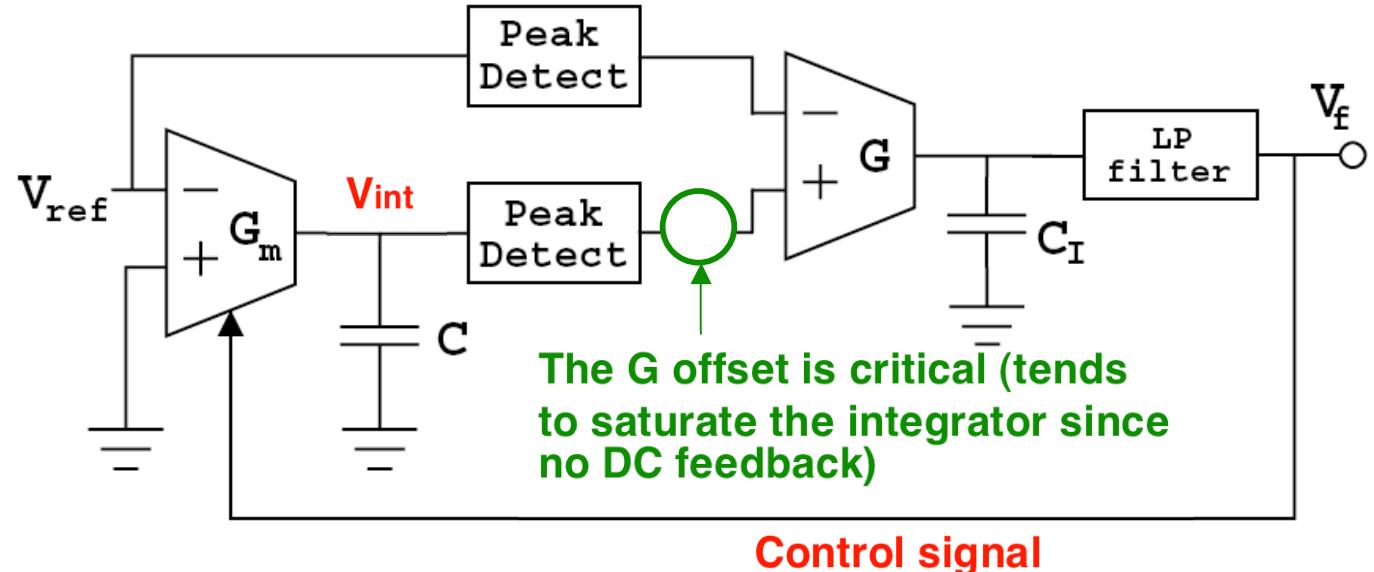
$$H(s) = G_m / (s \cdot C)$$

- Solving for  $|H(\omega)|=1$

$$\omega = G_m / C$$

- The integrator UG frequency is:

$$f_{UG} = G_m / (2 \cdot \pi \cdot C)$$



$V_{\text{ref}}$  is a “good” sinewave

$V_{\text{int}}$  is  $V_{\text{ref}}$  passed through the  $G_m$ - $C$  integrator

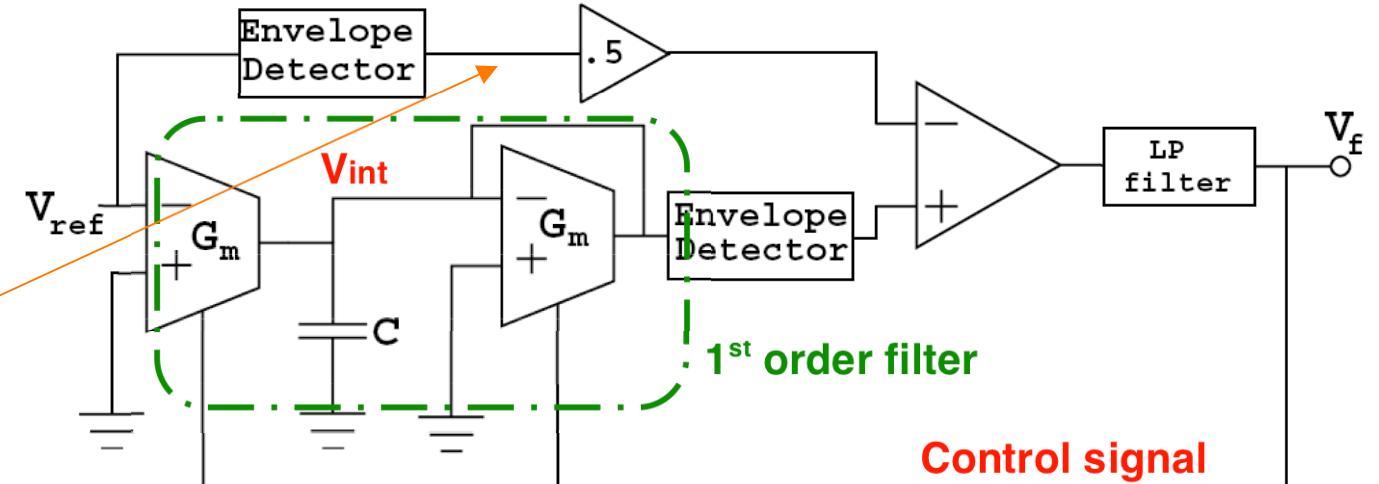
- $V_{\text{ref\_PEAK}}$  is compared to  $V_{\text{int\_PEAK}}$
- The loop with the  $G$ - $C_I$  integrator tends to have  $V_{\text{ref\_PEAK}}=V_{\text{int\_PEAK}}$  by changing  $G_m$   
This is obtained for  $G_m$  - $C$  at the  $V_{\text{ref}}$  frequency
- A non-ideal integrator causes  $\Delta f_o$  ( $A_o=40\text{dB}$  &  $\phi_{\text{err}}(@UG)<1^\circ \rightarrow \Delta f_o<0.1\%$ )



# Tuning systems

## 1<sup>st</sup>-order filter based tuning

- A 1<sup>st</sup> order filter is used
- The -3dB frequency is the target (this is the reason of the 0.5 gain loss)
- A DC feedback is present



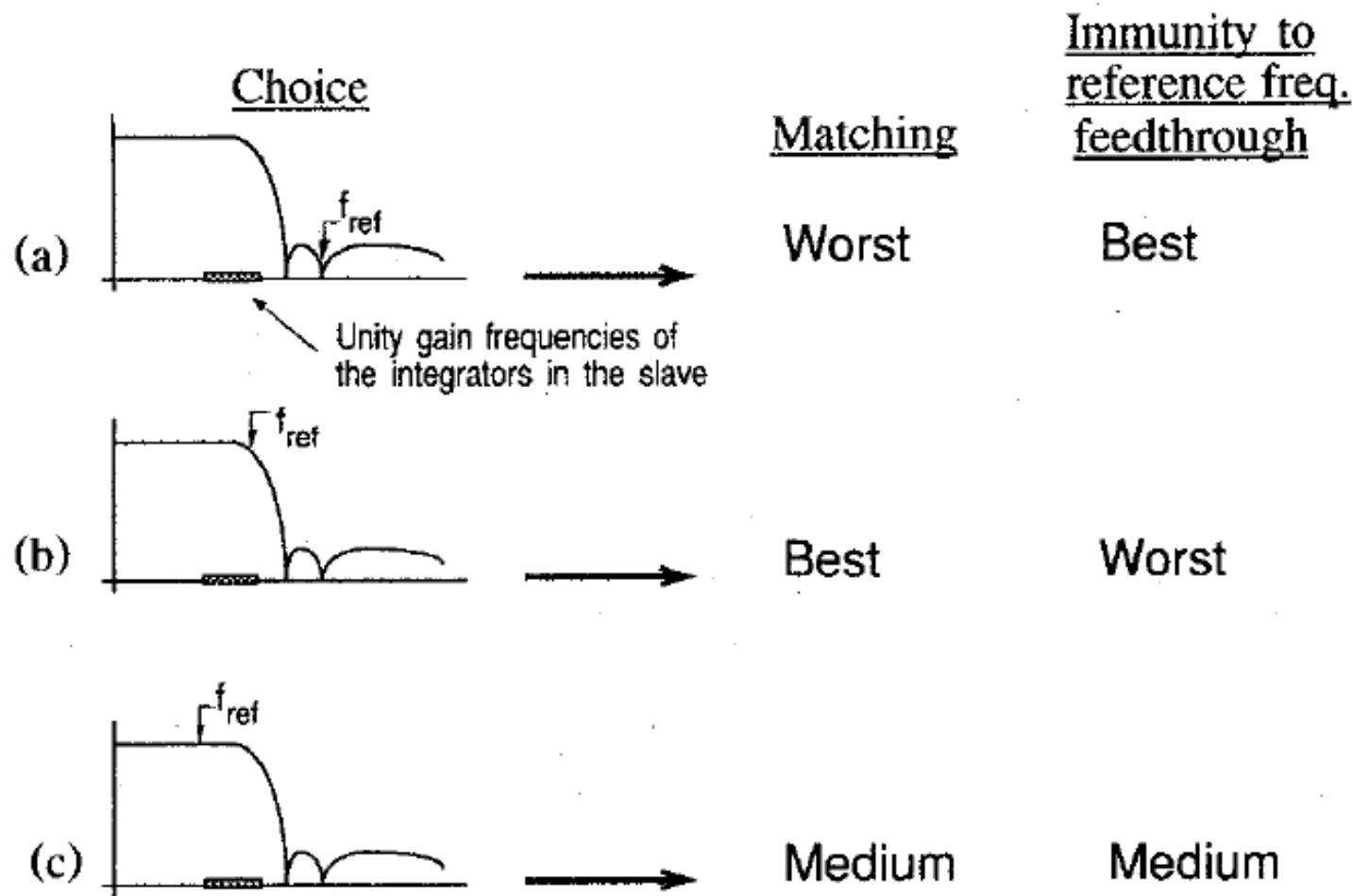
- The square of a signal with a relative amplitude of -3dB will result in an output DC-level of half that of a 0dB input signal.
- A peak-detector is on the other hand designed to preserve a linear relationship between input amplitude and the output voltage, and will thereby produce an output of  $\sqrt{1/2}$  times that of a 0dB signal.
  - When a ratio of the signals should be 3dB, implementing the attenuator after the squaring amplitude detector may improve accuracy, since it is usually easier to implement accurate integer ratios
- Design example: Chiang [ISCAS 2000], Lopez-Martinez [ISCAS 2001], Parker [JSSC 1995]



# Tuning Systems

## Optimum frequency choice

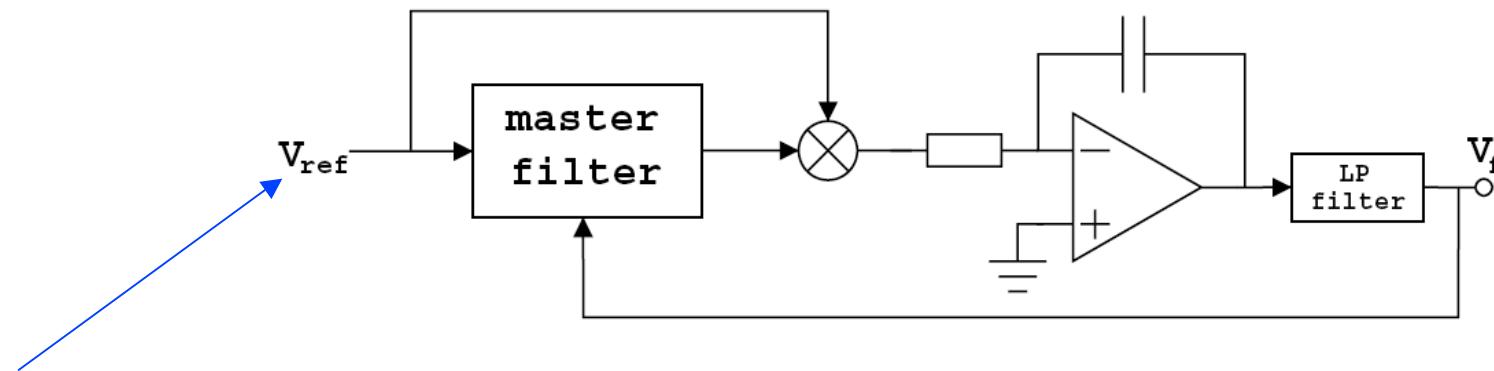
- Matching and main filter immunity has to be considered



# Tuning systems

## Phase-Locked Filters

- The main feature of this method is the good matching between master and slave to be obtain by realizing both filters with similar structures



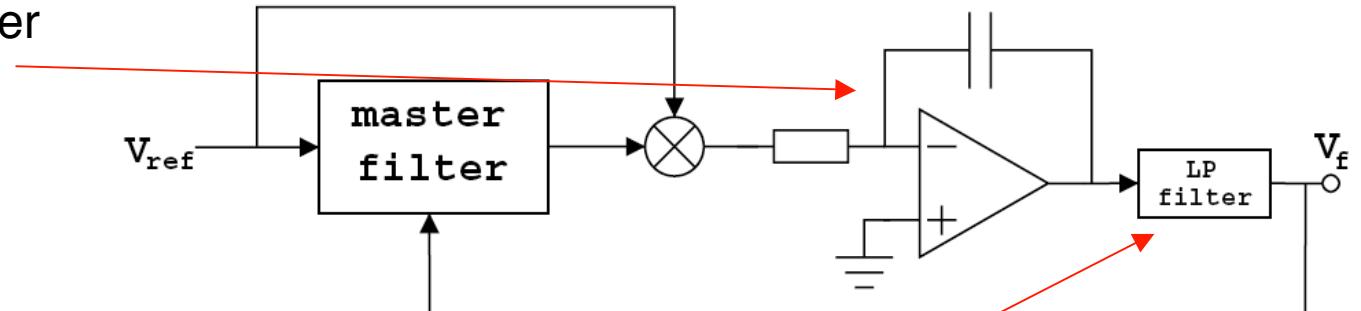
- A sine-wave reference-signal is used as input to the master filter.
- The phase of the filter output signal is compared with that of the reference signal
  - The phase comparison is carried out by multiplying the signals
  - The DC-component of the product of two signals with the same frequency depends on the phase difference
  - For a  $90^\circ$  phase difference the output will be zero



# Tuning systems

## Phase-Locked Filters

- The output from the multiplier is integrated over time,
- Voltage  $V_c$  is used as the frequency control signal



- This will effectively lock the phase-shift through the filter at 90°

A different phase shift produces a DC output to be integrated until the control signal has changed enough to correct the phase shift

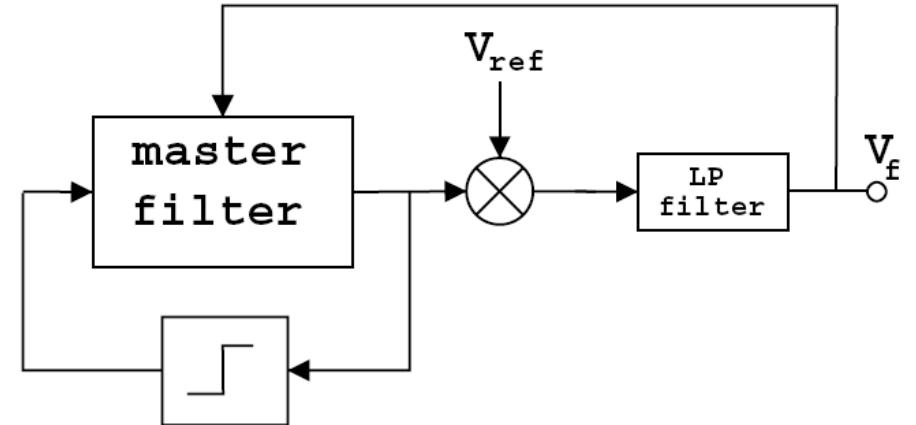
- A second order lowpass filter is usually used for the master filter, as it will have a 90° phase shift at its -3dB frequency.
  - This is true even when the slave filter is of a different type or order, because locking to a 90° difference usually simplifies design.
  - Higher order filters may have more than one frequency where the phase difference is 90°
    - → The tuning-circuit may converge to a wrong frequency
- Design examples: Khorramabadi [JSSC, 1984], Yoshizawa [JSSC, 2002]



# Tuning systems

## Phase-Locked Oscillators

- A phase-locking of an oscillator may be used
- To eliminate the need of:
  - a low-distortion sine wave reference-signal
  - the absolute accuracy of the phase-detector
- To guarantee that the circuit forms a stable oscillator with the active elements operating in their linear regions,
  - → new elements like nonlinear negative resistances, modified transconductors or limiters are usually required
- These changes reduce the master-slave matching w.r.t. a phase-locked filter
- Another approach is to try to keep a filter section oscillating by increasing the Q-value
  - This tends to cause a systematic frequency error



# Tuning systems

## Phase-Locked Oscillators

- An oscillator is formed by inserting a limiter in the feedback loop from the output to the input of a bandpass filter, which must have a passband gain larger than unity.
- The limiter will crop the peaks of the signal to some level
  - → the input signal amplitude is low enough for the filter to be sufficiently linear.
    - Too high input signal amplitude makes nonlinearities in the filter significant, with a change of oscillation frequency as a result.
- When the tuning is complete, the oscillator is phase-locked to the reference signal and any frequency error will make the phase error increase over time.
  - This in turn will change the DC-output from the phase-detector and adjust the control signals for the filter.
    - Since the phase error is the frequency error integrated over time, no stationary frequency error will remain
- Design examples: Banu [JSSC, 1985], Krummenacher [JSSC1988], Huang [JSSC 2001],

