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ZnO Nanofiber Thin-Film Transistors with Low-Operating Voltages

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Although significant progress has been made towards using ZnO nanofibers (NFs) in future high-performance and low-cost electronics, they still suffer from insufficient device performance caused by substantial surface roughness (i.e., irregularity) and granular structure of the obtained NFs. Here, a simple one-step electrospinning process (i.e., without hot-press) is presented to obtain controllable ZnO NF networks to achieve high-performance, large-scale, and low-operating-power thin-film transistors. By precisely manipulating annealing temperature during NF fabrication, their crystallinity, grain size distribution, surface morphology, and corresponding device performance can be regulated reliably for enhanced transistor performances. For the optimal annealing temperature of 500 °C, the device exhibits impressive electrical characteristics, including a small positive threshold voltage (V_{th}) of ≈0.9 V, a low leakage current of ≈10^{-12} A, and a superior on/off current ratio of ≈10^6, corresponding to one of the best-performed ZnO NF devices reported to date. When high-κ AlO_x thin films are employed as gate dielectrics, the source/drain voltage (V_{DS}) can be substantially reduced by 10× to a range of only 0–3 V, along with a 10× improvement in mobility to a respectable value of 0.2 $cm^2 V^{-1} s^{-1}$. These results indicate the potential of these nanofibers for use in next-generation low-power devices.

1. Introduction

In the past decade, thin-film transistors (TFTs) based on the unique 1D semiconductors as active device layers have been extensively investigated and explored for various technological applications in photodetectors, chemical and biological sensors, active matrix organic light emitting diodes, and so on.[1–7] Among these 1D nanomaterials, many novel synthesis techniques have then been developed, including chemical vapor deposition (CVD),[8–10] hydrothermal methods,[11–13] and template-assisted electrodeposition, etc;[14–16] however, all of these fabrication schemes come with different process-related disadvantages. For example, CVD has been widely employed for the growth of 1D semiconductor nanostructures,[17,18] in which this technique is still far from being compatible with the large-scale manufacturing platform due to the rather high fabricating cost, rigorous process control, low production throughput, and complicated subsequent device fabrication scheme.[9,19] Although hydrothermal methods are seem to be the simple process and capable to produce large amounts of 1D nanomaterials with the relatively low cost, they are challenging to precisely control the diameter, morphology, and crystal structure of the nanomaterials obtained, seriously influencing their chemical and physical properties, eventually limiting their practical utilizations.[13,20] In general, electrospinning is well accepted to its simplicity and versatility to yield organic, inorganic or composite nanofibers (NFs).[21,22] This technique can not only fabricate NFs with well-controlled properties, such as the excellent crystallinity, homogeneous chemical composition, and uniform diameters but also deliver the high throughput

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production of NFs, which illustrates promising perspectives of deploying electrospun NFs for next-generation high-performance electronic devices.

At the same time, owing to the superior electrical properties, chemical stability, and environmental friendliness, metal-oxide nanomaterials are usually considered as the ideal channel materials for TFTs.[23,24] In particular, In_2O_3 and ZnO have been the illustrating examples of high-performance metal-oxide nanomaterials as they consist of the relatively high electron mobility as well as the large bandgap for excellent transmittance in the visible region.[25] Nonetheless, the In-based metal oxides are not the ideal semiconductor materials for large-area integrated circuits because of the scarcity of In.[26–28] As a result, ZnO is usually adopted as the alternative "In-free" active material for metal-oxide-based electronic devices.[29–31] In this regard, the electrospun ZnO NFs have the great potential to satisfy all the stringent requirements for practical applications in large-area, low-cost, and high-performance integrated circuits. In any case, the current ZnO NF based TFTs, utilizing either single or multiple NFs as the channel materials, have the comparatively poor performance.[32–35] For instance, Belyaev et al. have fabricated the single ZnO NF device with the insufficient electrical performances, including the rather low field-effect mobility ($\approx 2.5 \times 10^{-6}$ cm^2 V^{-1} s^{-1}), saturation current ($<10^{-8}$ A), and I_{on}/I_{off} ($\approx 10^2$).[36] Also, Cadafalch Gazquez et al. have demonstrated the electrospun ZnO NF parallel arrayed TFTs with the inferior saturation current ($\approx 10^{-10}$ A) and I_{on}/I_{off} ($\approx 10^1$).[37] All these recent works have elucidated that the electrospun ZnO NFTFTs are still at their infancy stage and their electrical performance has to be further improved for the practical deployment. The unsatisfactory performance of these NF-based TFTs can be mainly attributed to the poor crystallinity of the ZnO channel obtained.[34] Moreover, the inherent surface roughness of ZnO nanomaterials (e.g., nanowires (NWs) and NFs) could also seriously modulate or even deteriorate their corresponding electrical properties.[38,39] It is found that the operation mode of ZnO NW TFTs can be reliably controlled by modifying their channels' surface morphology such that devices fabricated with smooth ZnO NWs yield depletion mode operation, while the ones associated with corrugated ZnO NWs exhibit the device operation in enhancement mode.[38] In addition, solution-processed metal-oxide semiconductors typically require a thermal annealing process to decompose the anion groups and generate bonds between the cations and oxygen atoms, which play a key role to enhance the crystallinity as well as to achieve the excellent chemical stability and physical properties. It is reported that binary polycrystalline metal oxides, such as In_2O_3, could exhibit the high electron mobility when they are annealed at a fairly high temperature.[40,41] On the other hand, the high-temperature annealing could as well give rise to the rough surface of NFs resulted from the overgrowth of nanoparticles, which significantly degrade their physical properties.[42] In this case, precisely adjusting the annealing temperature of the electrospun NFs can be considered as a simple and effective approach to control their surface morphology and crystallinity for the device performance enhancement, but few related studies are reported.

In this work, the electrospinning technique is utilized to synthesize large-scale and high-quality ZnO NFs. Zinc acetate salt is selected as the zinc precursor due to its relatively low decomposition temperature and high solubility, which is crucial to achieve superior electrical properties of the electrospun NFs. Since the nonuniform size distribution of nanograins existed within the ZnO NFs is found to yield poor electrical properties, such as the high off current, low saturation current, and reduced carrier mobility,[40,41] we systematically assess the effect of different annealing temperatures on the surface morphology, crystallinity, and electrical properties of the electrospun ZnO NFs. When the annealing is optimized at 500 °C, the fabricated NF device exhibits the respectable electrical performance with a low leakage current of $\approx 10^{12}$ A, which could have the superior pixel retention in display applications, a relatively high on/off current ratio of $\approx 10^6$, being highly preferred in electronic switching devices, and a small positive threshold voltage (V_{th}) of ≈0.9 V, that is attractive for the energy-efficient devices. With the aim to further decrease their operation voltages, solution-processed AlO_x thin film is also employed as the high-κ dielectric layer for the device construction and the corresponding operation voltage (e.g., source/drain voltage) can then be significantly reduced from 30 to 3 V. All these results indicate evidently the technological potency of our ZnO NFTFTs for the future high-performance, low-cost, large-area, and low-operating power electronics.

2. Results and Discussions

As shown in the scanning electron microscope (SEM) images in **Figure 1** and Figure S1 (Supporting Information), the as-spun ZnO NFs are randomly aligned on the receiver substrate as NF networks because of the bending instability of the whipping process. In specific, the NFs are first investigated with different annealing temperatures, ranging from 450 to 600 °C. Uniform and continuous ZnO NFs are obtained for the annealing temperature of between 450 and 550 °C. In this temperature range, when the temperature is increased, the NF surface becomes rougher, which would in principle act as the surface scattering site to disturb the carrier transport along the NF, reducing the carrier mean free time and mobility.[43,44] When the temperature is further increased to 600 °C, the NF would start to significantly overflow to give discrete and disconnected NF segments as marked in the region of yellow boxed in Figure 1c. Moreover, the zoom-in SEM is employed to evaluate the diameter and to verify the surface morphology of NFs annealed at different temperatures (Figure 1 and Figure S1, Supporting Information). Based on the statistics of more than 50 individual NFs for each sample group, the average diameters of NFs are observed to be 66.5 ± 4.2, 60.5 ± 5.0, 55.5 ± 3.5, and 58.5 ± 3.0 nm for the annealing temperatures of 450, 500, 550, and 600 °C, respectively (Figure 1f). This statistic demonstrates clearly that the diameter of ZnO NFs decreases as the annealing temperature increases, which is consistent to the results obtained from thermogravimetric analysis (TGA) curve presented in Figure S2 (Supporting Information), examining thermal properties of the starting ZnO precursor solutions. These trends of the diameter reduction and the surface roughness upturn for the increasing annealing temperature can be attributed to the degradation of organic residues decomposed from polyvinylpyrrolidone (PVP)

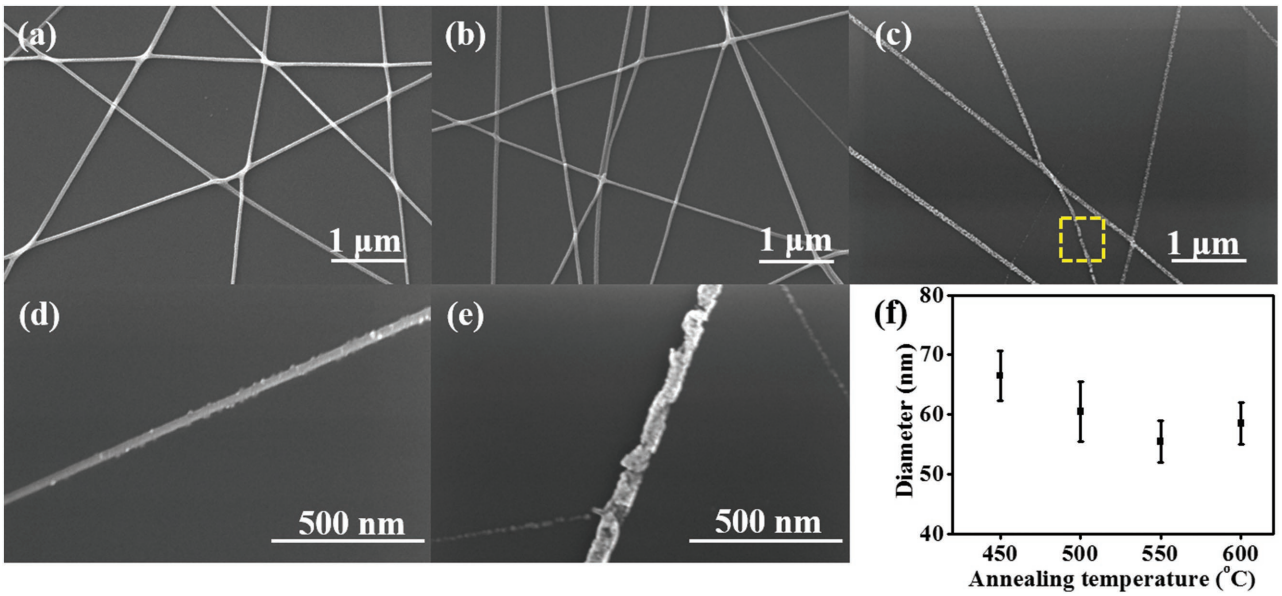


Figure 1. The SEM images of ZnO NFs annealed at different temperatures: a) 450 °C, b) 500 °C, and c) 600 °C (d) and (e) are the enlarged SEM images of a single NF corresponding to (b) and (c), respectively. f) Corresponding average diameter of ZnO NFs at different annealing temperatures.

and the enhanced diffusion rate of Zn atoms. Notably, there is a slight increase of the NF diameter at the temperature of 600 °C as compared with the one of 550 °C, which is probably caused by the dominating role of the nanocrystal growth along the NF. The reduction of nanofiber diameters from 450 to 550 °C is mostly due to the PVP degradation, while, for the nanofibers annealed at 600 °C, the increase of diameters is dominated by the grain growth. Based on the TGA analysis, the PVP precursor could not be completely decomposed at 450 °C or the lower temperature. This way, the residual carbon compounds would disorganize the Zn–O–Zn lattice, potentially acting as the electron transport channel even though the NFs have the smooth surface.[45] When the annealing temperature is increased to 600 °C, the organics within the NFs can be completely decomposed, whereas the ZnO nanoparticles would grow into large crystallites and eventually result into the discrete NF segments for the degraded electrical properties. It is obvious that the appropriate process window of the annealing temperature is narrow at ≈500 °C for the uniform diameter and continuous surface morphology. Besides, the diameter of nanofibers can also be precisely controlled by the distance between the needle tip and the collector, orifice size of the needle, and the electric potential applied between the needle tip and the collector. The density of the nanofibers can as well be regulated by controlling electrospinning time.

Next, X-ray diffusion (XRD) is performed to evaluate the crystallinity of ZnO NFs annealed with different temperatures as depicted in **Figure 2.** It is noted that when the NFs are annealed at 400 °C and higher, the XRD spectra exhibit nine distinct peaks at 31.75°, 34.41°, 36.23°, 47.51°, 56.57°, 62.84°, 66.36°, 67.93°, and 69.07°, corresponding to (100), (002), (101), (102), (110), (200), (112), and (201) lattice planes of ZnO (JCPDS, No. 80-0075), accordingly, which confirms the existence of crystalline ZnO NFs. There are not any impurities and secondary phases observed in the spectra, demonstrating the high purity of the products. With the increase of the annealing temperature, the diffraction peaks of ZnO NFs become sharper and more intense, which indicate the improvement of the crystallinity and the grain size of NFs obtained. Importantly, the grain size of ZnO nanoparticles existed in the NFs annealed at different temperatures can be assessed from XRD spectra by the Scherrer equation

$$D = \frac{K\lambda}{\beta \cos\theta} \tag{1}$$

where K is Scherrer constant, λ is the wavelength of X-rays, β is the full width of half-maximum of the diffraction peak, and

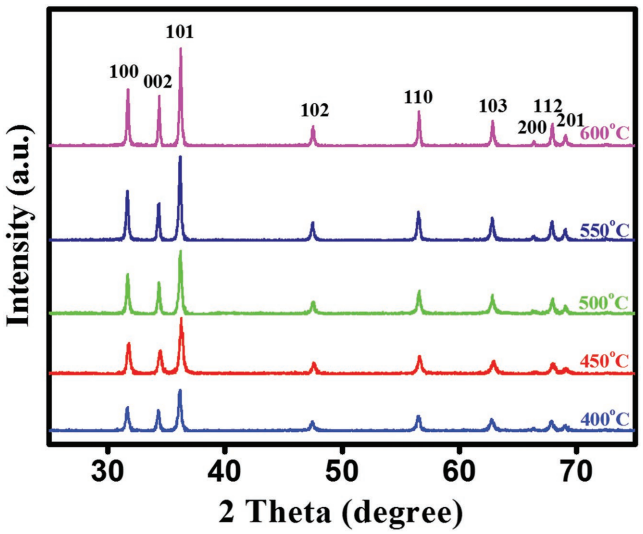


Figure 2. XRD profiles of ZnO NFs annealed at 400, 450, 500, 550, and 600 °C.

θ is the diffraction angle. This way, the grain size of ZnO nanoparticles can be determined as ≈15.3, ≈20.7, ≈24.7, and ≈32.4 nm with the annealing temperature of 450, 500, 550, and 600 °C, respectively. All these clearly illustrate the grain size getting larger with the increasing annealing temperature, which can be simply explained by the following Equation (2) correlating the relationship between growth speed of crystal grain and growth temperature

$$\upsilon = k\exp\left(-\frac{\Delta G^*}{RT}\right) \tag{2}$$

where υ is the growth speed of crystal grain, k and R are both constants, and ΔG^* is the growth activation energy which is an inherent material property. As ΔG^* is fixed, the growth speed υ follows the Arrhenius relationship of the growth temperature. Explicitly, the grain size would grow persistently with the increasing annealing temperature. As discussed above, when the gains grow too large, the NFs would have rough surface and become discrete NF segments giving rise to inferior electrical properties; hence, the high annealing temperature should be avoided. Similar phenomena has also been observed in other nanomaterial system, such as In_2O_3, even though the grain size existed in the electrospun ZnO NFs is larger than that of In_2O_3 NFs due to its enhanced diffusion of ZnO constituents at the same annealing temperature.[46]

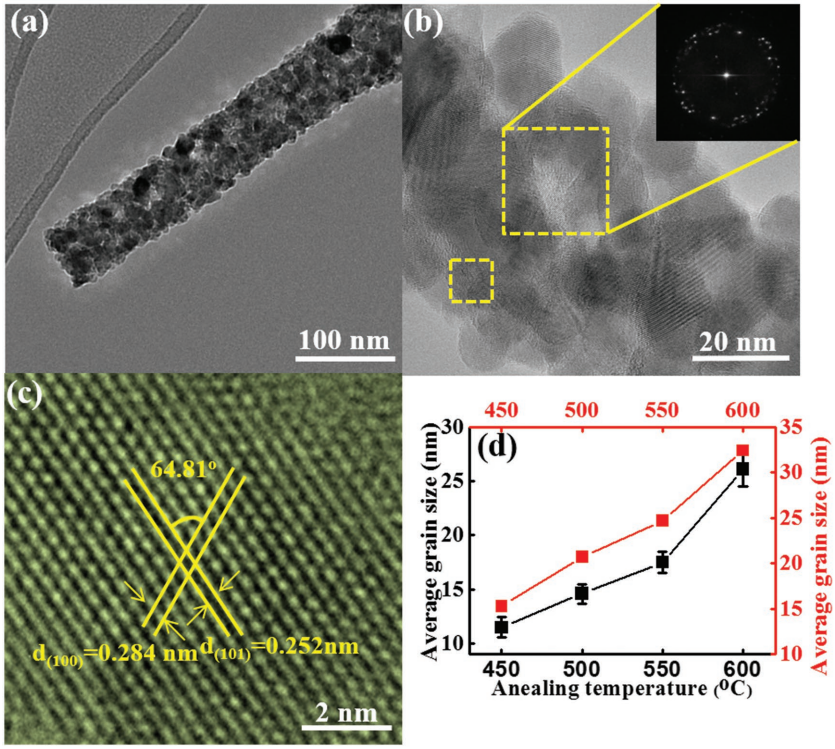
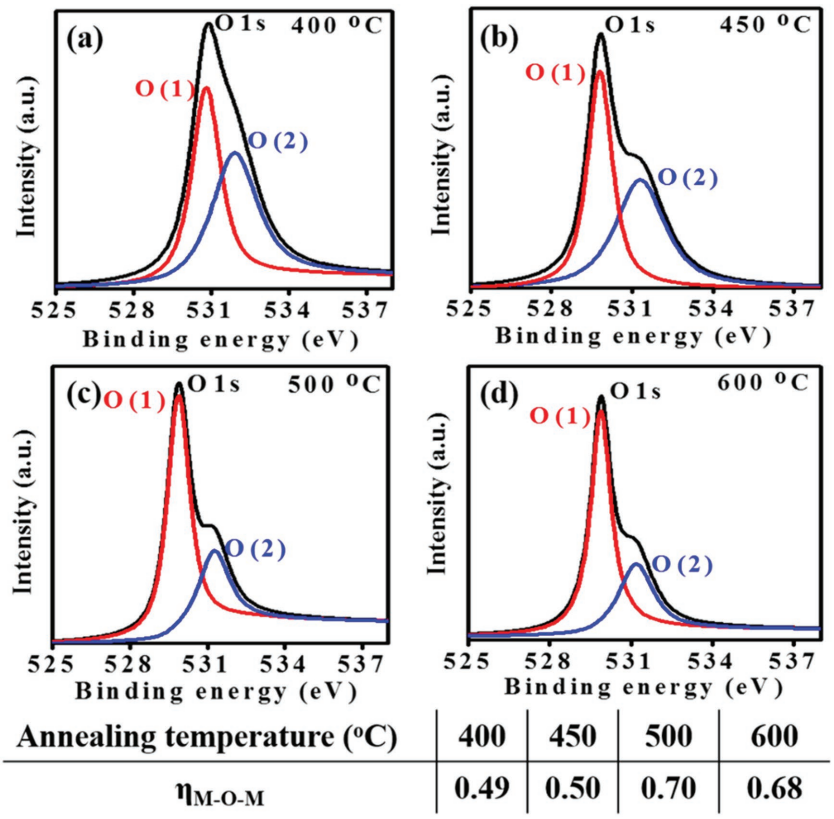


Figure 3. a) Bright-field TEM image of ZnO NFs. b) TEM image of single ZnO NF; the inset is the relative FFT pattern. c) HRTEM image of the area indicated by the yellow box in (b). d) The average grain size of ZnO nanoparticles composed in NFs annealed at different temperatures, where black points are measured from TEM images and red points are calculated from XRD spectra.

Apart from the crystallinity, it is also important to further understand the microstructure evolution of ZnO NFs annealed at various temperatures. As displayed in the high-resolution transmission electron microscope (HRTEM) images in **Figure 3** and Figure S3 (Supporting Information), when the annealing temperature is 500 °C, the NF is highly uniform in its diameter and is composed of nanograins exhibiting polycrystalline structure. The fast Fourier transform (FFT) image (Figure 3b inset) can confirm again the polycrystalline nature with the diffraction rings. Based on the HRTEM images, the average NF grain size can be determined as ≈11.5, ≈14.6, ≈17.5, and ≈26.1 nm for the annealing temperature of 450, 500, 550, and 600 °C, respectively, in which the trend is perfectly consistent to the one calculated from XRD spectrum (Figure 3d). Furthermore, the interplanar spacings of (101) and (100) are measured to be ≈0.252 and ≈0.284 nm, respectively, in Figure 3c, in which they are very close to the ideal interplanar spacing of cubic ZnO material (e.g., 0.248 nm for the (101) planes) as compared with the ones annealed at other temperatures, indicating the formation of stoichiometric and high-quality ZnO NFs annealed at 500 °C. It is also worth noting that the NFs annealed at ≈600 °C are broken into individual ZnO nanoparticles (Figure S3f, Supporting Information) during the preparation of TEM sample by ultrasonication, which further demonstrates the fragility of ZnO NFs processed at such high temperature.

In the meanwhile, X-ray photoelectron spectroscopy (XPS) is as well performed to better understand the local bonding differences among ZnO NFs fabricated with various annealing temperatures. As demonstrated in the typical XPS spectra of different ZnO NFs in **Figure 4**, the O 1s spectra can be deconvoluted into two principal signatures, namely the O (1) peak representing the M−O−M bonding located at 529.8 ± 0.1 eV, where M is the metal species, as well as the O (2) peak designating the surface metal hydroxide (M−OH) bonding and the weakly bound species (M−OR), such as CO_2 and H_2O located at 531.2 ± 0.1 eV.[47] As the annealing temperature increases from 400 to 500 °C, the intensity of O (1) peaks are obviously increased as compared with the ones of O (2) peaks. When the temperature is continued to increase to 600 °C, the corresponding intensity of O (1) peak is decreased slightly, which can be attributed to the fracture of NFs and reduction of the M–O–M lattice species. As the carrier transport is taken place in metal oxides highly dependent on the characteristics of M–O–M lattice, the quantity of M–O–M lattice (η_{M-O-M}) is a key parameter to describe their electronic transport properties. Specifically, η_{M-O-M} is defined as the sub-peak ratio of the M–O–M peak area to the total area of O1s peak following the Equation (3) below[44]

$$\eta_{M-O-M} = \frac{S_{M-O-M}}{S_{total}} \tag{3}$$



Annealing temperature (°C)	400	450	500	600
$\eta_{M\text{-}O\text{-}M}$	0.49	0.50	0.70	0.68

Figure 4. The XPS of ZnO NFs annealed at different temperatures: a) 400 °C, b) 450 °C, c) 500 °C, and d) 600 °C.

where $S_{M–O–M}$ is the area of the M–O–M peak and S_{total} is the total area of the O1s peak. The table in Figure 4 compiles the variation of $\eta_{M–O–M}$ values as the annealing temperature changes. For the annealing temperature at 500 °C, the $\eta_{M–O–M}$ value hits the highest point of 0.70, which can be deduced that the fabricated NFTFTs would exhibit the best electronic device performance (will be discussed in details in the next session). When the temperature further increases to 600 °C, the $\eta_{M–O–M}$ value decreases to some extent from 0.70 to 0.68, attributable to the fragmentation of the NFs. Overall, the $\eta_{M–O–M}$ values are extremely sensitive to the annealing temperature of ZnO NFs. Once the optimum annealing temperature of 500 °C is reached, the NFs are more favorable to form more M–O–M lattice species for the enhanced carrier transport.

In an effort to shed light on the influence of annealing temperatures on the electrical properties of NFs, numerous TFTs based on ZnO NF networks processed with different annealing temperatures are fabricated and characterized. **Figure 5**a demonstrates the SEM image of a representative ZnO NFTFT together with its schematic illustration configured in the global back-gated geometry. It should be noted that all devices are fabricated with the same process condition,

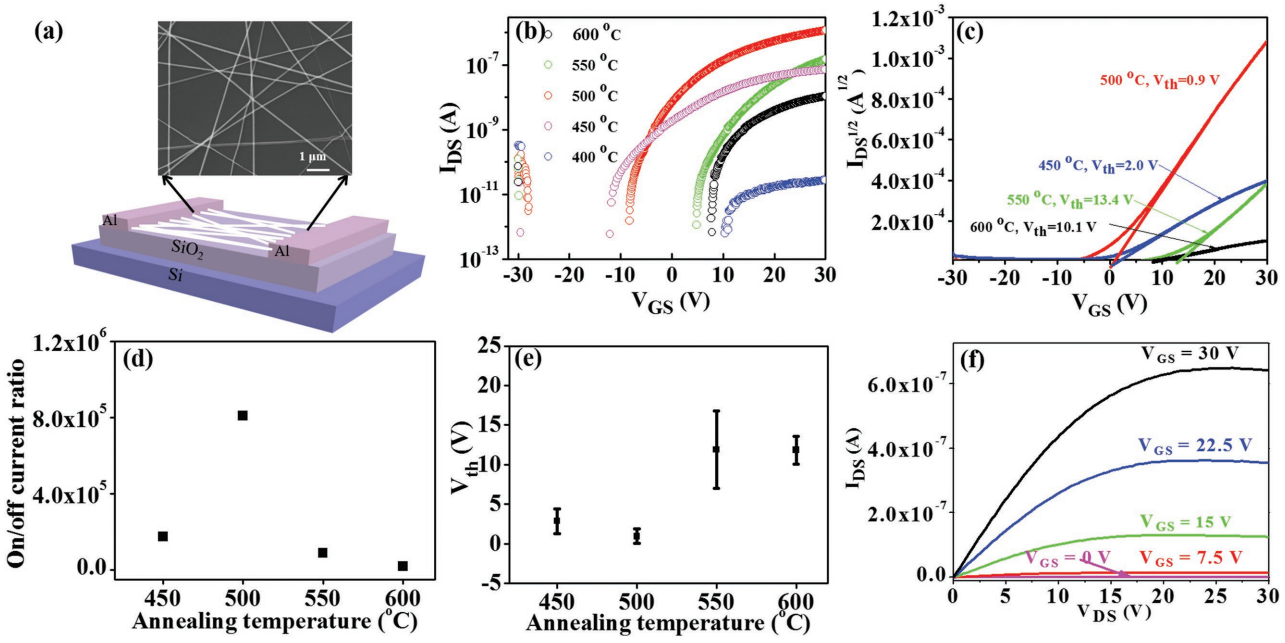


Figure 5. a) Top: SEM image and bottom: model of a typical back-gated ZnO NFTFT fabricated with Al electrodes and heavily doped silicon substrates covered with 300 nm thick SiO_2. b) The transfer curves, c) V_{th}, d) average on/off current ratio, and e) average V_{th} of ZnO NFTFTs annealed at different temperatures. f) The output curves of ZnO NFTFT annealed at 500 °C.

the identical device geometry (i.e., channel width and length of 1000 and 100 μm, respectively) and the similar NF network density, except for the annealing temperature. As we reported previously, too low or too high NF network density would influence their electrical properties.[46] In this work, the density of ZnO NF networks is controlled to ≈0.45 NF μm^{-1} with the electrospinning time of 30 s for all devices, in which this density is shown to exhibit the best electrical characteristics among all studied devices. Also, the same V_{GS} sweep rate is applied to ensure a consistent comparison among all devices characterized. Figure 5b demonstrates the corresponding transfer curves (I_{DS} versus V_{GS}) of ZnO NFTFTs using 300 nm thick SiO_2 as the dielectric layer, ZnO NF networks annealed from 400 to 600 °C as the active channel layer and the V_{DS} of 30 V. At the temperature of 400 °C, the NF device barely exhibits semiconductor properties. It could be deduced from TGA curves (Figure S2, Supporting Information) that there might be some amount of organic residuals existed in the NFs processed with low annealing temperatures, hindering the carrier transport. When the annealing temperature is increased from 450 to 600 °C, all the devices yield the intrinsic n-type conductivity, which could be mainly originated from the donor-like crystal defects, such as the O vacancies and/or Zn interstitials. As summarized in Table S1 (Supporting Information), the NF device performance is heavily depended on the annealing temperature. It is worth noting that all the devices annealed at various temperatures have relatively low off current, ranging from 10^{-13} to 10^{-11} A, which is advantageous for high-speed switching devices, high-performance UV detectors, and so on, while the saturation on current changes obviously with various temperatures. For example, the ZnO NF device processed at 500 °C has an on current of ≈1.3×10^{-6} A, nearly twenty times of the magnitude larger than the devices fabricated at 450 °C, which might be caused by the complete decomposition of PVP or its residual carbon compounds. Meanwhile, the on current decreases significantly after being annealed at 550 °C as compared with that annealed at 500 °C, attributable to the surface roughness resulting in a fluctuating shape along the radial direction and leading to surface scattering sites deteriorating the electron transport along the axial direction.[48] Also, the corresponding $\eta_{(M-O-M)}$ value would become smaller when the NF is annealed at 550 °C as compared with the one of 500 °C, therefore, the quantity of carrier propagation channels of ZnO NFs annealed at 550 °C is less than the ones annealed at 500 °C. In this case, when the annealing temperature is optimized at 500 °C, the NF device exhibits a considerable large on/off current ratio of ≈10^6, a relatively high electron mobility of ≈0.02 $cm^2\ V^{-1}\ s^{-1}$ and a comfortably small positive V_{th} of ≈0.9 V. Such a small positive V_{th} infers that the device can operate in enhancement mode yielding a zero current at the zero gate bias, indicating the reduced power consumption during practical utilizations. It is also noted that when the fibers are annealed at 450 °C, there is still a lot of organic residue left in the channel, deteriorating the corresponding gate coupling efficiency such that the on current is extremely low. Once the annealing temperature increases from 450 to 600 °C, the location of I_{off} exhibits a positive shift with the increasing annealing temperature. In specific, the I_{off} is located in negative V_{GS} at the annealing temperature of 450 °C while the corresponding V_{th} is extracted as 2.0 V from the $I_{DS}^{1/2}$ versus V_{GS} curves. This phenomenon can be attributed to the small SS value (0.31 V dec^{-1}). Moreover, the SS is generally related with defect states and their density. When the fibers are annealed at 450 and 500 °C, their enhanced smooth surface is anticipated to reduce the surface traps and the defect density, which results in the smaller SS values and increases the V_{th} values, transforming the device operation from depletion mode to enhancement mode. Therefore, the I_{off} locations are first existed at negative V_{GS} and changed according to the SS and V_{th} values. Conversely, when the fibers are annealed at 550 and 600 °C, the surface of nanofibers become rougher and even cracked, which would significantly hinder the gate coupling and transportation of carriers. This way, the corresponding V_{th} values and I_{off} location are eventually shifted to the large positive V_{GS}, accordingly. Here, the mobility is measured and extracted by Equation (4) in the Experimental Section and V_{th} is obtained in the saturation region through the maximum curvature of the $I_D^{1/2}$ versus V_{GS} plot. In order to fully identify the variation between annealing temperatures and device performance, 10 devices are compared and contrasted for the on/off current ratio, V_{th}, saturation on current and off current, corresponding to Figure 5d,e, and Figure S4 (Supporting Information), respectively. It is clear that the ZnO NFTFTs processed at 500 °C exhibit the best electrical performance. As depicted in the output characteristics (I_{DS} versus V_{DS} curves) of the optimized ZnO NFTFT in Figure 5f, it gives a typical n-type conducting and current saturation behaviors. In addition, at a small V_{DS} bias, the output current increases linearly with the V_{DS} bias, indicating the electrical contact between ZnO NF networks and Al electrodes is Ohmic-like here. More importantly, when our optimized ZnO NF devices are compared against recent state-of-the-art counterparts reported in the literature (**Table 1**), our devices can deliver the highest electron mobility

Table 1. A comparison of electrical properties of the electrospun ZnO NFTFTs.

Materials	Polarity	Source/drain	Substrate	μ_e or μ_h [$cm^2\ V^{-1}\ s^{-1}$]	Saturation current [A]	I_{on}/I_{off}	Year	Ref.
ZnO	n	copper wire/copper wire	SiO_2/Si	–	6×10^{-11}	10^3	2008	[33]
ZnO	n	Au/Au	SiO_2/Si	4.6×10^{-3}	10^{-9}	$<10^1$	2013	[34]
Ce-doped ZnO	P	An/Au	SiO_2/Si	–	10^{-8}	10^1	2014	[32]
La-doped ZnO	P	An/Au	SiO_2/Si	–	10^{-9}	$<10^1$	2015	[35]
Al-doped ZnO	n	Al/Al	SiO_2/Si	33×10^{-3}	10^{-8}	10^3	2016	[36]
ZnO	n	Ti-Au/Ti-Au	SiO_2/Si	0.018	≈nA	$<10^1$	2016	[37]
Our work	n	Al/Al	SiO_2/Si	0.02	1.26×10^{-6}	10^7	2017	–

of ≈0.02 cm^2 V^{-1} s^{-1}, the largest saturation on current of 10^{-6} A and maximum on/off current ratio of ≈10^6, representing one of the best ZnO NF devices investigated so far.

In order to further reduce the operation voltage (e.g., V_{DS} of 30 V) employed above and improve the device performance, solution processed AlO_x film is used as gate dielectric layer for the device construction. As compared with other solution-processed high-k dielectrics, AlO_x is adopted here due to its relatively large-area uniformity, high dielectric constant of 6.7, excellent surface smoothness with a roughness of below 0.2 nm and almost pinhole free characteristics (e.g., low leakage current density down to 1 nA cm^{-1} at 2 MV cm^{-1} and high breakdown electric field of greater than 5 MV cm^{-1}).[46] Importantly, this smooth surface can minimize the carrier scattering, being highly beneficial for the carrier mobility enhancement and improved device stability. **Figure 6**a gives the output curves of the optimized ZnO NFTFT using AlO_x dielectrics with the gate voltage (V_{GS}) stepping from 0 to 2 V in five steps, while Figure 6b illustrates the corresponding transfer curves with the V_{GS} sweeping from −1 to 3 V at a fixed scan rate and a V_{DS} = 3 V. All these indicate the minimized operating voltage achieved with the use of high-κ dielectrics of AlO_x. The V_{DS} of 3 V here is reduced by 10 times, exhibiting the same or even better device performances, as compared with the device based on SiO_2 dielectrics. Specifically, the device yields a V_{th} of ≈0.42 V, a field-effect mobility of ≈0.2 cm^2 V^{-1} s^{-1}, a saturation on current of ≈1.12×10^{-6} A, an off current of ≈4.32×10^{-13} A and an I_{on}/I_{off} of ≈2.56×10^6. This significant performance enhancement can be due to the better interface quality between ZnO NF and AlO_x dielectric with the reduced interface defects and minimized interface carrier scattering. Importantly, after sweeping the gate voltage for 50 cycles, the transfer characteristics do not change significantly even without any device passivation applied to the current device configuration. The slight V_{th} shift of 0.25 V can be probably related to the interaction between unpassivated NF and ambient environment. In the future, more detailed device stability measurement, including prolonged periods of electrical stress with operating gate biases, will be performed to assess the V_{th} shift and corresponding degradation mechanism. In any case, as shown in Figure 6d and Figure S5 (Supporting Information), the on/off current ratio, the saturation on current and the off current are all relatively stable after 50 cycles of the gate voltage sweeping. These negligible changes of all device parameters suggest strongly that the optimally annealed ZnO NFs are highly crystalline with minimized surface scattering for the enhanced electronic device performance and electrical stability, being the ideal active materials for the next-generation, large-scale, and low-operating power electronic devices.

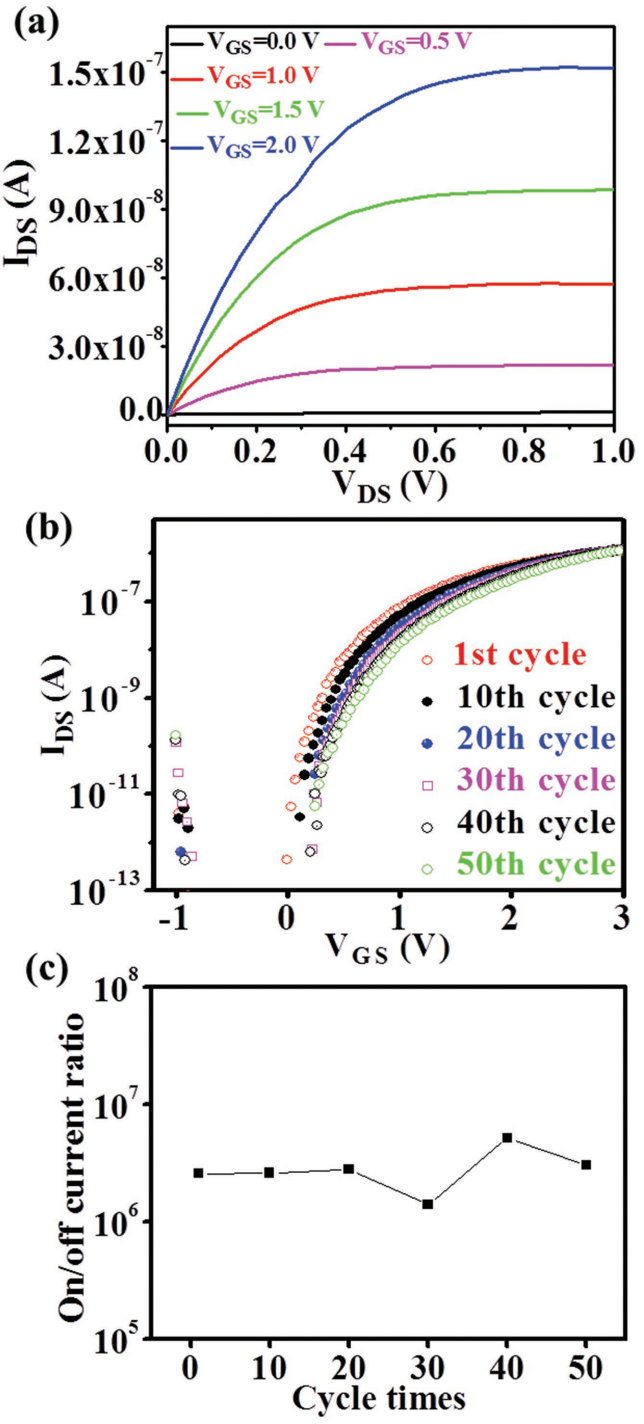


Figure 6. The electrical properties of ZnO NFTFTs fabricated by Al_2O_3 dielectric layer. a) Output curves, b) transfer curves at different cycle times, and c) the on/off current ratio corresponding to different cycle times.

3. Conclusions

In conclusion, high-performance and low-operating power field-effect transistors based on ZnO NF networks are demonstrated with the simple one-step electrospinning method. It is found that the crystallinity, the surface morphology, and the electrical properties of NF can be simply and reliably controlled by the annealing temperature during the fiber spinning. As compared with other state-of-the-art ZnO NF devices, our optimized device exhibits one of the best NF device performance up to now, including a high saturation on current of ≈1.26×10^{-6} A, a low off current of ≈1.54×10^{-12} A, and a respectable field-effect electron mobility of ≈0.04 cm^2 V^{-1} s^{-1},

a small positive V_{th} of ≈0.9 V as well as a high I_{on}/I_{off} of ≈10^6. In order to further decrease the operation voltage and enhance the device characteristics, high-κ dielectric of solution processed AlO_x thin films, instead of the conventional SiO_2 dielectrics, are employed for the device construction, in which the source/drain voltage can be substantially reduced by 10 times to a range of only 0 to 3 V. Also, the electron mobility can be improved by 10 times to the value of 0.2 $cm^2\ V^{-1}\ s^{-1}$. Importantly, all device parameters do not change significantly after 50 cycles of gate voltage sweeping, indicating the electrical stability contributed by the enhanced ZnO nanofiber device channel. All these findings reveal explicitly that the optimally annealed electrospun ZnO NFs consist of the promising potential for the high-performance, large-scale, and low-operating power electronics, such as photodetectors, gas sensor arrays, and display applications.

4. Experimental Section

Preparation of the Electrospinning Precursor: The ZnO electrospinning precursor solution was prepared by dissolving of 0.3 g zinc acetate dihydrate ($Zn(C_2H_5O_2)_2{\bullet}2H_2O$, Aladdin, 99.9%) and 0.8 g PVP (Aladdin, K88-96) into 5 g *N*,*N*-dimethylformamide (DMF, Aladdin, AR, 99.5%). Then, the above precursor solution was stirred for 5 h at room temperature (≈25 °C).

Solution Processed AlO_x Thin Film Fabrication: The AlO_x precursor solution was prepared by dissolving of 0.1 M aluminum nitrate nonahydrate ($Al(NO_3)_3{\bullet}9H_2O$, 99.99%, Aladdin) in 9.4 g DMF (Aladdin, AR, 99.5%) which worked as solvent. The above solution was then stirred at room temperature for 12 h and then kept standing for another 12 h to get clear and uniform solution. After that, a p-type heavily doped Si wafer (1 cm × 1 cm) with clean surface was treated with oxygen plasma for 5 min to enhance its surface hydrophilicity. Before spin coating, the AlO_x precursor solution was filtered by 0.22 µm polytetrafluoroethylene syringe filter. The prepared solution was spun coated onto the processed Si wafer at a fixed speed of 5000 rpm for 12 s. After that, the wafer was placed on a hot plate and baked at 150 °C for 10 min. The AlO_x thin film was then pretreated by using a high-pressure mercury UV lamp for 30 min to decompose the nitrate anion in the precursor solution into oxygen and nitrogen dioxide radicals in order to enhance the interface properties and surface morphologies of the deposited film.[46] Finally, the above AlO_x solvent film was further annealed at 700 °C in the air for 3 h to obtain the dense and smooth AlO_x thin film with the surface roughness of less than 0.2 nm.[46]

Electrospinning Process and ZnO NF Characterization: Figure S6 (Supporting Information) demonstrates the electrospinning procedure for the ZnO NF fabrication. The uniform precursor solution was put into a syringe which has a stainless steel needle with a ≈0.5 mm inner diameter. The horizontal distance between the stainless steel needle and grounded substrate was kept for 12 cm. The positive accelerating voltage of 15 kV was applied between the needle and the collector, injection rate was set as 0.5 mL h^{-1}, and the NFs were obtained on the collector substrate with a proper spinning time of 30 s. After that, the as-spun composite fiber networks were baked at 150 °C for 10 min. In order to improve the adhesion strength between the NFs and the substrate, which can significantly influence the device performance, the prepared ZnO/PVP NFs are processed with UV-assisted irradiation for 40 min before calcinations. The UV lamp power is 1 kW and the wavelengths of the lamp are 290–320 nm. Such UV treatment can facilitate the strong photochemical activation of electrospun nanofibers in order to obtain the stable adherent nanofiber network and electronic clean interface.[46] All the above mentioned experimental processes were conducted at the room temperature with a relative humidity of 30–50%. In order to remove residual organics and to form crystalline ZnO NFs, NFs were further annealed at various temperatures (≈400, 450, 500, 550, and 600 °C, respectively) for 2 h in the air. Finally, ZnO NFs were obtained on the SiO_2 (≈300 nm thickness) and high-*k* AlO_x dielectric layer, respectively.

The density and surface morphology of ZnO NFs were investigated by SEM (JEOL JSM-7800F). In order to analyze the thermal behavior of ZnO precursor solution, TGA (Mettler Toledo TGA-2) was conducted with a heating rate of 10 °C min^{-1} ramping from 30 to 800 °C. The crystal structure of ZnO NFs was analyzed by XRD (Rigaku D/max-rB), TEM (JEOL JEM-2100), and HRTEM (JEOL JEM-2100). The chemical compositions were measured by XPS (ESCALAB 250). For the TEM sample preparation, ZnO NFs after annealed at various temperatures are ultrasonically suspended into anhydrous ethanol solution, and then drop-casted onto copper grids.

ZnO NF Device Fabrication and Characterization: As shown in Figure S6d (Supporting Information), for preparing source and drain electrodes, Al electrodes were thermally evaporated onto the NF active layer using a shadow mask with the channel width and length of 1000 and 100 µm, accordingly. The electrical properties of prepared NFTFTs were measured under ambient conditions by a semiconductor parameter analyzer (Keithley 2634B). The NFTFT mobility was measured and extracted by the following equation

$$I_{DS} = \left(\frac{WC_i\mu_{FE}}{2L}\right)/(V_G - V_{th}) \quad (4)$$

where C_i is the areal capacitance of the dielectric layer, W/L is the ratio of channel width to channel length of NFTFT, V_G is the gate voltage, and V_{th} is the threshold voltage, which can be obtained in the saturation region through the maximum curvature of the $I_D^{1/2}$ versus V_G plot.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

annealing, electrospinning, low-operating voltage, transistor, ZnO nanofiber

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