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Floating Gate Memory-based Monolayer MoS_2 Transistor with Metal Nanocrystals Embedded in the Gate Dielectrics

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In recent years, two dimensional (2D) layered materials such as graphene have received considerable attention for their atomic thickness, unique structure and special electrical characteristics.[1–4] However, the zero bandgap character has greatly limited its applications for graphene based switching circuits[2,5] and nonvolatile memory cells, in which the clearly defined on-and-off or program-and-erase states are essential. As compared with graphene, Monolayer MoS_2 has its natural advantages with a direct band gap of 1.8 eV and thus allows the fabrication of transistors with on/off ratio over 10^8.[6,7] Like graphene, monolayer MoS_2 can be readily obtained by the mechanical cleavage technique, chemical vapor deposition or lithium intercalation method for its excellent mechanical strength and weak inter-layer Van der Waal's force.[7] Also, various MoS_2 based electronic components have been recently demonstrated, such as small-signal amplifier, logic circuits, nonvolatile memory cells, etc., which further illustrate its great potential in numerous future electronic applications.[8–16]

As an essential part of electronics, nonvolatile memory cells have been heavily deployed in portable devices to achieve secure and fast data storage, such as the floating gate memory, which was first reported by Kahng and Sze in 1967.[17–21] Since then, the development of very large-scale integration has driven all components to scale in both lateral and vertical dimensions for the higher packing density, reduced energy consumption and minimized short-channel effect, which presents one of the ultimate challenges here. Generally, crystalline silicon is the dominant channel material used in the memory industry. As compared with silicon, monolayer MoS_2 has a relatively small dielectric constant ($\varepsilon = 7$) and atomic thickness, both of which can easily enable ultrathin-body MOSFETs to suppress the short channel effect.[23] Also, its comparably large device on/off ratio can facilitate the clear distinguishment between different memory states, being advantageous even for the multi-level data storage.[14,24] Although the relative high mobility of over 600 $cm^2V^{-1}s^{-1}$ reported previously is mainly caused by the coupling of the back- and top-gate,[22] a high mobility over 40 $cm^2V^{-1}s^{-1}$ of field effect transistors based on hBN-graphene heterostructures, which is comparable to that of crystalline silicon, was reported recently.[16] All these performance enhancement can lead to the achievement of highly efficient MoS_2 based energy-saving and low-operating-power electronics, satisfying all the stringent requirement for the future development of nonvolatile memory devices.

Although the natural advantages of MoS_2 make it a promising candidate for future memory device channel materials, the lack of an effective charge trapping layer still remains a substantial problem. Also, decreasing tolerance for charge loss caused by the defects in the tunneling oxide and increasing cell-to-cell interference would seriously limit the scaling, which is of significance for the high density storage and low power consumption.[19,21] This way, nonvolatile memory cells based on MoS_2/graphene heterostructures were fabricated lately to tackle this issue.[12,15] Employing this heterostructure, the capacitive interference between neighboring cells as well as the coupling between the electrodes and the floating gate can be significantly diminished through the minimization of the floating gate thickness.[12,15,23] However, this sophisticated fabrication process would make it difficult for the commercial large-scale production. Moreover, the trap level and charge distribution are difficult to be controlled for the entire graphene layer and the tolerance for charge loss caused by defects in the oxide is still unresolved. Lots of work has been done to find the suitable charge trapping layer for MoS_2 based memory cells. For example, multibit data storage with charge trapping sites formed in plasma treated MoS_2 has been reported recently with long retention time.[14] This easy fabrication process is unique and low cost; however, the plasma treatment may inevitably damage the surface of MoS_2, making the on-state current decrease significantly and resulting in a relatively small program/erase ratio. On the other hand, discrete charge trapping layers such as metallic nanocrystals are founded to have lower power consumption and better tolerance for charge loss.[19,25–33] By

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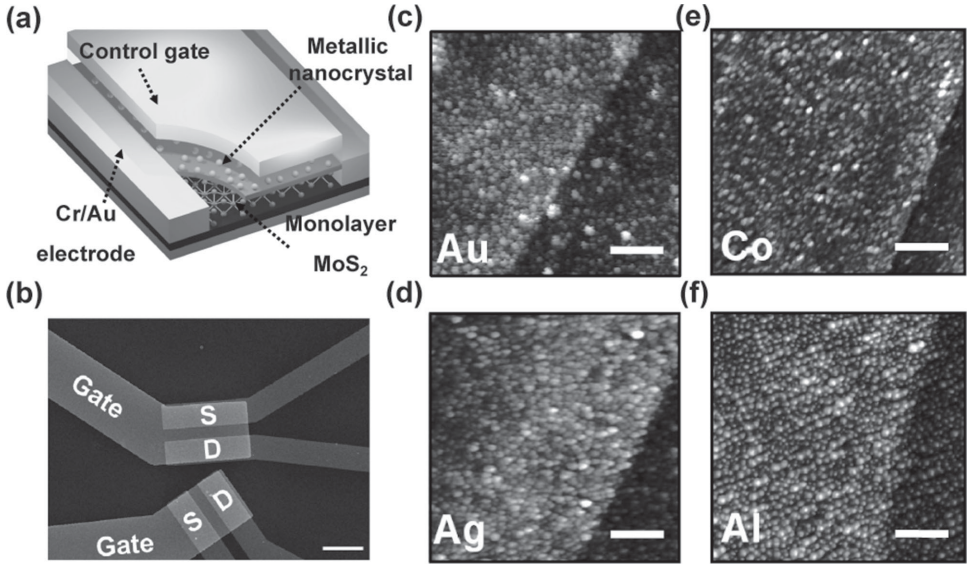

Figure 1. Structure of the MoS_2 based metallic nanocrystal floating gate memory cells. (a) Three-dimensional view of the structure of the metallic nanocrystal floating gate memory cell. (b) SEM image of the memory cell. The channel length is 1.5 μm and the scale bar is 5 μm. (c-f) AFM images of various nanoscrystals deposited onto the single layer MoS_2, pre-deposited with a 6.5 nm thick of HfO_2. All the scan size is 500 × 500 nm, the scale bar is 100 nm.

choosing the appropriate metal and grain size, the trap density and distribution can be effectively controlled, which are important to the enhancement of electron retention time.[34] More importantly, the deposition of metallic nanocrystals does not conflict with the fabrication of conventional floating gate memory cell and this easy processing makes it easily adaptable for future memory devices.[25] In this regard, here, the atomically thick MoS_2 channel and nanocrystal floating gate are employed together for the fabrication of nonvolatile memory cells. Specifically, four different metallic nanocrystal floating gates are utilized as the charge trapping layer and the memory cells with Au nanocrystals exhibit impressive performance with a large memory window of 10 V, a high program/erase ratio of approximately 10^5 and a long retention time of 10 years. All these evidently hold the promise of MoS_2 based metallic nanocrystal floating gate memory for the future nonvolatile data storage.

Figure 1a shows the device structure of the memory cell and Figure 1b gives the representative scanning electron microscope (SEM) image (Raman spectra is given in Figure S1 in Supporting Information). Monolayer MoS_2 is exfoliated onto a 288 nm thick thermally grown SiO_2 layer. Cr/Au is used as the source/drain electrodes and the channel length is 1.5 μm. The tunneling oxide is 6.5 nm thick HfO_2 deposited by atom layer deposition (ALD) under 90 °C. For the lack of dangling bonds on the surface of MoS_2, we deposit 1 nm thick Al as the seeding layer before the ALD process in order to initiate a uniform deposition. The charge trapping layer is then deposited by the thermal deposition of metallic nanocrystals with different work functions (Au~5.4 eV, Co~5.0 eV, Ag~4.4 eV, Al~4.2 eV)[35] under 6×10^{-4} Pa. Notably, semiconductor nanocrystals are not a good choice for the trapping layer here because they can only store a few electrons in each nanocrystal as a result of the Coulumb blockade effect, yielding a smaller memory window.[19,36] Finally, 20 nm thick HfO_2 is deposited onto the entire surface as the blocking oxide followed by the deposition of Cr/Au (10/30 nm) as the control gate. The 1 nm thick metal layer is deposited to form isolated islands or nanocrystals as the floating gate. Atom force microscope (AFM) images of the deposited metallic nanocrystals are given in Figure 1c-d. As shown in the images, the corresponding metal grains are close, compact and well uniform in size. In specific, the Au/Co/Ag nanocrystals show a similar grain size of 3–5 nm while the Al one presents the size of 4–8 nm with the details given in Supporting Information Figure S2.

Figure 2 shows the band diagram of the memory cell in the flat band state (Figure 2a) and operation state (Figure 2b-e). The work function of MoS_2 is 4.6–4.9 eV[32,33] and the electron affinity of HfO_2 is 2.11–2.17 eV. The barrier height for electrons to tunnel through the tunneling oxide is 2.5–2.8 eV. To simplify the band diagram, Fermi level shift caused by the carrier density is not taken into consideration. In view of the 6.5 nm thick HfO_2, electrons can tunnel through the tunneling oxide via the mechanism of Fowler-Nordeim tunneling. In general, there are two distinct states, namely program and erase, for the floating gate memory cell, which is purely dictated by the drain-to-source (I_{ds}) current.[19] When a suitable control gate voltage (V_{cg}) is applied, the charge stored in the floating gate will shift the threshold voltage (V_{th}) and change the I_{ds}. In the consideration of energy saving and device stability, the proper read voltage is usually set to be 0 V. In the erase state, there is no charge stored in the floating gate, the channel allows a high I_{ds} current when applied the read V_{cg} (0 V). Once a positive V_{cg} is applied, the energy band slope of the tunneling oxide layer raises and the barrier becomes very thin; therefore, electrons can then tunnel through the HfO_2 oxide from the conduction band of MoS_2 to the floating gate as a result of the Fowler-Nordheim tunneling effects (Figure 2b).[37] This way, the charge stored in the floating gate

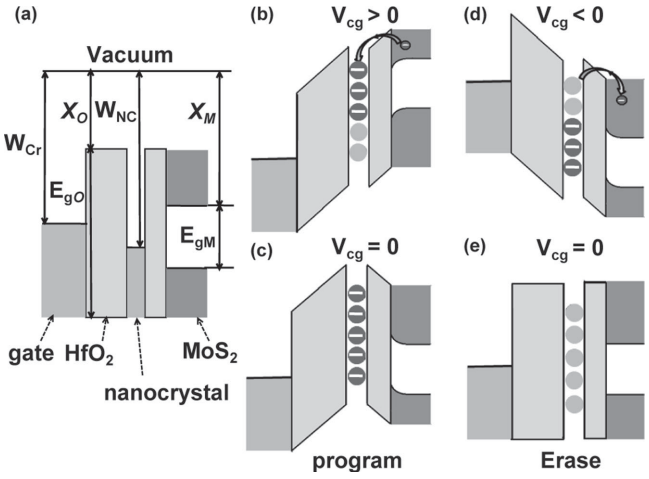

Figure 2. Simplified band diagram of the nanocrystal floating gate memory devices. (a) Flat band state with no contact between layers. W stands for the work function, E_g designates for the band gap and χ represents the electron affinity. Cr, O, NC and M stand for top gate, HfO_2 oxide, nanocrystals and MoS_2, respectively. (b-c) Band diagram of the program operation and state. Trapping level can be controlled by the metallic nanocrystal used as the floating gate. (d-e) Band diagram of the erase operation and state. Fermi level shift caused by the carrier density is not taken into consideration to simplify the band diagram.

will shift the V_{th} and the memory cell is turned into the program state (Figure 2c). By choosing the appropriate trapping layer, the trap level can be easily controlled. In order to discharge the floating gate, a strong negative voltage is needed to apply on the control gate and electrons will tunnel back to the MoS_2 channel (Figure 2d). When sufficient electrons are 'pushed' back to the channel, the channel becomes conductive and the memory cell can be operated back into the erase state again (Figure 2e).

It should be noted that the work function of the deposited nanocrystal is different with that of bulk materials.[38] To evaluate the trapping level of the nanocrystal, capacitance-voltage (C-V) characteristics of the device with different nanocrystal floating gates is given in **Figure 3**a. It is observed that the flat band voltage (V_{FB}) shifts to the positive side in order of Al, Ag, Co and Au. The flat band voltage is given by:

$$V_{FB} = \phi_{MS} - \frac{Q_i}{C_{ox}} - \frac{1}{\varepsilon_{ox}} \int_0^{t_{ox}} \rho_{ox}(x) x \, dx \qquad (1)$$

where Q_i designates for the charge located at the interface between the oxide and the semiconductor, and ρ_{ox} represent the charge density distributed within the oxide. It is clear that the V_{FB} of floating gate devices is largely affected by the presence of the charge trapped in the oxide layer as well as at the oxide-semiconductor interface.[39,40] Moreover, we have also fabricated a metal-oxide-semiconductor capacitor without nanocrystals in the dielectric, and the corresponding C–V characteristic is given in Supporting Information Figure S3. The C–V hysteresis of the control sample without nanocrystals is negligible, which indicates little charge trapped in HfO_2 and the interface. For the p-type substrate here, a positive shift of the V_{FB} indicates an enlargement of the charge trapped in the floating gate, inferring that the Au floating gate traps the most electrons. The capacitance of Al floating gate device is relatively low as compared with others. This is possibly attributed to the oxidation of deposited Al layer on top of the tunneling oxide surface and form a protective thin oxide, the oxidation increase the thickness of the dielectric, which decreases the gate oxide capacitance.

Figure 3b presents the transfer characteristics of various nanocrystal floating gate memory cells, sweeping the control gate voltage from –15 V to the positive side and then the opposite direction. Transfer characteristics of the transistor without nanocrystals in the dielectric are given in Supporting Information Figure S4. The small hysteresis of the transfer curve demonstrates that the hysteresis is mainly caused by the nanocrystal, not by the charge trapped in the interface. It is explicit that the memory windows increase with the work function of nanocrystal floating gates despite the deviation (Figure 3c) and Au case has the largest memory windows, just as predicted above. The V_{th} of Au/Co/Ag floating gate memory cells for program state are all roughly above 0 V, while the one of Al is below 0 V.

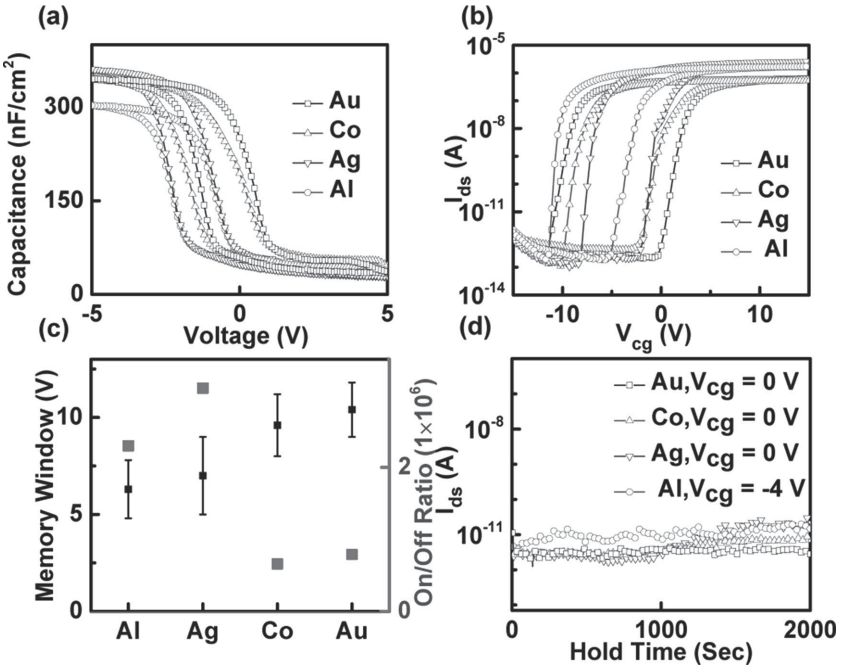

Figure 3. (a) C–V characteristics of the device with different metal nanocrystals. p-type Si is used as the substrate and Cr/Au (10/30 nm) with an area of 100×100 μm is deposited as the top electrode. (b) Transfer characteristics of the memory cell with different nanocrystals. (c) Memory windows and on/off ratio with different nanocrystal floating gates. (d) Evolution of the drain-to-source current of the program state for 4 different memory cells. The read voltage is set to be 0 V for the Au/Co/Ag cells since their V_{th} are all roughly at around 0 V but –4 V for the Al cell as its V_{th} is at –4 V.

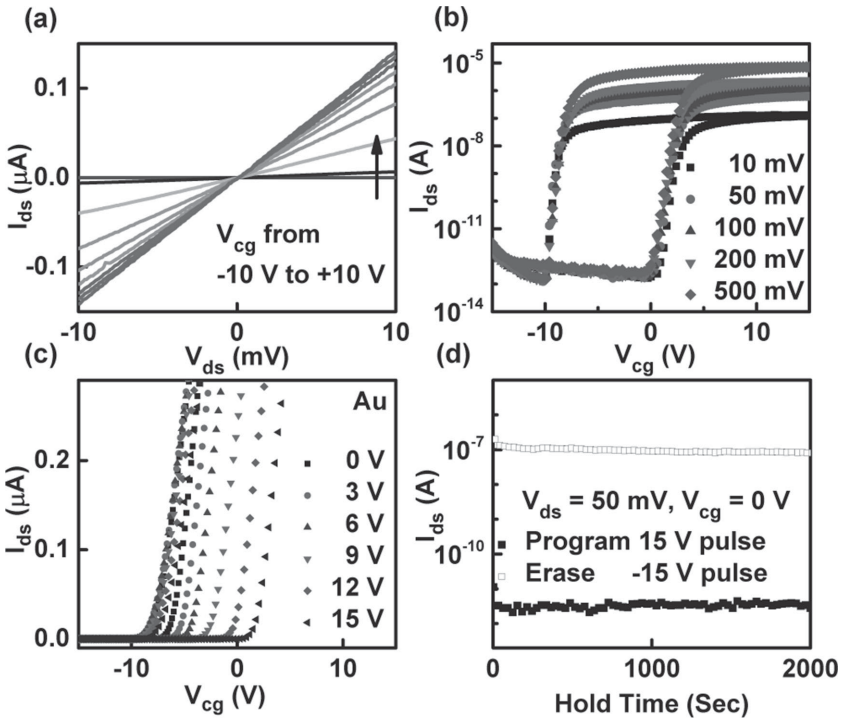

Figure 4. Electrical characteristics of the Au nanocrystal floating gate memory cell. (a) Output characteristics from -10 mV to 10 mV for different control gate voltage. (b) Transfer characteristics for different drain-to-source bias from 10 mV to 500 mV. (c) Dependence of memory windows on the control gate voltage applied to the device. The maximum control gate voltage varies from 0 V to 15 V. (d) Evolution of the source-to-drain current of the program/erase state in 2000 s of hold time. The voltage pulse duration is 3 s.

Also, the evolution of I_{ds} of the program state is given in Figure 3d. After a +15 V pulse at the control gate with duration of 3 s, we read the program state current at a constant drain voltage of 50 mV for 2000 s. After 2000 s, the program state current shows almost no increase, indicating very little charge leakage from the floating gate. Since Au has the largest work function here, the charge stored in the floating gate needs more energy to escape from the trap, resulting in the smallest leakage from the oxide layer compared to others.

In view of the excellent charge retention capability of the Au nanocrystal floating gate memory cell, more detailed electrical measurements are performed to evaluate its characteristics. First, we carry out a small bias I_{ds}-V_{ds} study with different V_{cg} to assess the contact properties of these devices, which are the key factors influencing the corresponding signal delay and frequency response.[12] As depicted in **Figure 4**a, all curves fit the linear relationship even under a relatively small bias of 10 mV, suggesting a good ohmic-like contact between Cr and MoS_2 (more detailed information is given in Supporting Information Figure S5). In future, lower work function metals such as Sc can also be employed for the improved contacts with MoS_2 flakes, implying higher output current with the lower voltage. Also, as shown in Figure 4b, it is obvious that all transfer curves do not exhibit any significant shift and all exhibit a consistently large memory window of 11 V when the drain-to-source bias (V_{ds}) is varied. Importantly, the maximum drain current increases accordingly in the same ratio with the V_{ds}, ranging from 10 mV and 500 mV, illustrating a stable electrical performance for these floating gate cells.

Next, the amount of electrons tunneling through the oxide and the corresponding charge density are assessed in order to investigate the effect of potential change of the floating gate as well as the threshold voltage on the memory cell. The tunneling probability is highly depended on the corresponding potential difference such that any change of the maximum V_{cg} would affect the resulting electron tunneling process. As presented in Figure 4c, when the maximum control gate voltage ($V_{cg,max}$) increases from 0 V to 15 V, the memory window changes from 2 V to 11 V, respectively, indicating the larger amount of charge trapped in the floating gate with higher $V_{cg,max}$. Similar studies on other nanocrystal floating gate cells are also given in Supporting Information Figure S6. The charge stored in the floating gate is electrons rather than positive charges for the erase state lines are overlapped. Notably, even for different amount of electrons get stored in the gate, the same erase voltage can still erase them all, yielding insignificant V_{th} shift in the erase state, which suggests no positive charge tunneling through the oxide. This way, the charge density can be calculated by $n = (\Delta V \times C_{FG-CG})/q$, where $\triangle$V is the memory window of ~10 V, $C_{FG\text{-}CG}$ can be obtained as $C_{FG-CG} = \varepsilon_0 \varepsilon / d$, for ε_0 is the permittivity of vacuum, ε is relative dielectric constant and d is thickness of the blocking oxide.[41] As the ALD grown HfO_2 blocking oxide is 20 nm thick with the relative dielectric constant of 11, the charge density is estimated to be ~2.9×10^{13} cm^{-2}, which is in agreement with that of nonvolatile memory capacitor based on Au nanocrystals[42] and comparable to the one of newly developed multi-layer graphene floating gate.[12] At the same time, the current at both program and erase state are quite stable with a program/erase ratio of approximately 10^5 within a duration of 2000 s, as shown in Figure 4d. All these demonstrate a sufficiently large and stable memory window with strong potential for the multi-level data storage.

Furthermore, the dynamic behavior of the fabricated cells is also examined. Control gate voltage pulses (±15 V) with different pulse duration are applied to the cells while the V_{ds} is set constant at 50 mV. As given in **Figure 5**a, for a fixed pulse width of 300 ms, stable and reproducible switches with the program/erase ratio of approximately 10^5 between the erase and program state can be attained. When the pulse width decreases from 300 ms to 100 ms, the program state current stay constant, illustrating a fully programmable and effective memory cell here (Figure 5b). However, the erase state current decays slowly, partly attributable to the charge impurities at the semiconductor/dielectric interface.[43] For the shorter pulse width down to 10 ms, the program state current increases slightly by approximately a decade

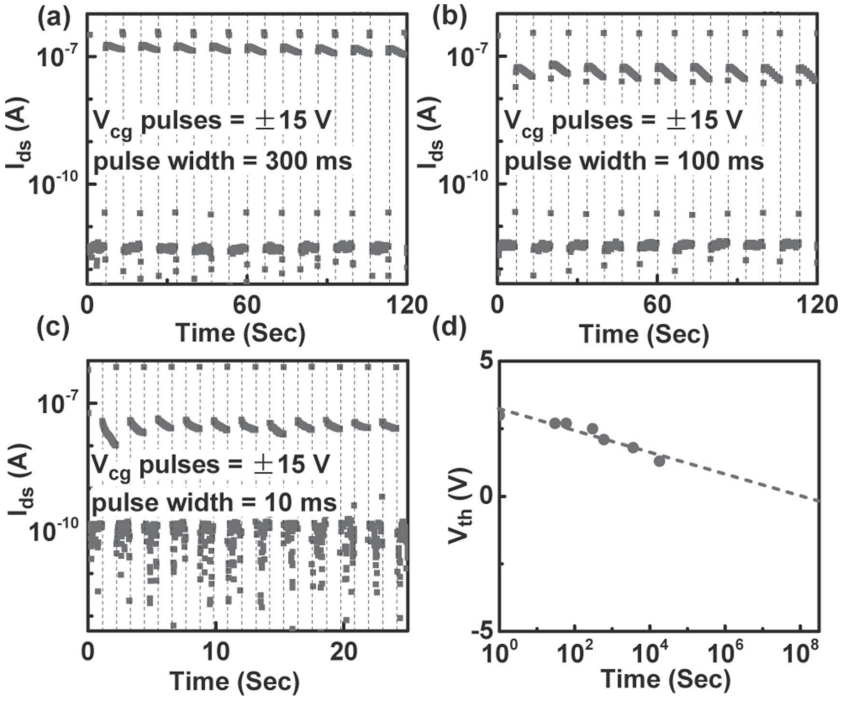

Figure 5. Switching dynamics and charge retention characteristic of the Au floating gate memory cell. (a-c) Switching dynamics of the Au floating gate memory cell in response to voltage pulse width of 300, 100, 10 ms. (d) Charge retention characteristic of the Au floating gate memory cell.

(Figure 5c). This may be caused by the unoptimized contact resistance, in which this current increase can be alleviated with the improved electrical contacts.

Also, since the charge retention is extremely sensitive to the temperature and humidity, in order to ensure a stable operating environment, measurement of the retention time is carried out in ambient and dark condition with the temperature of 15 °C. The amount of charges stored in the floating gate can be calculated from the corresponding V_{th} shift. After a +15 V voltage pulse with a duration of 3 s, the transfer characteristic is measured to evaluate the V_{th} of the state. The scanning range is set to be relatively small of 0 V to 4 V and the pulses are applied to the control gate after each measurement in order to minimize the influence of the tunneling electrons that are imported. Time-resolved behavior of the device V_{th} is presented in Supporting Information Figure S7. As shown in Figure 5d, the V_{th} of the program state changes from 3.1 V to 1.3 V within 5 h. The erase state shows almost no shift. Since the erase state V_{th} is maintained at –7 V, we can estimate that the charge retains ~60% after ten years, demonstrating good charge retention characteristics. However, there are still several problems needed to be solved in the near future. As the V_{th} is relatively negative, even there are about 60% of the charges stored in the floating gate, the channel is conductive at 0 V. Although this problem can be resolved by shifting the read voltage to the negative side, further study is probably needed to improve the memory cell performance and characteristics.

In summary, we have fabricated nonvolatile floating gate memory cells based on MoS_2 transistors with different nanocrystals embedded in gate dielectrics and found that the Au nanocrystal memory cell exhibits the best device characteristics. Importantly, the cell gives the excellent on/off ratio over 10^6, large memory window of 10 V, stable program/erase ratio of approximately 10^5 and good retention time for 10 years. Also, this convenient fabrication scheme of nanocrystal floating gates is compatibility with the existing memory cell production process.[25] All these impressive performance as well as the easy process integration evidently indicate the technological potency of these MoS_2 based nanocrystal floating gate cells for the development of future nonvolatile memory devices.

Experimental Section

Materials: Monolayer MoS_2 were prepared by mechanically exfoliated from bulk MoS_2 crystal (purchased from SPI supplies). The number of layers in these MoS_2 nanosheets was distinguished by the inspection under optical microscope and Raman spectroscopy.

Device Fabrication: The source/drain electrodes were deposited through electron-beam lithography and lift-off processes. PMMA was used as the resist layers and after the development of the patterns, Cr/Au was deposited by the thermal deposition. After the deposition, we used acetone to lift-off the patterns. Tunneling and blocking oxide were grown with KE-MICRO TALD-200A. Various nanocrystals were deposited by the thermal deposition under 6×10^{-4} Pa.

AFM characterization: AFM imaging was performed by Bruker Multimode 8 with Scan Assist-Air probe under peak force mode in the ambient condition. In order to get the representative morphology of the metal grains, we characterized the surface of the metal nanocrystals right after the deposition within an hour. Before the final image was recorded, a relatively low setpoint was used to protect the tip of the probe. Since Al is oxidized easily in air and the oxidized Al nanocrystal floating gate cannot store much charge, resulting in the small memory window. Therefore, we deposit 1.5 nm Al instead to minimize the oxidation effect.

Electrical Characterization: Output and transfer curves were obtained using 4155C semiconductor parameter analyzer in the ambient condition at room temperature. C-V behavior was measured with Keithley 4200-SCS semiconductor characterization system in the air ambient at room temperature. Switching dynamics and charge retention properties were characterized using Agilent B2902A in the ambient condition.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

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