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Sub-kT/q switching in In_2O_3 nanowire negative capacitance field-effect transistors†

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Limited by the Boltzmann distribution of electrons, the sub-threshold swing (SS) of conventional MOSFETs cannot be less than 60 mV dec^{-1}. This limitation hinders the reduction of power dissipation of the devices. Herein, we present high-performance In_2O_3 nanowire (NW) negative capacitance field-effect transistors (NC-FETs) by introducing a ferroelectric P(VDF-TrFE) layer in a gate dielectric stack. The fabricated devices exhibit excellent gate modulation with a high saturation current density of 550 μA μm^{-1} and an outstanding SS value less than 60 mV dec^{-1} for over 4 decades of channel current. The assembled inverter circuit can demonstrate an impressive voltage gain of 25 and a cut-off frequency of over 10 MHz. By utilizing the self-aligned fabrication scheme, the device can be ultimately scaled down to below 100 nm channel length. The devices with 200 nm channel length exhibit the best performances, in which a high on/off current ratio of $>10^7$, a large output current density of 960 μA μm^{-1} and a small SS value of 42 mV dec^{-1} are obtained at the same time. All these would not only evidently demonstrate the potency of NW NC-FETs to break through the Boltzmann limit in nanoelectronics, but also open up a new avenue to low-power transistors for portable products.

Introduction

The aggressive miniaturization of traditional metal–oxide-semiconductor field-effect transistors (MOSFETs) has led to the increase in chip density and operating frequency. At the same time, the corresponding higher power consumption would become a major challenge, especially in battery-operated portable devices.[1,2] Lowering the subthreshold swing (SS) is an effective way to reducing the operating voltage of the devices. However, because of the Boltzmann distribution of carriers, the SS of conventional MOSFETs cannot be less than 60 mV dec^{-1} at room temperature.[2,4] This limitation hinders the reduction of power dissipation of the devices. Pursuing new device configurations with a lower SS would be one of the promising approaches to tackle the power consumption issue.[4,5] Particularly, the reduced SS is critical for further development of sub-100 nm channel length (L_{ch}) transistors, in which the short-channel effect and unavoidable leakage current dominate the overall carrier transport.[6,7] Negative capacitance field-effect transistors (NC-FETs) are revealed to break through the SS limit of 60 mV dec^{-1} by introducing a ferroelectric layer into the gate stack.[5] NC-FETs have received more and more attention in recent years due to their excellent modulation behaviors and compatibility with the conventional integrated circuits.[3–5,8]

In theory, the SS of typical MOSFETs can be obtained by

$$SS = \frac{\partial V_{gs}}{\partial \Psi_S}\frac{\partial \Psi_S}{\partial(\log_{10} I_{ds})} = \left(1 + \frac{C_S}{C_{int}}\right)\frac{K_B T}{q}\ln 10 \qquad (1)$$

where V_{gs} is the gate voltage, I_{ds} is the drain current, Ψ_s is the surface potential of the transistor channel, K_B is the Boltzmann constant, T is the temperature, and C_S and C_{int} are the capacitance of the channel layer and dielectric layer, respectively. When the ferroelectric gate insulator exhibits negative differential capacitance characteristics during the polarization switching process, $(1 + C_s/C_{ins})$ could be smaller

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than 1 and make SS less than 60 mV dec^{-1} at room temperature (T = 300 K).[8,9] In other words, since the ferroelectric gate insulating layer can induce disproportionate changes in the carrier concentration through nonlinear polarization processes, a small increment of applied voltage would then lead to numerous charges accumulating onto the ferroelectric/channel interface.[3,5,10] Therefore, the sensitivity of the applied gate voltage to the surface potential can be greatly enhanced, yielding the sub-60 mV dec^{-1} swing to the device operation at room temperature.

At the same time, non-planar device structures have been extensively explored for enhanced electrostatic control.[11–13] Ultrathin and narrow body (nanowire) transistors are hence developed for aggressive channel length scaling while maintaining excellent gate control.[11,12] Among many potential materials, In_2O_3 NWs possess a wide band gap of 2.8 eV and a high field-effect mobility (~1500 cm^2 V^{-1} s^{-1}),[12,13] which is advantageous for the fabrication of transistors with a large on–off ratio, high-speed operation and low-power consumption. The low dielectric constant of In_2O_3 (~4.1) would also make it suitable for the channel material of NC-FETs,[14] considering that the required substantial semiconductor capacitance can be contributed by the increased oxide and ferroelectric capacitance for the capacitance matching in stable negative-capacitance structures.[8,14,15] Also, the dielectric layer thickness must be decreased for the larger dielectric capacitance, in which all these would induce significant difficulty in the gate fabrication processes and yield the corresponding gate leakage issue.[8,15] Meanwhile, the good metal–semiconductor contact of the In_2O_3 NWs also makes them desirable for various device applications.[16–18] In any case, although several previous studies have demonstrated the steep subthreshold characteristics in transistors using ferroelectric gate dielectrics,[9,10,19–21] the NW based NC-FETs with ultra-short channels (*i.e.* sub-100 nm) have never been reported until now. In such a short channel regime, there are a number of device phenomena, such as the short-channel effect, drain-induced barrier lowering (DIBL) and other fabrication issues, which would critically impact the power consumption of the fabricated transistors.[6,22,23] Therefore, developing ultra-short channel NC-FETs employing NWs is not only a prototype demonstrated for fundamental research, but also a key step to overcome practical challenges in the semiconductor industry.

Herein, taking advantages of both the negative capacitance effect of ferroelectrics as well as the superior electrical modulation performance of the In_2O_3 NWs, we present a novel approach to fabricate high-performance In_2O_3 NW NC-FETs. The fabricated devices exhibit an ultra-small SS value of less than 60 mV dec^{-1} for 4 orders of magnitude of the channel current (channel length, L_{ch} = 3 μm) at room temperature. Importantly, the saturation current density can reach 550 μA μm^{-1}, which is comparable to the one of the advanced FinFETs.[24,25] The simple inverter circuit composed of multiple NCFETs is also demonstrated, and the inverter achieves a large voltage gain of 25 and a cut-off frequency of over 10 MHz. In order to further explore the performance limit of In_2O_3 NW NC-FETs, the self-alignment fabrication approach is employed to obtain devices with the L_{ch} scaled down to 100 nm. Devices with 200 nm channel length exhibit the best performances, in which a high on/off current ratio of >10^7, a large output current density of 960 μA μm^{-1} and a small SS value of 42 mV dec^{-1} are obtained at the same time. It is also noted that the highest process temperature during the device fabrication is 150 °C, which is entirely compatible with the state-of-the-art flexible electronics on plastic substrates, and opening up potential utilizations of the In_2O_3 NW NC-FETs in new application domains.

Results and discussion

Fig. 1a depicts the schematic illustration of the side-gated In_2O_3 NW NC-FETs, while the inset gives the corresponding equivalent circuit diagram and all the details of their fabrication processes are presented in Fig. S1 in the ESI.† In brief, a copolymer (MMA) layer was first spin-coated onto the substrate. Subsequently, chemical vapour deposition (CVD) grown In_2O_3 NWs with diameters of ~60 nm were transferred onto the Si/SiO_2/MMA substrate using a contact-printing method (see Fig. S2 in the ESI†).[16] The external electrodes were then patterned by electron-beam lithography (EBL) with a distance of 500 nm between the dual-side-gated electrodes, followed by Cr/Au (20/100 nm) deposition. As a result, the fabricated NW channel was suspended from the device substrate after electrode lift-off (Fig. 1b). Next, HfO_2 with a specific thickness and matched capacitance was deposited for a stable negative capacitance structure using atomic layer deposition (ALD); this way, the asymmetrical charge screening and gate leakage current could be minimized accordingly. Finally, the P(VDF-TrFE) (70 : 30 in mol%) film was spin-coated onto the substrate and baked on a hot plate at 130 °C for 30 min for the crystallization of P(VDF-TrFE) ferroelectric domains. Fig. 1c shows the electric field distribution in the channel region of three different NW transistor configurations: a dual-gated transistor with the NW being suspended, a normal dual-gated transistor and a single-gated transistor. The results are simulated using an element analysis method. It is evident that the suspended NW channel achieves the largest polarization around the NWs, considering that the coercive electric field of the P(VDF-TrFE) film is around 50 MV m^{-1} with the detailed simulation results given in Fig. S3 in the ESI.†[26,27] Moreover, the capacitance deviation caused by the slight deviation in the gate patterning process can be reduced as well, which improves the corresponding error-tolerant range in the fabrication processes (see Fig. S3 in the ESI†).

The HfO_2 layer between the In_2O_3 NWs and the ferroelectric layer is deposited for reducing the interfacial impact and rendering the entire system, including the gate stack/channel layer, energetically stable.[4,28,29] Moreover, if a steep subthreshold device characteristic defined by the negative capacitance is targeted here, the subthreshold region of the transistor has to be precisely overlapped with the voltage operating range of

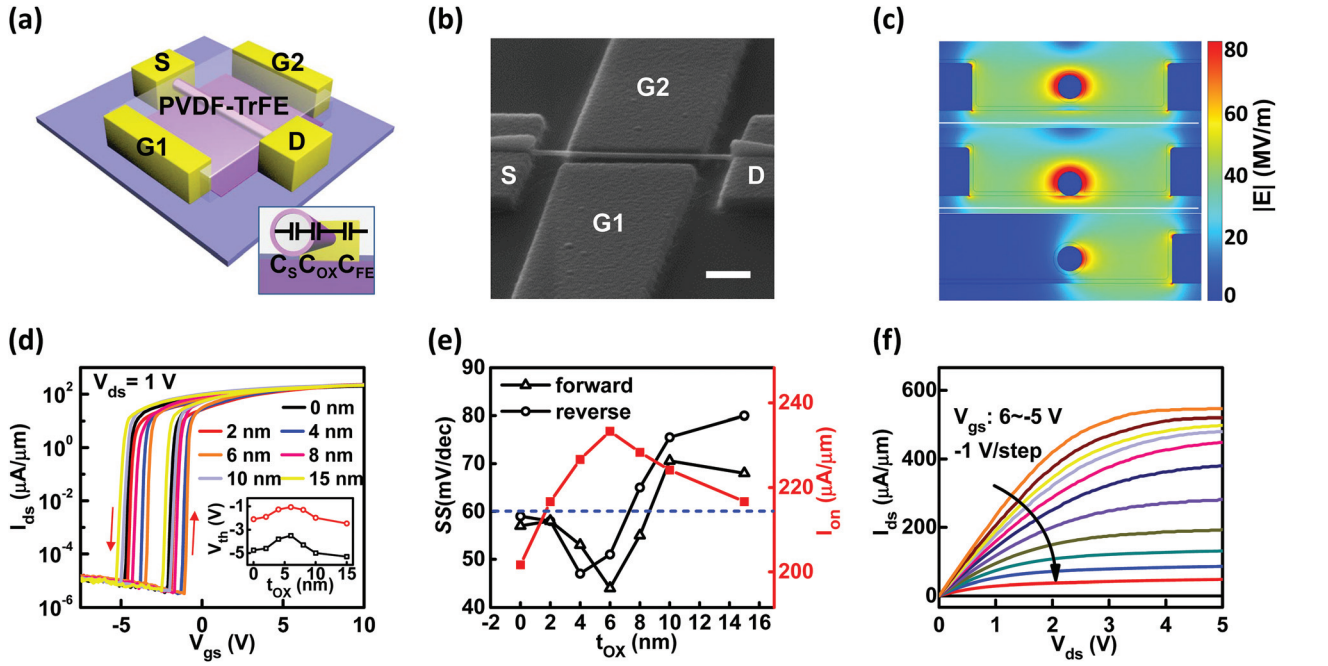

Fig. 1 Device structures and electrical performances of the side-gated In_2O_3 NW NC-FETs. (a) Schematic diagram of the employed device structure. The inset shows the equivalent capacitor model of the NC-FET. (b) SEM image of the device channel with the substrate tilting at 70°. The scale bar is 1 μm. (c) Cross-sectional electric field distribution of different NW device architectures using finite element analysis simulation. The top, mid and bottom represent the dual-gated transistor with NW suspending, normal dual-gated transistors and single-gated transistors, respectively. (d) Transfer curves of devices with different thicknesses of the HfO_2 layer. V_{gs} sweeps between ±10 V and the sweep speed is 0.4 V s^{-1}. The inset gives the threshold voltage (V_{th}) *vs.* HfO_2 thickness (t_{OX}) data. The red and black lines represent the forward sweep and reverse sweep, respectively. (e) The on-state current density (I_{on}) and SS extracted as a function of t_{OX}. (f) The output characteristics of the NC-FET with 6 nm thick HfO_2 and P(VDF-TrFE) as the dielectric layer.

the ferroelectric layer. Therefore, devices with various HfO_2 thicknesses (t_{OX}) are studied in order to achieve the maximum voltage amplification effect of ferroelectric P(VDF-TrFE), and their transfer characteristics are then evaluated as shown in Fig. 1d. The Fig. 1d inset gives the relationship of the threshold voltage (V_{th}) *versus* t_{OX}, while Fig. 1e displays the on-state current density (I_{on}) and SS extracted from their transfer characteristics. It is clear that the device with the gate stack dielectric of 6 nm HfO_2 can achieve the maximum voltage amplification with an ultra-small SS value of 44 mV dec^{-1} when simultaneously operating at the largest I_{on} and smallest V_{th}. Notably, both the SS values extracted from the forward sweep direction (from −10 V to 10 V, SS_{for}) and the reverse sweep direction (from 10 V to −10 V, SS_{rev}) are less than 60 mV dec^{-1} at room temperature. As the t_{OX} is larger than 8 nm, the voltage drop across the ferroelectric layer becomes smaller, and the thick oxide layer causes the negative capacitance of the ferroelectric layer to be masked in the total series capacitance of the gate stack. On the other hand, when the t_{OX} is less than 4 nm, the deposited HfO_2 layer is not dense enough to suppress the interfacial impact.[28] All these results indicate that the 6 nm thick HfO_2 layer is most suitable to be the insertion layer here. In addition, the hysteresis mostly originated from the fact that the internal gate voltage change cannot promptly follow the change speed of the external gate voltage. As the copolymer P(VDF-TrFE) is comprised of long carbon chains, the switching time becomes even longer so that it is challenging to minimize or completely eliminate the hysteresis in our work. In order to confirm the origin of the hysteresis, we have fabricated devices of the same dimensions and structures but with a non-ferroelectric polymethyl methacrylate (PMMA) layer. The device exhibits a slight hysteresis and it confirms that the hysteresis in our NC-FETs is derived from the polarization behavior of the ferroelectric layer. More details are shown in Fig. S4 in the ESI.† Fig. 1f demonstrates the output characteristics of the device, illustrating the efficient saturation and pinch-off behavior as well as suggesting the effective modulation of the In_2O_3 active channel controlled by the gate voltage. The saturation current density can reach up to 550 μA $μm^{-1}$, proving that the output current density has not been sacrificed for the diminution of SS.[27,30] As the control sample, In_2O_3 NC-FETs with the non-suspended NW channels were also fabricated and studied as shown in Fig. S5 in the ESI.† The SS_{for} is found to be larger than the SS_{rev}, while both values are higher than the sub-threshold limit of 60 mV dec^{-1}. This performance degradation is mainly attributed to the charge accumulation in the In_2O_3/SiO_2 interface, and the gate coupling in the non-suspended structure is not as desirable as that in the suspended ones. This is consistent

with the simulation results, indicating the superiority of the designed gate geometry with the suspended NW channel.

In order to demonstrate the prominent modulation and output characteristics of NC-FETs as well as to explore their versatility in device integration, multiple devices were employed to construct functional digital circuits. Two NC-FETs with different channel lengths were fabricated on a single In_2O_3 NW, serving as the "switch" and the "load" of the inverter respectively. Fig. 2a depicts the SEM image of the fabricated inverter circuit. In particular, the gate of the "switch" transistor is operated as the input terminal while the electrode connection between the "switch" and the "load" acts as the output terminal. The equivalent circuit diagram is shown in the Fig. 2c inset. As presented in the static DC output characteristic in Fig. 2b, it is obvious that the input voltage can be effectively transferred into its opposite state by the inverter circuits. The voltage gains can then be extracted accordingly and importantly, and a gain higher than 25 is obtained (Fig. 2c).[31] The dynamic response of the inverter can also be further evaluated using a harmonic-waveform input signal spanning from 100 to 10 MHz (Fig. 2d), in which the obtained performance is comparable to those of the advanced gate-all-around single crystal silicon NW inverters.[31–35] Notably, the AC gain is kept relatively stable at around 20 until the input frequency is increased to 300 kHz, while the inverter can be characterized by a cut-off frequency of above 10 MHz. All these results have demonstrated the outstanding performances and integration capabilities offered by the In_2O_3 NC-FETs.

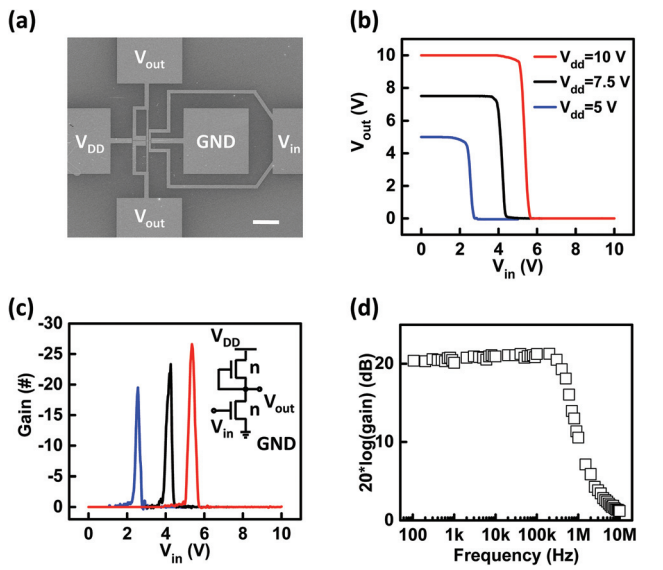

Fig. 2 Electrical performances of the inverter assembled by two NC-FETs. (a) SEM image of the inverter circuit. The scale bar is 20 μm. (b) The static D.C. output properties of the inverter circuit with different V_{dd}. (c) D.C. voltage gain of the inverter as a function of the input voltage. The inset is the equivalent circuit diagram of the inverter circuit. (d) The frequency dependence of the A.C. voltage gain (dB) of the inverter.

Generally, as both the properties of semiconductors and ferroelectrics can be easily affected by temperature changes, it is important to assess their temperature dependence on the device performance of the NC-FETs. Fig. 3a gives the temperature dependence of the transfer characteristics of a typical In_2O_3 NW NC-FET. A metal–insulator transition is observed in the NC devices. When the V_{gs} is less than −2.5 V, In_2O_3 NWs behave as a classical semiconductor with conductance decreasing as the temperature is decreased. Whereas for V_{gs} > 3 V, it is obvious that the conductance increases as the temperature is decreased, which is a hallmark of metallic behavior.[35,36] These findings indicate apparently different device operating regimes as depicted in Fig. 3b. The transition from the insulating state to the metallic state further indicates the high quality of our In_2O_3 channel and the non-damaging nature of the fabrication process.[35] As shown in the details of I_{on} and V_{th} of both forward and reverse sweeps in Fig. 3c, the I_{on} increases with the decreasing temperature whereas the V_{th} and pinch-off voltage shifts to the positive direction, demonstrating the dominant role of the negative capacitance device structure in the gate modulation here. Also, Fig. 3d shows a V_{gs} dependence of the transconductance (g_m) *versus* V_{gs} at various temperatures. The height of the g_m peaks increases as the temperature is decreased, reflecting the enhancement of the voltage amplification effect caused by the negative capacitance device structure; and this is consistent with the previous simulations about dual-gated negative capacitance devices.[20,37] Regardless, the In_2O_3 NW NC-FETs present quite different temperature dependent performances as compared with the top-gated In_2O_3 NW MOSFETs fabricated with only HfO_2 as the gate dielectrics (Fig. 3e and Fig. S6 in the ESI†). The pinch-off voltages of the top-gated devices typically shift to the negative direction as the temperature decreases, which is opposite to the NC-FETs studied above. In addition, the MOS device shows non-hysteresis operation until the temperature increases to above 240 K, while the SS_{for} value is always larger than the SS_{rev} one when the hysteresis appears. The hysteresis character of the In_2O_3 NW MOSFET most probably originated from the interface traps around the NW channel, because the interface traps can be suppressed at low temperatures, resulting in the elimination of the hysteresis.[20,38,39] As a comparison the polarization-originated hysteresis character observed in the NC-FETs changes little as the temperature changes from 80 K to 300 K. It is also noted that the introduction of organic ferroelectric layers could reduce the gate leakage current due to their excellent electrical insulating properties (see Fig. S5 in the ESI†). Fig. 3f shows the temperature dependence of SS for both NC-FETs and top-gated MOSFETs. The SS values of NC-FETs are smaller than those of the top-gated counterparts for the entire temperature range. All these demonstrate that the simple insertion of an NC ferroelectric layer in the gate dielectric stack can efficiently lower the transistors' power consumption, especially in the device subthreshold region.

As aforementioned, the side-gated NC-FETs exhibit desirable modulation in the subthreshold region with SS values less than 60 mV dec^{-1} at room temperature. Nevertheless, to inves-

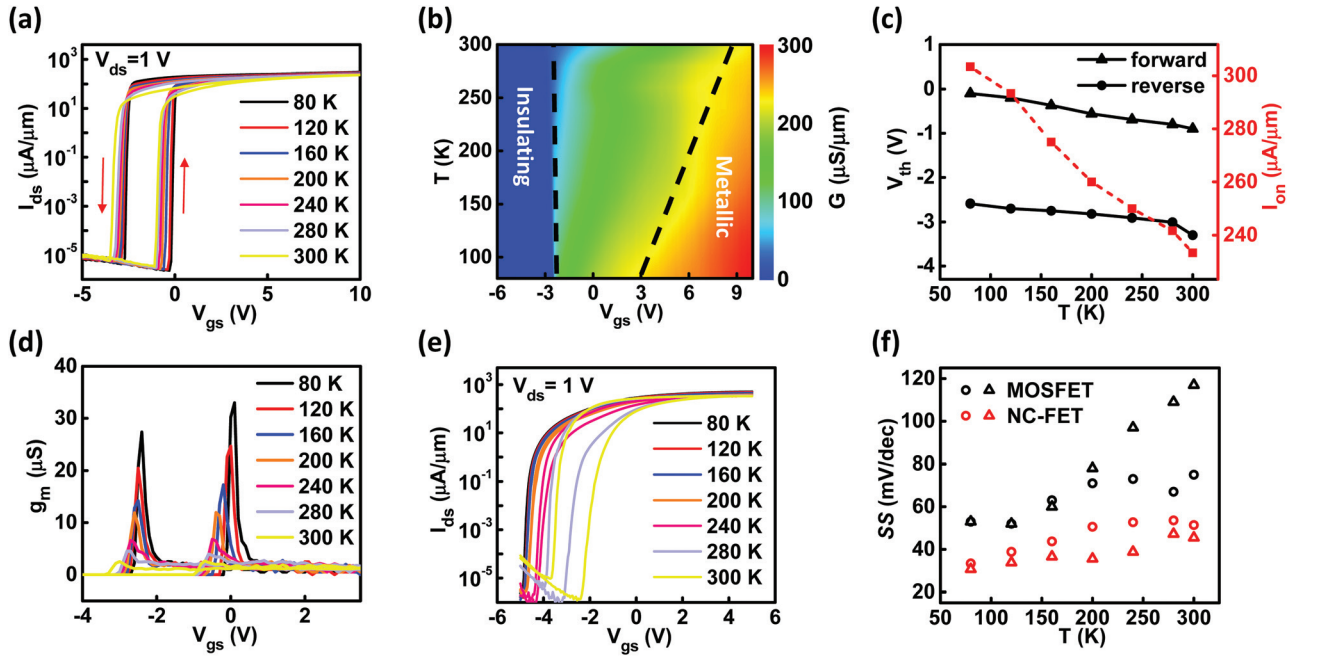

Fig. 3 Low-temperature characteristics of the side-gated In_2O_3 NW NC-FETs. (a) Typical transfer characteristics of the NC-FETs at various temperatures, ranging from 80 K to 300 K. V_{gs} ranges from −10 V to 10 V with a sweeping speed of 0.4 V s^{-1}. (b) 3D plot of drain conductance density (*G*) *versus* temperature (*Y* axis) and gate voltage (*X* axis) of the In_2O_3 NW NC-FETs. The guided line (black dash) illustrates the transition from the insulating state to the metallic state. Bias voltage is 1 V. (c) Detailed plots of the threshold voltage extracted from both the V_{gs} forward sweep (from −10 V to 10 V) and the reverse sweep (from 10 V to −10 V) and I_{on} *versus* the temperature. (d) Transconductance *versus* V_{gs} at varying temperatures within the subthreshold region (−4 V to 3.5 V) (e) Transfer characteristics of the normal top-gated In_2O_3 NW MOSFETs at various temperatures. The dielectric layer of the device is 6 nm HfO_2 only. (f) Temperature dependence of SS from 80 K to 300 K, for both the side-gated In_2O_3 NC-FETs and the top-gated In_2O_3 MOSFETs. The triangular and round symbols represent the forward and reverse sweeps, respectively.

tigate the miniaturizing scalability of the In_2O_3 NW NC-FETs, the self-aligned fabrication method is then employed for shrinking the L_{ch} down to 100 nm.[40–42] Fig. 4a–c show the schematic illustration of the corresponding device fabrication processes. A suspended NW channel was first fabricated without any gate electrode. Subsequently, considering the negligible change of the coercive electric field of P(VDF-TrFE) with its thickness ranging from 40 nm to 200 nm and the easy dielectric breakdown of HfO_2 with the thickness below 6 nm, a 6 nm thick HfO_2 layer was hence selected to be deposited to be the insertion layer and preventing the NW from being shortened in the following processes.[43] Then, the self-aligned process was introduced by depositing an 8 nm Cr/Au film across the In_2O_3 NW onto the substrate, where the NW was just used as a "shadow mask" there. Finally, the gate leads were added onto the Cr/Au film and the P(VDF-TrFE) film was spin-coated onto the entire substrate. Fig. 4d presents the SEM image of a representative gate self-aligned In_2O_3 NW NC-FET with a 200 nm length channel, in which the bright electrodes, dark electrodes and area enclosed within the dashed box are the source/drain regions, gate leads and self-aligned gates, respectively. As compared with the side-gated structure, the self-aligned gate configuration not only eliminates the parasitic resistance, but also shortens the distance between the gate and the NW. We have also made a simulation for the electric field distribution around the channel region of the self-aligned NC-FET (Fig. 4e and f). It is evident that the electric field modulus around the NW in this self-aligned structure is three times that in the side-gated structure when applying the same gate voltage. The details of the simulation are shown in Fig. S7 in the ESI.† As a result, the energy consumption of the gate self-aligned NC-FETs can be largely minimized due to the reduced operating voltage as well as the compatibility with ultra-short channel technologies.

Furthermore, the scaling behavior of the gate self-aligned In_2O_3 NW NC-FETs is also studied by fabricating a set of devices with different channel lengths on an individual In_2O_3 NW (Fig. 5b inset). In detail, the L_{ch} of all devices spans from 3 μm to 100 nm, and all devices are measured under the same test conditions. Fig. 5a shows the transfer characteristics of the devices. The reverse sweeping curves are only displayed there for the ease of observation, while the forward sweeping curves are shown in Fig. S8 in the ESI.† All devices can be fully turned on and pinched off with operation voltages smaller than 2 V. The I_{on} increases proportionally as the channel length is reduced, and the SS can be kept reliably less than 60 mV dec^{-1} over 4 decades of I_{ds} until the L_{ch} is scaled down to 200 nm (Fig. 5b). When the device channel length is further scaled to 100 nm, the shape of the transfer curve becomes different from the previous devices. In particular, the corresponding SS value is increased to 90 mV dec^{-1}, being higher than 60 mV dec^{-1}. This deviation can be understood as the

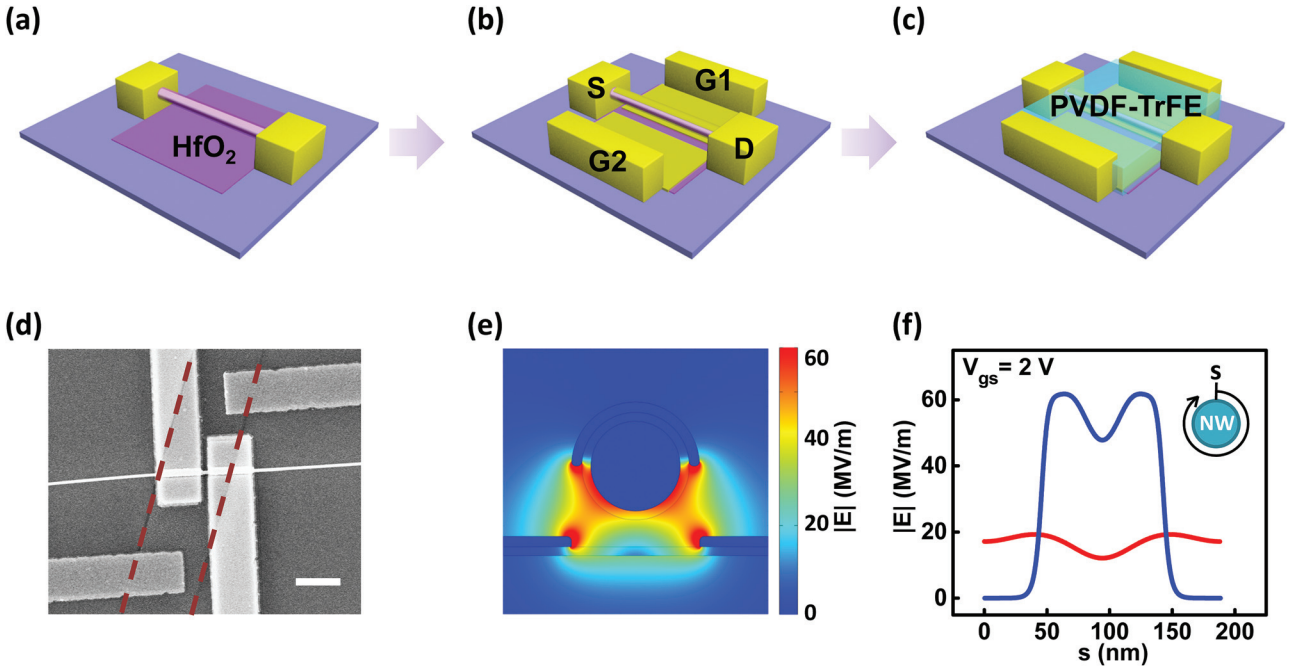

Fig. 4 Device structures of the gate self-aligned In_2O_3 NC-FETs. (a) A layer of MMA is spin-coated onto the Si/SiO_2 substrate followed by the transfer of In_2O_3 NWs. Standard e-beam lithography is applied to define the source and drain electrodes. Then, an HfO_2 buffer layer is deposited by ALD. (b) A small window across the NW channel is patterned by the EBL process and followed by the self-aligned metal deposition, after which the gate leads were added onto the thin Cr/Au film. (c) The ferroelectric P(VDF-TrFE) film is assembled by the spin-coating process at 2000 rpm, and then baked on the hot plate at 130 °C for 30 min. (d) SEM image of the gate self-aligned In_2O_3 NW transistor with L_{ch} = 200 nm. The scale bar is 1 μm. The dashed lines indicate the area of the Cr/Au film. (e) Cross-sectional electric field distribution of the gate self-aligned device architecture. (f) The simulation results for the electric field modulus distribution around the NW, and the *x*-axis is defined as shown in the inset. The blue line and red line represent the non-self-aligned architecture and gate self-aligned architecture, respectively.

fact that the parasitic contact resistance cannot be neglected any more in ultra-short channel devices; otherwise, since the short L_{ch} of 100 nm is somewhat comparable to the mean free path of charge carriers, the electron transport mechanism may be altered to the quasi-ballistic transport here.[16,44] As a result, we believe that the performance degradation of the sub-100 nm channel devices would be alleviated by shrinking the diameter of the NW channels.[44,45] Also, Fig. 5c compiles a summary of g_m and V_{th} of the gate self-aligned In_2O_3 NC-FETs as a function of L_{ch}, ranging from 100 nm to 3 μm. The peak g_m value is found to approach 13.6 μS for the 100 nm channel length device. The pinch-off voltage is as well revealed to drift to the negative direction with the reducing channel length. In principle, the gate self-aligned configuration is a special kind of side-gated device structure. The narrower side-gate width would typically lead to the smaller electric field near the NW surfaces; therefore, the V_{th} would shift towards the negative direction with the decreasing L_{ch}.[27] We have also fabricated gate self-aligned devices with the non-suspended structure (see Fig. S9 in the ESI†), in which the device performance is not comparable to the one of the suspended structure because of the insufficient ferroelectricity induced between the gate tip and the NW channel.

As discussed above, devices with 200 nm channel length can exhibit excellent modulation properties. The transfer characteristics of an independent device with a 200 nm long channel are shown in Fig. 5d, where a high I_{on} of 86 μA μm^{-1} and an outstanding on/off current ratio larger than 10^7 have been achieved. Notably, the V_{th} of both forward and reverse sweeps are located at around 0.8 V and −1.5 V, respectively. The details of the reverse sweep in the subthreshold region are as well depicted in the Fig. 5d inset, which indicates that the SS of the device can stay steadily over 4 decades of I_{ds}. The average SS can be calculated to be 42 mV dec^{-1} over 5 decades, indicating the superior modulation capability of the NC structure here. Nevertheless, the SS_{for} value is slightly larger than the SS_{res}, and reaches 107 mV dec^{-1}. This can be attributed to the thin metal film covered on top of the In_2O_3 NWs, which reduces the coupling of the nanowire channel and the ferroelectric layer (see Fig. S7 in the ESI†). At the same time, the output saturation current density can reach up to 960 μA μm^{-1}, reflecting the superior output characteristics of these short channel devices (Fig. 5e). In order to further investigate the stability and reproducibility of these devices, a statistical analysis of the SS values compiled among 26 independent 200 nm long channel devices has been performed. Both the average SS over 4 decades (SS_{avg}) and the minimum SS value (SS_{min}) are extracted and the statistical results are shown in Fig. 5f. Most of the devices have SS_{avg} values less than 60 mV dec^{-1} and SS_{min} values less than 40 mV dec^{-1}, demonstrating the excel-

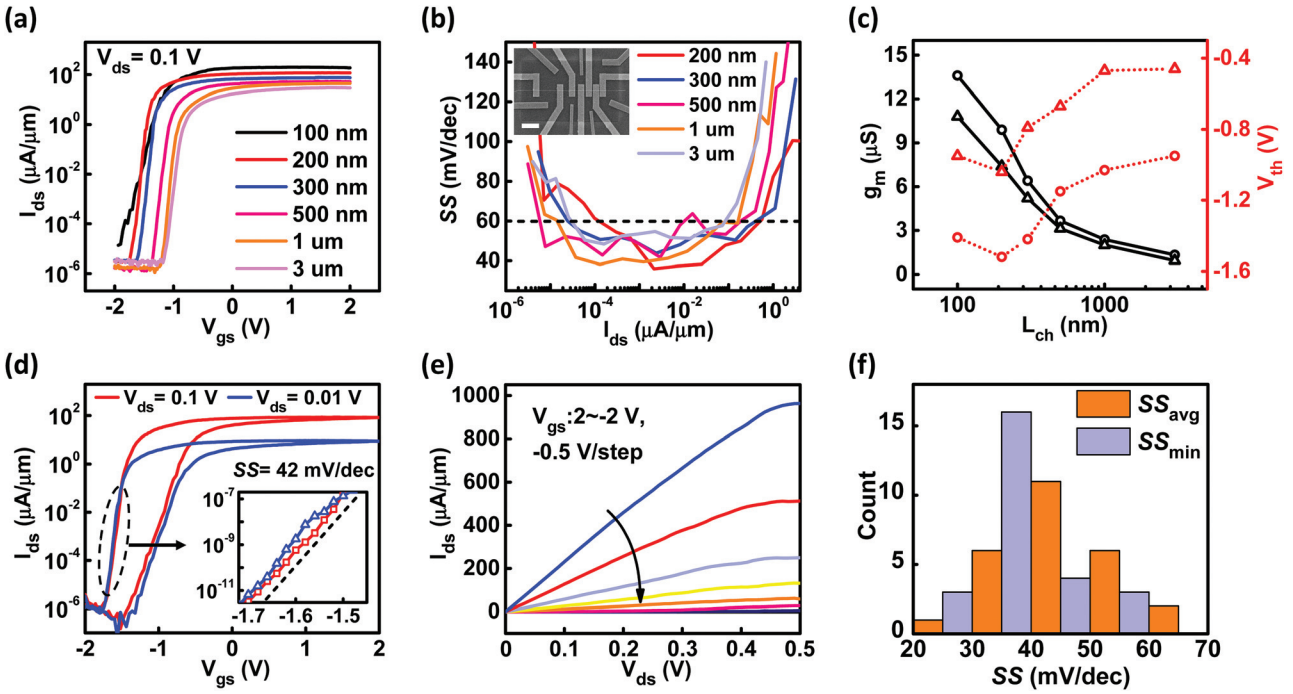

Fig. 5 Scaling-down behaviors and electrical performances of the self-aligned NC-FETs. (a) Transfer characteristics of the self-aligned In_2O_3 NW NC-FETs with L_{ch} values ranging from 100 nm to 3 μm, and the sweep speed is 0.08 V s^{-1}. The reverse sweeping curves are only displayed here for easy observation. (b) SS values as a function of the channel current density with various L_{ch} values. The SS values are extracted from the reverse sweeping transfer curves. The inset is the SEM image of the devices (with different channel lengths) assembled on a single NW, and the scale bar is 3 μm. (c) Detailed plots of g_m and the threshold voltage as a function of L_{ch}. The triangular and round symbols represent the forward and reverse sweeping directions, respectively. (d) Transfer characteristics of independent gate self-aligned In_2O_3 NW NC-FETs measured at room temperature, with V_{ds} of 0.1 V and 0.01 V. The channel length of the device is 200 nm and the V_{gs} sweep speed is 0.08 V s^{-1}. The device shows a counterclockwise hysteresis. The inset is the zoom-in graph of the subthreshold region during the reverse sweeping. (e) Output characteristics of the 200 nm channel In_2O_3 NW NC-FET. (f) Statistical results of the SS distribution of 200 nm channel devices, including the average SS over 4 decades (SS_{avg}) and the minimum SS value (SS_{min}). 26 devices were measured in total.

lent uniformity of our CVD growth In_2O_3 NWs as well as the admirable electrical stability of the short-channel NC-FET structure. All these results have explicitly demonstrated the superior device performance of the In_2O_3 NW NC-FETs as compared with the conventional top-gated MOSFETs with the same channel lengths (see Fig. S10 in the ESI†).

Conclusions

In summary, we have demonstrated the facile In_2O_3 NW NC-FETs with SS values less than 60 mV dec^{-1} at room temperature, which is aimed to break through the limitation caused by the "Boltzmann Tyranny". By simply introducing a ferroelectric P(VDF-TrFE) layer in the gated dielectric stacks, the fabricated devices can exhibit excellent modulation characteristics, including an exceptional on/off current ratio of larger than 10^7, a high saturation current density of 550 μA $μm^{-1}$, and an SS value less than 60 mV dec^{-1} for over 4 decades of channel current. Importantly, an inverter circuit has also been assembled with a voltage gain of 25 and a cut-off frequency of above 10 MHz, indicating the integration capabilities of NW NC-FETs developed here. The temperature and channel length dependent performances of these NC devices are as well investigated. When the channel length is scaled down to 200 nm in the self-aligned structure, the devices maintain excellent performances with a small average SS value of 42 mV dec^{-1} for more than 5 decades of I_{ds}, a large output current density of 960 μA $μm^{-1}$ and a low V_{th} at around −1.5 V. Although the SS_{for} value in the short channel devices has a little degradation due to the weakened ferroelectric gate coupling, the devices have still exhibited favorably high performance within a power budget. All these results have evidently illustrated the great potency of these In_2O_3 NC-FETs for substantial power reduction in future nanoelectronics.

Experimental

Nanowire synthesis

The single crystalline In_2O_3 NWs used in this work were synthesized in a horizontal tube furnace (Lindberg Blue M) *via* the chemical vapor deposition (CVD) approach. In_2O_3 powders and graphite powders were mixed well with a weight ratio of 10 : 1 and then put into the center of a quartz boat. Silicon substrates with 1 nm thick gold catalyst pre-deposited were

placed upside-down above the powder pile. Then, the quartz boat was inserted into the quartz tube reactor and heated to 1050 °C. The quartz tube was next heated for 1 hour under a constant flow of mixed gas (argon/oxygen = 100 : 1) at a flow rate of 200 sccm. When the system was cooled down to room temperature, a large amount of NWs was formed on the surface of the silicon substrates.

Device fabrication and characterization

First of all, a layer of a copolymer was spin-coated onto a p-type silicon substrate with a 100 nm thick thermally grown SiO_2 layer at a speed of 4000 rpm. Then, the sample was baked using a hot plate at 150 °C. Subsequently, the CVD grown In_2O_3 NWs were dispersed onto the substrate with a contact-printing method.[16] After that, PMMA 495 was spin-coated at 4000 rpm and baked at 150 °C. The external electrodes were later defined by e-beam lithography (IT300 with Raith), followed by metal deposition and lift-off. The equivalent oxide, the HfO_2 layer, was then deposited *via* ALD with a growth rate of 1.0 Å per cycle as follows. The sample chamber temperature is maintained at 95 °C during HfO_2 deposition. The tetrakis (dimethylamino)hafnium(IV) (TDMAH) precursor source was heated to 80 °C while the H_2O source was kept at room temperature. The flow rate of Ar carrier gas was set to 30 sccm. The pulse times for TDMAH and H_2O were kept at 0.1 s and 0.4 s, respectively, and the post-purge times were maintained at 100 s and 120 s, accordingly. The P(VDF-TrFE) solution was finally spin-coated onto the substrate at 2000 rpm and annealed at 130 °C for 30 min in order to obtain the desirable ferroelectric performance.

Electrical characterization

Electrical measurements of the In_2O_3 NC-FETs were performed on a probe station equipped with a Keysight B1500A semiconductor parameter analyzer operated under an ambient atmosphere. Similarly, low-temperature electrical measurements were performed with the Lake Shore TTPX Probe Station and the same Keysight B1500A semiconductor parameter analyzer. The output characteristics of the inverter circuit were evaluated using the DSO-X 2022a oscilloscope, while the AC signal is generated by using an Agilent 33210A arbitrary waveform generator.

Conflicts of interest

There are no conflicts to declare.

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