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Facile synthesis and growth mechanism of Ni-catalyzed GaAs nanowires on non-crystalline substrates

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Abstract
GaAs nanowires (NWs) have been extensively explored for next generation electronics, photonics and photovoltaics due to their direct bandgap and excellent carrier mobility. Typically, these NWs are grown epitaxially on crystalline substrates, which could limit potential applications requiring high growth yield to be printable or transferable on amorphous and flexible substrates. Here, utilizing Ni as a catalytic seed, we successfully demonstrate the synthesis of highly crystalline, stoichiometric and dense GaAs NWs on amorphous SiO_2 substrates. Notably, the NWs are found to grow via the vapor–solid–solid (VSS) mechanism with non-spherical NiGa catalytic tips and low defect densities while exhibiting a narrow distribution of diameter (21.0 ± 3.9 nm) uniformly along the entire length of the NW (>10 μm). The NWs are then configured into field-effect transistors showing impressive electrical characteristics with $I_{ON}/I_{OFF} > 10^3$, which further demonstrates the purity and crystal quality of NWs obtained with this simple synthesis technique, compared to the conventional MBE or MOCVD grown GaAs NWs.

S Online supplementary data available from stacks.iop.org/Nano/22/285607/mmedia

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Gallium arsenide (GaAs) nanowires (NWs) have attracted significant research attention in recent years as they are promising one-dimensional building blocks for future high performance electronics, photonics and photovoltaics due to their direct bandgap, high carrier mobility and unique length scale [1–4]. Many different methods have been extensively studied to prepare highly crystalline GaAs NWs, including the top-down etching approach [5], bottom-up solution-based growth [6], laser ablation [7], molecular beam epitaxy (MBE) [8] and metal–organic chemical vapor deposition (MOCVD) [9]. Among these, MBE and MOCVD methods are typically adopted following the well-known vapor–liquid–solid (VLS) and/or vapor–solid–solid (VSS) growth mechanisms [1, 9]; however, single-crystalline substrates such as GaAs wafers are usually employed as the underlying templates for the epitaxial growth of such NWs, which could limit their subsequent device integration for certain applications. For example, different kinds of NWs have been successfully demonstrated to print on receiver substrates for gigahertz circuitry on plastics and electronic skins [10–12]. In this regard, there is an urgent need to explore other alternative techniques for preparing highly crystalline GaAs NWs with high growth yield and controlled properties on non-crystalline substrates for technological applications [13, 14].

Importantly, in the typical VLS/VSS synthesis of NWs, gold (Au) nano-clusters (NCs) or particles are preferably

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used as the catalysts because of their relatively low eutectic melting temperature for alloying with the NW materials. Au, nevertheless, is not an ideal material and is well known to be incompatible with the conventional silicon (Si)-based CMOS technology as the resultant deep traps in Si greatly degrade the electrical properties [15, 16]. For this reason, other metals such as aluminum (Al) [15] and nickel (Ni) [17] have been investigated to substitute for Au for the VLS/VSS growth of Si and other NWs, while self-catalyzed and oxide-assisted growth of NWs is also explored [8, 18]. But there are still limited reports on the detailed synthesis and characterization of GaAs NWs utilizing catalysts other than Au NCs. A deep understanding of the growth mechanism is also of profound interest to further enhance the physical properties of GaAs NWs. Here, we demonstrate a facile and successful synthesis technique, utilizing Ni NCs, to prepare very dense GaAs NWs on amorphous Si/SiO_2 substrates. These grown NWs are found to follow the VSS mechanism with low defect densities, and they are very uniform in diameter, stoichiometric, and single crystalline with a smooth surface exhibiting good electrical performance when configured as field-effect transistors (FETs).

2. Experimental details

2.1. Synthesis of GaAs NWs

A dual-zone horizontal tube furnace, one zone for the solid source (upstream) and one zone for the sample substrate (downstream), was used as the reactor for the synthesis of GaAs NWs, as shown in the supporting information (figure S1 available at stacks.iop.org/Nano/22/285607/mmedia). At first, thermal evaporation was carried out with 99.995% pure Ni powders to deposit a 0.5 nm thick Ni film on Si/SiO_2 substrates (50 nm thermal grown) under a vacuum of $<5 \times 10^{-6}$ Torr. The processed substrate was then placed in the middle of the downstream zone with a tilt angle of $\sim 20^{\circ}$ and thermally annealed at 800 °C for 10 min in a hydrogen environment to obtain Ni NCs as the catalysts, similar to the technique reported in [17, 19]. The solid source, GaAs powders, were placed within a boron nitride crucible positioned in the upstream zone a distance of 10 cm from the sample. During the NW growth, the source was heated to the required source temperature (850–950 °C) while the substrate was cooled to the preset growth temperature (580–620 °C). Hydrogen (99.9995% purity) was used as the carrier gas to transport the thermally vaporized solid GaAs source downstream and the pressure was maintained at ∼1 Torr for the entire duration of the growth process. After the growth, the source and substrate heater were stopped together and cooled down to room temperature under the hydrogen flow. In this case, the grown NWs were chemically intrinsic without any intentional dopants.

2.2. Characterization of GaAs NWs

Surface morphologies of grown GaAs NWs were examined with a scanning electron microscope (SEM; FEI/Philips XL30) and transmission electron microscope (TEM; Philips CM-20). Crystal structures were determined by collecting x-ray diffraction (XRD) patterns on a Philips powder diffractometer using Cu Kα radiation ($\lambda = 1.5406$ Å), imaging with a high resolution TEM (JEOL 2100F) and selected area electron diffraction (SAED; Philips CM-20). Elemental mappings were performed using an energy dispersive x-ray (EDX) detector attached to the JEOL 2100F to measure the chemical composition of the grown NWs. For the elemental mapping and TEM, the GaAs NWs were first suspended in the ethanol solution by ultrasonication and drop-casted onto the grid for the corresponding characterization.

The GaAs NW FETs were fabricated by drop-casting the NW suspension onto highly doped p-type Si substrates with a 50 nm thermal grown gate oxide. Photolithography was utilized to define the source and drain regions and 50 nm thick Ni was thermally deposited as the contact electrodes followed by a lift-off process. The electrical performance of fabricated back-gated FETs was characterized with a standard electrical probe station and an Agilent 4155C semiconductor analyzer.

3. Results and discussion

3.1. High density NW growth

Based on the VLS/VSS growth mechanism, metallic Ga constituents would first alloy with Ni catalysts and the supersaturated Ga precipitates would next react with As (probably in the form of As_2 vapor) at the NC/NW interface leading to NW growth [20]; therefore, the substrate, source temperatures and precursor V/III ratio are the critical parameters for controlling the precursor transport and affecting the corresponding NW formation. In this study, as shown in figure 1(a), very dense, uniform, long (>10 μm) and relatively straight GaAs NWs are successfully obtained with substrate/source temperatures of 600 °C/900 °C, H_2 gas flow of 100 sccm (pressure $\sim$ 0.4 Torr) and a growth time of 30 min. At lower substrate temperatures (<580 °C), Ni NCs, formed in the annealing process, are far from the equilibrium liquid phase and only a minor portion of NCs can form NiGa alloy effectively due to the melting point lowering effect of nanomaterials [21], yielding a low density of NWs. At higher temperatures (>620 °C), as the congruent evaporation temperature of GaAs is ∼630 °C, As_2 has a much higher vapor pressure so that decomposition of the grown GaAs NWs is induced [22]. In this case, the solid solubility of Ga in Ni NCs also increases at such higher temperatures and this would further reduce the Ga supersaturation to lower the NW growth yield [23]; as a result, the optimal substrate temperature was observed at ∼600 °C (figure S2 available at stacks.iop.org/Nano/22/285607/mmedia). On the other hand, the source temperature was also varied between 850 and 950 °C. For lower source temperatures, there are inefficient precursors delivered for the NW growth, while for higher temperatures, more than sufficient precursors are evaporated (figure S3 available at stacks.iop.org/Nano/22/285607/mmedia) to induce the significant tapering and coating of NWs, which will degrade the NW device performance by lowering their gate coupling efficiencies [24, 25]. Based on the surface morphologies (figure S2 available at stacks.iop.org/

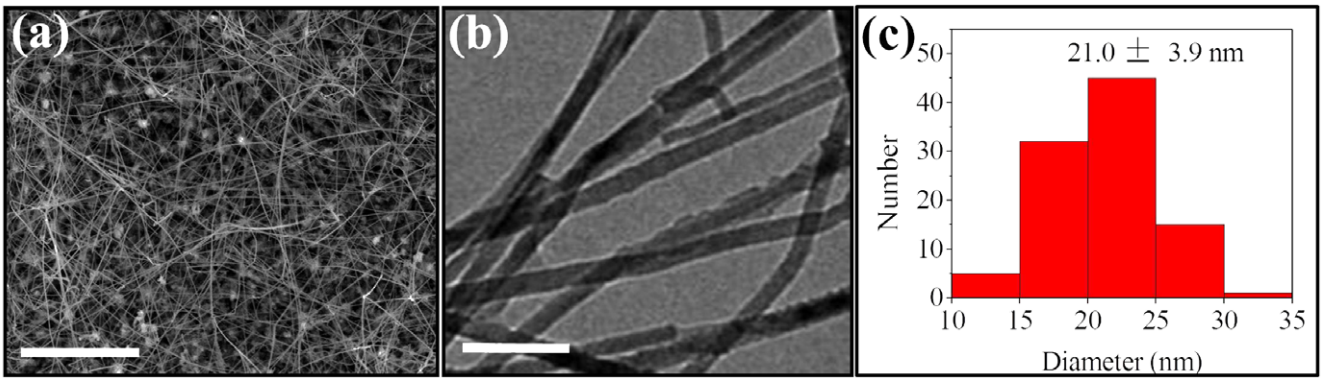

Figure 1. (a) SEM and (b) TEM images of GaAs NWs grown with the optimal condition. (c) Diameter statistics of 98 NWs observed in the corresponding TEM images. The scale bars of (a) and (b) are 2 μm and 50 nm, respectively. The grown NWs have a smooth surface and a narrow diameter distribution. (Optimal growth condition: substrate/source temperatures at 900/600 °C, H_2 flow at 100 sccm (pressure ∼0.4 Torr) and growth time for 30 min.)

Nano/22/285607/mmedia), a source temperature of 900 °C is found to be better than one of 950 °C for synthesizing GaAs NWs with a higher growth yield and fewer coatings.

It is well-known that the tapering and surface coating of GaAs NWs are mainly caused by the imbalance of the precursor V/III ratio supplied during the growth, while a higher V/III ratio is required for the formation of longer and more uniform NWs [26–28]. For this simple solid source CVD technique, the V/III ratio cannot be directly and independently controlled but can instead be tailored by adjusting the growth time and carrier gas flow together. According to the fundamental mechanism of GaAs solid source evaporation, there are three major steps involved: (1) dissociation of Ga and As atoms in the surface layer of the source powders; (2) As_2 vapor formation from surface As atoms and (3) partial evaporation of Ga atoms and partial residue as Ga liquid on the source surface [22]. When the growth is prolonged, the V/III ratio decreases gradually due to the persistent overpressure of As_2 vapor; therefore, less As_2 would react with Ga in the catalyst/NW interface for the NW formation [8, 29] and those excess Ga atoms would impinge onto and/or diffuse from the substrate to the NW surface as coatings and taper via the vapor–solid (VS) mechanism [30]. At the same time, a high gas flow or process pressure would reduce the mean free path of precursor molecules leading to more impingement of those molecules onto the NW surface and substrates; this would induce even faster dissipation of the V/III ratio to form more coatings and tapering (figure S4 available at stacks.iop.org/Nano/22/285607/mmedia). In this regard, our NWs were grown with a relatively low gas flow (100 sccm) and short growth time (30 min) to aim for reduced surface coatings (figure 1(b)) without sacrificing much on the NW length and density. To shed light to further confirm this coating formation, two separate NW growth procedures were performed with the same conditions except for a different growth time (figure S5 available at stacks.iop.org/Nano/22/285607/mmedia). Long and thin NWs are obtained with the short growth run while significant thicker NWs with coatings are yielded in the longer growth run, which strongly suggests depletion of the V/III ratio and both axial and lateral NW growth for the prolonged synthesis.

Importantly, the NW diameters are uniform along the nanowire and no tapering is observed, confirming the optimal control of processing parameters in our growth. Also, as depicted in figure 1(c), the NW diameters are determined to be 21.0 ± 3.9 nm from the statistics of 98 individual NWs from the TEM images. This narrow diameter distribution is remarkably good considering the simplicity of this growth technique as compared to the sophisticated MBE and MOCVD systems [8, 9] and the variation of commercially available colloidal Au nano-particles for growing small diameter NWs (∼10%).

3.2. Single-crystalline, stoichiometric GaAs NWs and the growth mechanism

The crystal quality and orientation of GaAs NWs were then studied by XRD and SAED as shown in figure 2. Based on the XRD spectrum, the cubic zinc blende (ZB) structure is observed with no peaks associated with the hexagonal wurtzite (WZ) structure. The corresponding SAED patterns (figures 2(b)–(d)) of representative NWs illustrate the single-crystalline quality and again confirmed the ZB structure of the NWs, which is consistent with the XRD results. However, a small fraction of NWs demonstrate WZ structure in the TEM and SAED characterization (data not shown), in which the signal is too weak to be detected by conventional XRD. This presence of the WZ structure is probably due to the preferential higher surface energy phase in nanomaterials [31]; further investigation is in progress to study the control of such crystal structures by tuning the growth parameters. Importantly, there is a low defect density associated with the NWs (TEM images) such that little twin planes or related defects are observed, which could be attributed to the successful control of the high V/III ratio and growth temperatures. It is also noted that no dominant growth axis was found. Most NWs studied by TEM grew along the ⟨111⟩ direction while few grew in other directions such as ⟨110⟩ and ⟨311⟩ with higher index planes. This is expected as low index planes have a lower surface energy which favors crystal growth during the formation of NWs [13, 32].

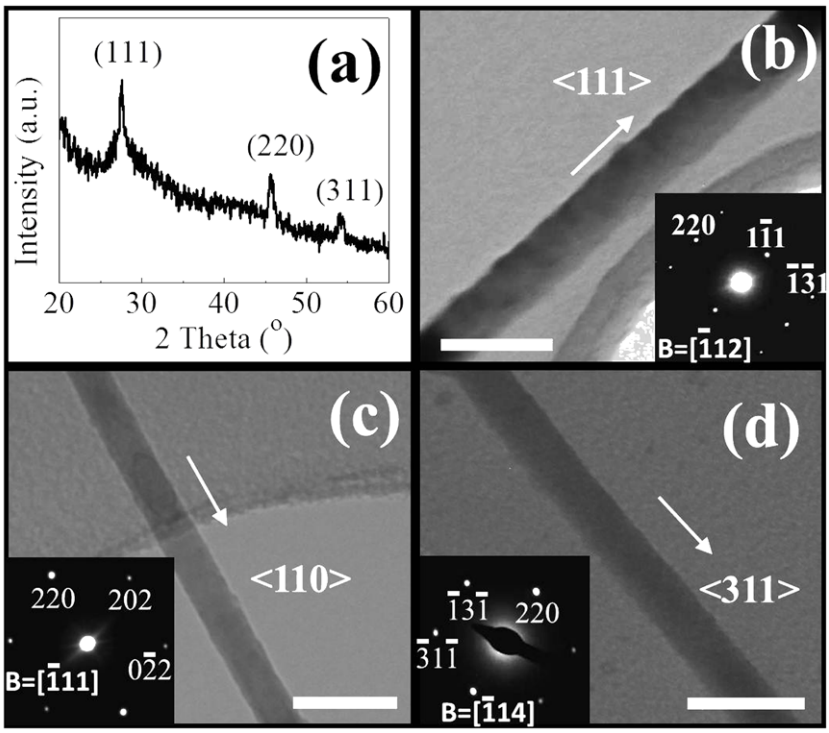

Figure 2. (a) XRD pattern and (b)–(d) the TEM and SAED of GaAs NWs grown at a source/substrate temperature of 900/600 °C with 100 sccm H_2 flow and 30 min growth. The scale bars of (b)–(d) are 50 nm. ZB structure is dominant for most NWs observed under both XRD and SAED characterization.

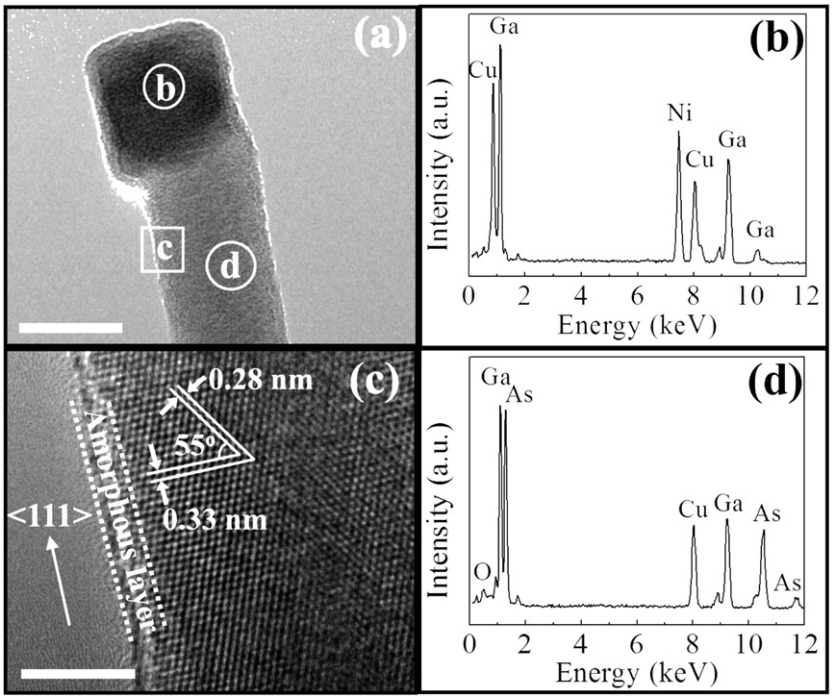

Figure 3. (a) TEM image of a GaAs NW grown at source/substrate temperature of 900/600 °C with 100 sccm H_2 flow and 30 min growth. (b) EDX spectrum of the catalyst tip. (c) The corresponding HRTEM image of the NW. (d) The EDX spectrum of the NW body. The scale bars of (a) and (c) are 20 and 5 nm, respectively. The non-spherical shape of the catalyst and elemental analysis verified a VSS growth mechanism. HRTEM shows the good crystallinity of the grown NWs.

Notably, as shown in figure 3(a), the Ni-based catalytic seeds can be clearly observed at the tips of most NWs, which are a distinct characteristic of the tip-based, VLS/VSS growth mechanism. Anyhow, there is still no general consensus on the confirmation of the growth mechanism (VLS versus VSS) among all the NW studies [33–36]. In order to further

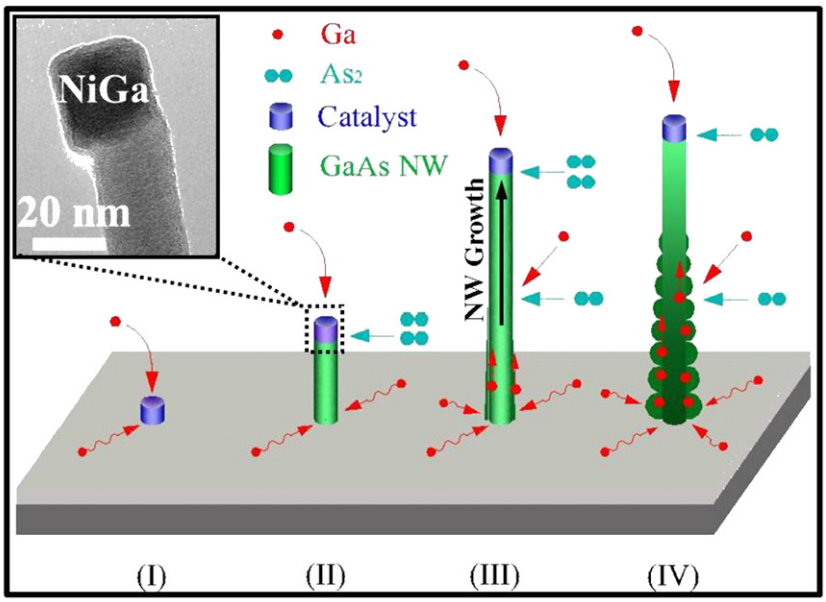

Figure 4. Schematic illustration of the VSS growth mechanism of Ni-catalyzed GaAs NWs in our studies. (I) NiGa alloy seeds are formed by the diffusion of Ga atoms into the Ni catalyst particles. (II) GaAs NWs are grown by supplying As_2 to the interface between the NW tip and body and then reacting with Ga from supersaturation in the catalytic tips. The non-spherical tips observed here indicate that the seeds remain in the solid state during the growth, which confirms the VSS mechanism. (III) As the growth continues, the V/III ratio decreases and more excess Ga atoms impinge or diffuse from the substrate surface to the NW surface to induce the radial NW growth, (IV) Significant radial NW growth results in heavy coating and/or tapering.

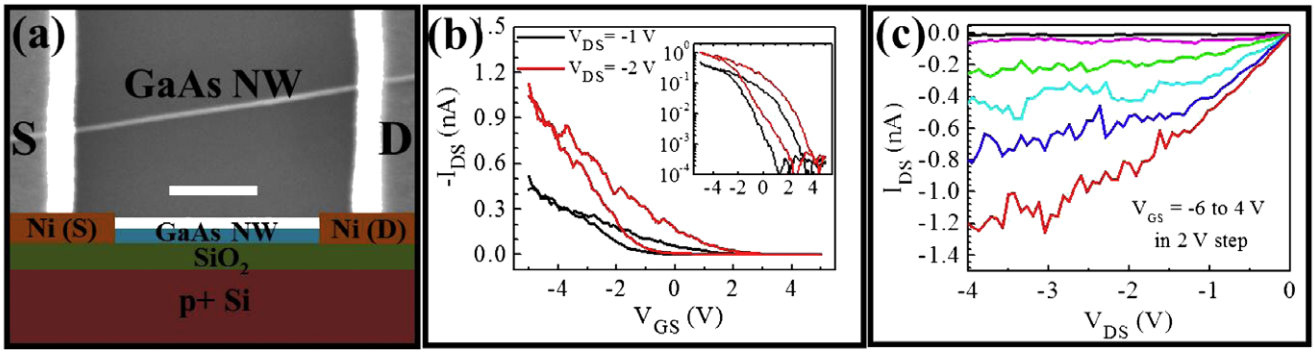

Figure 5. Electrical characterization of GaAs NWs. (a) A SEM image and schematic view of the back-gated NW FET fabricated with GaAs NWs grown at a source/substrate temperature of 900/600 °C with 200 sccm H_2 flow and 30 min growth; the scale bar is 500 nm. (b) I_{DS}–V_{GS} and (c) I_{DS}–V_{DS} curves of the representative FET. The I_{ON}/I_{OFF} ratio is found to be greater than 10^3.

explore the mechanism taking place in our growth, EDX elemental analysis with an electron beam size of 0.2 nm was performed on the tip (region b) to access the corresponding chemical composition. In the tip region (figure 3(b)), the only constituents are Ni and Ga with an atomic ratio of approximately 1:1; no As atoms is found, suggesting a stable NiGa alloy taking the role of the catalytic seed here. Based on the binary phase diagram between Ni and Ga, the NiGa alloy has a melting point of ∼1200 °C which is much higher than our growth temperature (∼600 °C) [37]; therefore, the catalyst tips are believed to exist as solid particles during NW growth. Moreover, as found in the TEM, crystalline square-like or cylindrical tips are typically observed in our synthesis which deviate significantly from the spherical seeds observed in the VLS mechanism [33, 36]. This observation has indicated that the seed particles are not present in the molten form and further confirms the VSS mode (figure 4) in our study, similar to the case reported for Au-catalyzed GaAs NW growth in MOCVD [9].

Following the VSS mechanism, the grown GaAs NWs have a 2–3 nm thick amorphous surface oxide layer as depicted in figure 3(c) and this layer thickness is consistent with the typical native oxide present on the surface of the bulk GaAs crystal. Based on the HRTEM image, the distances between the adjacent lattice planes are found to be 0.28 and 0.33 nm, which are in good agreement with the plane spacing of {200} and {111} families in the ZB structure. Also, the EDX elemental mapping gives a Ga/As atomic ratio close to 1:1 with around 7% oxygen in the overall composition (figure 3(d)), where this low oxygen content probably comes from the

surface oxide layer [38]. All these suggest the grown NWs are highly crystalline and stoichiometric with a low structural defect density.

3.3. Electrical performance of NW FETs

In order to characterize the electrical properties of the Ni-catalyzed GaAs NWs, FETs were fabricated using Ni (∼50 nm) source/drain (S/D) metal contacts in a common back-gated configuration (50 nm thermal oxide as the gate dielectric and a heavily boron doped Si substrate as the gate). Figure 5 illustrates the electrical properties of a representative FET with an individual GaAs NW as the channel material with a diameter of ∼20 nm (including the surface oxide layer) and a channel length of ∼2 μm. As shown in figures 5(b) and (c), the transistor exhibits p-type conduction and shows a minimal hysteresis with an ON current $I_{ON} \sim -1.2$ nA at $V_{DS} = -4$ V and $V_{GS} = -6$ V. This p-type characteristic is probably attributable to the unintentional doping of residual carbon existing in the growth system [39]; further investigation is ongoing. Further enhancement of the ON current could be achieved in the future by incorporating p-type dopants like carbon or zinc during the growth and utilizing better electrical contacts such as a Au/Zn/Au metal stack for p-type GaAs [40] in order to eliminate the Fermi level pinning (∼0.48 eV above the conduction band of p-GaAs) [41]. Importantly, this device exhibits a respectable $I_{ON}/I_{OFF} > 10^3$ as depicted in figure 5(b), (inset) at $V_{DS} = -2$ V and this excellent gate coupling (even in the back-gated device structure) and low OFF-state leakage demonstrate well the potency of GaAs NWs for high performance electronic devices.

4. Conclusions

In summary, we have demonstrated a simple technique to synthesize highly crystalline and stoichiometric GaAs NWs on non-crystalline substrates via the VSS mechanism with non-spherical NiGa catalytic tips by utilizing Ni NCs as the starting catalyst. This is shown to serve as an effective catalytic material which leads to the high crystal quality and high growth yield of GaAs NWs with uniform diameters. Notably, these NWs are grown with a low defect density and minimized surface coatings which enable high performance NW devices with $I_{ON}/I_{OFF} > 10^3$. All these enhanced properties may have significant implications for GaAs NWs for various future technological applications.

Acknowledgments

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References

[1] Gudiksen M S, Lauhon L J, Wang J, Smith D C and Lieber C M 2002 Growth of nanowire superlattice structures for nanoscale photonics and electronics *Nature* **415** 617–20
[2] Yan R X, Gargas D and Yang P D 2009 Nanowire photonics *Nat. Photon.* **3** 569–76
[3] Woodall J M 1980 III–V compounds and alloys—an update *Science* **208** 908–15
[4] Yoon J *et al* 2010 GaAs photovoltaics and optoelectronics using releasable multilayer epitaxial assemblies *Nature* **465** 329–34
[5] Sun Y G and Rogers J A 2004 Fabricating semiconductor nano/microwires and transfer printing ordered arrays of them onto plastic substrates *Nano Lett.* **4** 1953–9
[6] Yu H and Buhro W E 2003 Solution-liquid–solid growth of soluble GaAs nanowires *Adv. Mater.* **15** 416–9
[7] Morales A M and Lieber C M 1998 A laser ablation method for the synthesis of crystalline semiconductor nanowires *Science* **279** 208–11
[8] Colombo C, Spirkoska D, Frimmer M, Abstreiter G and Morral A F I 2008 Ga-assisted catalyst-free growth mechanism of GaAs nanowires by molecular beam epitaxy *Phys. Rev.* B **77** 155326
[9] Persson A I, Larsson M W, Stenstrom S, Ohlsson B J, Samuelson L and Wallenberg L R 2004 Solid-phase diffusion mechanism for GaAs nanowire growth *Nat. Mater.* **3** 677–81
[10] Takahashi T, Takei K, Adabi E, Fan Z Y, Niknejad A M and Javey A 2010 Parallel array InAs nanowire transistors for mechanically bendable, ultrahigh frequency electronics *ACS Nano* **4** 5855–60
[11] Fan Z Y, Ho J C, Jacobson Z A, Yerushalmi R, Alley R L, Razavi H and Javey A 2008 Wafer-scale assembly of highly ordered semiconductor nanowire arrays by contact printing *Nano Lett.* **8** 20–5
[12] Takei K, Takahashi T, Ho J C, Ko H, Gillies A G, Leu P W, Fearing R S and Javey A 2010 Nanowire active-matrix circuitry for low-voltage macroscale artificial skin *Nat. Mater.* **9** 821–6
[13] Fortuna S A, Wen J G, Chun I S and Li X L 2008 Planar GaAs nanowires on GaAs (100) substrates: self-aligned, nearly twin-defect free, and transfer-printable *Nano Lett.* **8** 4421–7
[14] Fan Z Y, Ho J C, Takahashi T, Yerushalmi R, Takei K, Ford A C, Chueh Y L and Javey A 2009 Toward the development of printable nanowire electronics and sensors *Adv. Mater.* **21** 3730–43
[15] Wang Y W, Schmidt V, Senz S and Gosele U 2006 Epitaxial growth of silicon nanowires using an aluminium catalyst *Nat. Nanotechnol.* **1** 186–9
[16] Renard V T, Jublot M, Gergaud P, Cherns P, Rouchon D, Chabli A and Jousseaume V 2009 Catalyst preparation for CMOS-compatible silicon nanowire synthesis *Nat. Nanotechnol.* **4** 654–7
[17] Ford A C, Ho J C, Fan Z Y, Ergen O, Altoe V, Aloni S, Razavi H and Javey A 2008 Synthesis, contact printing, and device characterization of Ni-catalyzed, crystalline InAs nanowires *Nano Res.* **1** 32–9
[18] Shi W S, Zheng Y F, Wang N, Lee C S and Lee S T 2001 A general synthetic route to III–V compound semiconductor nanowires *Adv. Mater.* **13** 591–4
[19] Ford A C, Ho J C, Chueh Y L, Tseng Y C, Fan Z Y, Guo J, Bokor J and Javey A 2009 Diameter-dependent electron mobility of InAs nanowires *Nano Lett.* **9** 360–5
[20] Zhang G Q, Tateno K, Sanada H, Tawara T, Gotoh H and Nakano H 2009 Synthesis of GaAs nanowires with very small diameters and their optical properties with the radial quantum-confinement effect *Appl. Phys. Lett.* **95** 123104
[21] Roduner E 2006 Size matters: why nanomaterials are different *Chem. Soc. Rev.* **35** 583–92
[22] Goldstein B, Szostak D J and Ban V S 1976 Langmuir evaporation from (100), (111a), and (111b) faces of GaAs *Surf. Sci.* **57** 733–40

[23] Dayeh S A, Soci C, Bao X Y and Wang D L 2009 Advances in the synthesis of InAs and GaAs nanowires for electronic applications *Nano Today* **4** 347–58
[24] Zhao X W, Hauser A J, Lemberger T R and Yang F Y 2007 Growth control of GaAs nanowires using pulsed laser deposition with arsenic over-pressure *Nanotechnology* **18** 485608
[25] Hong W K, Song S, Hwang D K, Kwon S S, Jo G, Park S J and Lee T 2008 Effects of surface roughness on the electrical characteristics of ZnO nanowire field effect transistors *Appl. Surf. Sci.* **254** 7559–64
[26] Joyce H J *et al* 2009 Unexpected benefits of rapid growth rate for III–V nanowires *Nano Lett.* **9** 695–701
[27] Joyce H J *et al* 2008 High purity GaAs nanowires free of planar defects: growth and characterization *Adv. Funct. Mater.* **18** 3794–800
[28] Plante M C and LaPierre R R 2008 Control of GaAs nanowire morphology and crystal structure *Nanotechnology* **19** 495603
[29] Borgstrom M T, Immink G, Ketelaars B, Algra R and Bakkers E P A M 2007 Synergetic nanowire growth *Nat. Nanotechnol.* **2** 541–4
[30] Krylyuk S, Davydov A V and Levin I 2010 Tapering control of Si nanowires grown from $SiCl_4$ at reduced pressure *ACS Nano* **5** 656–64
[31] Dick K A, Caroff P, Bolinsson J, Messing M E, Johansson J, Deppert K, Wallenberg L R and Samuelson L 2010 Control of III–V nanowire crystal structure by growth parameter tuning *Semicond. Sci. Technol.* **25** 024009
[32] Ihn S G, Song J I, Kim T W, Leem D S, Lee T, Lee S G, Koh E K and Song K 2007 Morphology- and orientation-controlled gallium arsenide nanowires on silicon substrates *Nano Lett.* **7** 39–44
[33] Wu Y Y and Yang P D 2001 Direct observation of vapor–liquid–solid nanowire growth *J. Am. Chem. Soc.* **123** 3165–6
[34] Kodambaka S, Tersoff J, Reuter M C and Ross F M 2007 Germanium nanowire growth below the eutectic temperature *Science* **316** 729–32
[35] Zhang Z, Shimizu T, Chen L, Senz S and Gosele U 2009 Bottom-imprint method for VSS growth of epitaxial silicon nanowire arrays with an aluminium catalyst *Adv. Mater.* **21** 4701–5
[36] Hofmann S *et al* 2008 Ledge-flow-controlled catalyst interface dynamics during Si nanowire growth *Nat. Mater.* **7** 372–5
[37] Massalski T, Okamoto H, Subramanian P and Kacprzak L 1990 *Binary Alloy Phase Diagrams* vol 3 (Materials Park, OH: ASM International)
[38] Ghita R V, Negrila C, Manea A S, Logofatu C, Cernea M and Lazarescu M F 2003 X-ray photoelectron spectroscopy study on n-type GaAs *J. Optoelectron. Adv. Mater.* **5** 859–63
[39] Calawa A R 1978 Effect of H_2 on residual impurities in GaAs MBE layers *Appl. Phys. Lett.* **33** 1020–2
[40] Sanada T and Wada O 1980 Ohmic contacts to p-GaAs with Au/Zn/Au structure *Japan. J. Appl. Phys.* **19** L491–4
[41] Mead C A 1966 Metal–semiconductor surface barriers *Solid-State Electron.* **9** 1023–33