BHARAT ACHARYA EDUCATION
Cell: 98204 08217
BharatSir@hotmail.com

DELAYS AND DELAY ROUTINES

Delays in a computer system can be of two types:
1) Hardware delays
2) Software delays

	HARDWARE DELAYS	SOFTWARE DELAYS
1	Caused by external hardware (Timer IC like 8254)	Caused by a software delay routine (program)
2	μP is not involved in causing the delay and hence is free for other applications.	μP is busy as it is executing the delay routine so cannot be used otherwise.
3	Multiple delay routines are possible	Multiple delay routines are not possible
4	Flexibility is low as h/w is involved.	Flexibility is high as delay caused by s/w.
5	External h/w required so ckt. becomes more complex and expensive	External h/w not required so ckt. is simple and less expensive

SOFTWARE DELAYS

Software delays are produced in programs by one of the various software **"Delay Routines"**.

As the amount of delay required varies from application to application different types of delay routines are present, as follows:

1) Using NOP Instruction
2) Using One 8-bit register
3) Using One 16-bit register
   (Nested delay routines):
4) Using Two 8-bit registers
5) Using One 8-bit register and One 16-bit register
6) Using Two 16-bit registers

1) Using NOP Instruction

Eg: NOP;

1-byte instruction
Opcode fetch --- 4 T-states.
T_D = 4T.
T = 1/(Clk freq)
∴ assuming 8085 working at 3 MHz, T = 1/(3 MHz) = 0.333 μ sec.
∴ T_D = 4 × 0.333 = 1.332 μ sec.

∴ T_D = 1.332 μ sec.
This is the maximum delay that can be achieved by writing a NOP instruction.

2) Using One 8-bit register

Delay:	**MVI B**, 8-bit count	7T
Loop:	**DCR B**	4T
	JNZ Loop	10/7T
	RET	10T

NT MT

T_D = MT + [(Count)$_d$ × NT] – 3T

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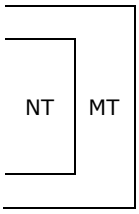
NT = No of T-states inside the loop {here NT = 10T + 4T = **14T**}
MT = No of T-states outside the loop {here MT = 7T + 10T = **17T**}
$Count_{max}$ = 255 {8-bit count in decimal}

$\therefore T_{D\,max}$ = 17T + [255 × 14T] – 3T
$\therefore T_{D\,max}$ = 3584T.
assuming 8085 working at 3 MHz i.e. T = 333 n sec.

$\therefore$ **$T_{D\,max}$ = 1.18 m sec.**

3) Using One 16-bit register

Delay:	**LXI B**, 16-bit count	10T
Loop:	**DCX B**	6T
	MOV A, C	4T
	ORA C	4T
	JNZ Loop	10/7T
	RET	10T



T_D = MT + [$(Count)_d$ × NT] – 3T

here **NT** = 6T + 4T + 4T + 10T = **24T**
MT = 10T + 10T = **20T**

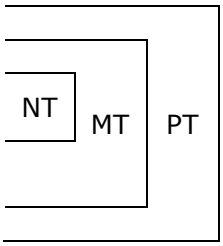
$Count_{max}$ = 65535 {16-bit count in decimal}

$\therefore T_{D\,max}$ = 20T + [65535 × 24T] – 3T
$\therefore T_{D\,max}$ = 1572057T.
assuming 8085 working at 3 MHz i.e. T = 333 n sec.

$\therefore$ **$T_{D\,max}$ = 0.525 sec.**

4) Using Two 8-bit registers

Delay:	**MVI C**, Count2	7T
Loop2:	**MVI B**, Count1	7T
Loop1:	**DCR B**	4T
	JNZ Loop1	10/7T
	DCR C	4T
	JNZ Loop2	10/7T
	RET	10T



T_D = PT + [$(Count2)_d$ × T_{loop1}] – 3T
T_{loop1} = MT + [$(Count1)_d$ × NT] – 3T

NT = No of T-states inside loop1 {here NT = 4T + 10T = **14T**}.
MT = No of T-states outside loop1 but inside loop2 {MT = 7T + 4T + 10T= **17T**}
PT = No of T-states outside loop2 {here PT = 10T + 7T = **17T**}.
$Count1_{max}$ = 255 {8-bit count in decimal}
$Count2_{max}$ = 255 {8-bit count in decimal}

$\therefore T_{D\,max}$ = 914954T.
assuming 8085 working at 3 MHz i.e. T = 333 n sec.

$\therefore$ **$T_{D\,max}$ = 0.304 sec.**

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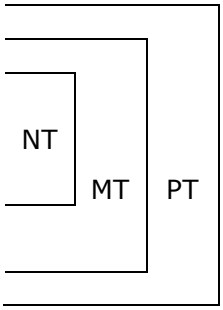
5) Using One 8-bit register and One 16-bit register

Delay:	**MVI D**, Count2	7T
Loop2:	**LXI B**, Count1	10T
Loop1:	**DCX B**	6T
	MOV A, C	4T
	ORA B	4T
	JNZ Loop1	10/7T
	DCR D	4T
	JNZ Loop2	10/7T
	RET	10T



$\mathbf{T_D = PT + [(Count2)_d \times T_{loop1}] - 3T}$
$\mathbf{T_{loop1} = MT + [(Count1)_d \times NT] - 3T}$

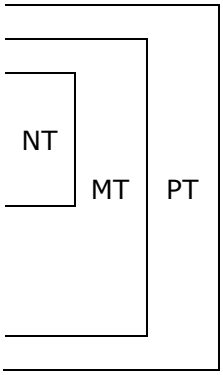
Here **NT** = 6T + 4T + 4T + 10T = **24T**.
MT = MT = 10T + 4T + 10T = **24T**.
PT = 7T + 10T = **17T**.
$Count1_{max}$ = 65535 {16-bit count in decimal}
$Count2_{max}$ = 255 {8-bit count in decimal}

assuming 8085 working at 3 MHz i.e. T = 333 n sec.

∴ $\mathbf{T_{D\ max}}$ **= 133.69 sec.**

6) Using Two 16-bit registers

Delay:	**LXI B**, Count2	10T
Loop2:	**LXI D**, Count1	10T
Loop1:	**DCX D**	6T
	MOV A, E	4T
	ORA D	4T
	JNZ Loop1	10/7T
	DCX B	6T
	MOV A, C	4T
	ORA B	4T
	JNZ Loop2	10/7T
	RET	10T



$\mathbf{T_D = PT + [(Count2)_d \times T_{loop1}] - 3T}$
$\mathbf{T_{loop1} = MT + [(Count1)_d \times NT] - 3T}$

Here **NT** = 6T + 4T + 4T + 10T = **24T**.
MT = MT = 10T + 6T + 4T + 4T + 10T = **34T**.
PT = 10T + 10T = **20T**.
$Count1_{max}$ = 65535 {16-bit count in decimal}
$Count2_{max}$ = 65535 {16-bit count in decimal}

assuming 8085 working at 3 MHz i.e. T = 333 n sec.

∴ $\mathbf{T_{D\ max}}$ **= 9 hours, 32 min, 24 sec.**

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Summary:

Delay Method	Max duration
NOP	1.332 μ sec
One 8-bit register	1.18 m sec
One 16-bit register	.525 sec
Two 8-bit registers	.304 sec
One 8-bit / one 16-bit reg	133.69 sec
Two 16-bit register	9 hrs, 32 min, 24 sec

Please Note: *All these calculations are w.r.t. 8085 operating at 3 MHz.*
In case in the exam, the frequency is different then calculate 1T = 1/(Clk. freq.), and then calculate the appropriate delay. ☺ In case of doubts, contact Bharat Sir: - 98204 08217.