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8259

PROGRAMMABLE INTERRUPT CONTROLLER

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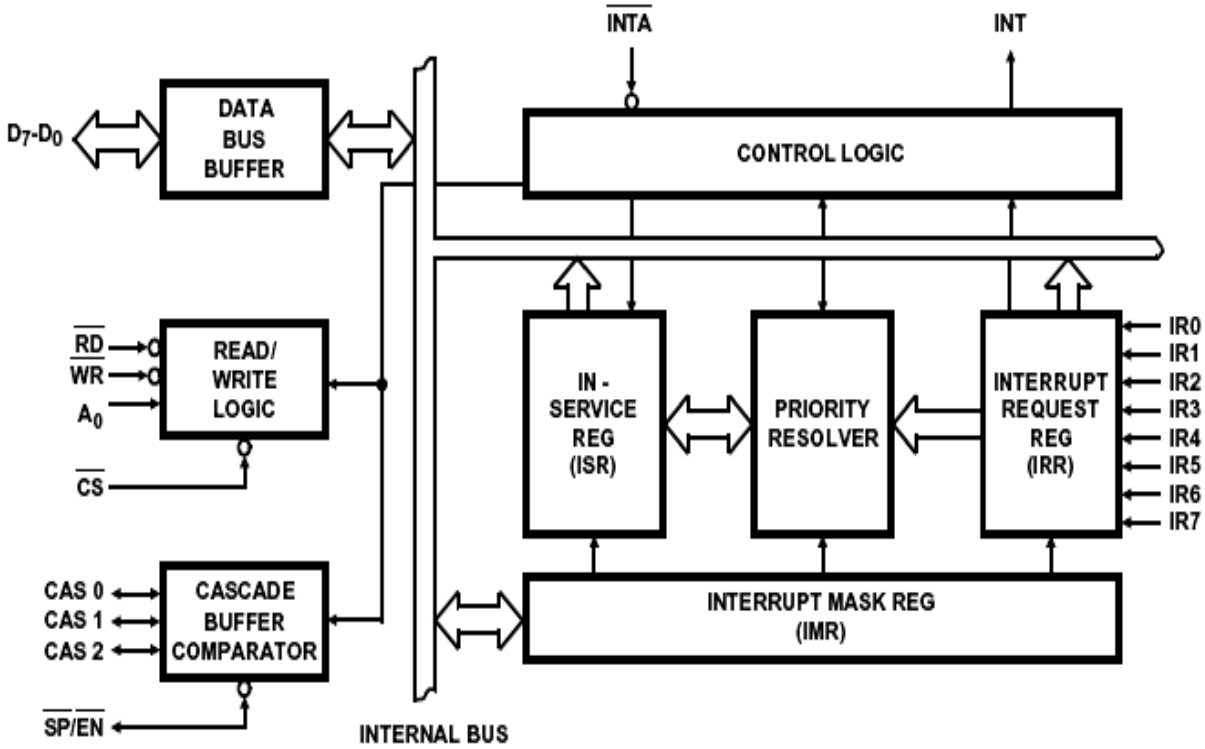
Salient Features of 8259 PIC

- 8259 is a **Programmable Interrupt Controller** (PIC) designed to work with **8085**, **8086** etc.
- A **single 8259** can handle **8 interrupts,** while a **cascaded** configuration of 8 slave 8259's and 1 master 8259 can handle **64 interrupts**.
- 8259 can **handle edge** as well as **level triggered** interrupts.
- 8259 has a **flexible priority** structure.
- In 8259 interrupts can be **masked** individually.
- The **Vector address** of the interrupts is **programmable**.
- Status of interrupts (pending, In-service, masked) can be easily read by the µP.

Architecture of 8259



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The architecture of 8259 can be divided into the following parts:

1) Interrupt Request Register (IRR)
- 8259 has **8 interrupt** input lines **IR_7 ... IR_0**.
- The IRR is an **8-bit register** having **one bit** for **each** of the **interrupt** lines.
- When an **interrupt request** occurs on any of these lines, the **corresponding bit** is **set** in the Interrupt Request Register (**IRR**).

2) In-Service Register (InSR)
- It is an **8-bit** register, which **stores** the **level** of the Interrupt Request, which is **currently** being **serviced**.

3) Interrupt Mask Register (IMR)
- It is an **8-bit** register, which stores the **masking pattern** for the interrupts of 8259. It stores **one bit per interrupt level**.

4) Priority Resolver
- It **examines** the **IRR**, **InSR**, and **IMR** and determines which interrupt is of **highest priority** and should be sent to the µP.

5) Control Logic
- It has **INT output** signal **connected to** the **INTR** of the µP, to **send** the **Interrupt** to the µP.
- It also has the **INTA input** signal **connected to** the **INTA** of the µP, to **receive** the interrupt **acknowledge**.
- It is also used to control the remaining blocks.

6) Data Bus Buffer
- It is a bi-directional buffer used to **interface** the internal **data bus** of 8259 with the external (system) data bus.

7) Read/Write Logic
- It is used to accept the RD, WR, A_0 and CS signal.
- It also holds the Initialization Command Words (ICW's) and the Operational Command Words (OCW's).

8) Cascade Buffer / Comparator
- It is used in **cascaded mode** of operation.
- It has two components:

i. CAS_2, CAS_1, CAS_0 lines:
- These lines are **output for the master**, **input for the slave**.
- The **Master sends** the **address of** the **slave** on these lines (hence output).
- The **Salves read** the **address** on these lines (hence input).
- As there are 8 interrupt levels for the Master, there are **3 CAS lines ($\because$ $2^3 = 8$).**

ii. SP/EN (Slave Program/Master Enable):
- In **Buffered Mode**, it **functions** as the **EN line** and is used to **enable** the **buffer**.
- In **Non buffered mode**, it **functions** as the **SP output line**.
- **For Master** 8259 **SP** should be **high**, and **for** the **Slave SP** should be **low**.