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Interfacing and Interrupt Sequence for CASCADED 8259

- When **more than one 8259s** are connected to the µP, it is called as a **Cascaded configuration**.
- A Cascaded configuration **increases** the **number of interrupts** handled by the system.
- As the **maximum** number of **8259s** interfaced can be **9** (1 Master and 8 Slaves) the **Maximum** number of **interrupts** handled can be **64**.
- The **master 8259** has **SP/EN = +5V** and the **slave** has **SP/EN = 0V**.
- **Each slave's INT** output is **connected** to the **IR input** of the **Master**.
- The **INT** output **of** the **Master** is **connected** to the **INTR** input of the **µP**.
- The **master addresses** the individual **slaves through** the **CAS_2, CAS_1, CAS_0 lines** connected from the master to each of the slaves.
- **Each 8259** (Master or Slave) **has** its **own address** and **has to be initialized separately**.

When an **interrupt request** occurs **on** a **SLAVE**, the **following sequence** of events is executed:

1) The **slave 8259 resolves** the **priority** of the interrupt and **sends** the **interrupt to** the **master** 8259.
2) The **master resolves** the **priority** among its slaves and **sends** the **interrupt to** the **µP**.
3) The **µP finishes the current instruction** and **responds** to the interrupt **by sending 3 INTA pulses**.
4) **In response to the first INTA pulse** the **master does** the **following** tasks:
   i. It **sends** the **opcode** of **CALL** instruction **to** the **µP** on the data bus.
   ii. It **sends** the **3-bit salve identification number** on the **CAS lines**.
   iii. The **Master sets** the **corresponding bit** in **its InSR**.
   iv. The **Slave identifies** its number on the **CAS lines** and **sets** the **corresponding bit in its InSR**.
5) In **response to** the **second and third INTA** pulse the **slave** places the **lower byte and** then the **higher byte of** the **ISR address** on the data bus **respectively**.
6) **During** the **third INTA** pulse the **InSR bit** of the **slave** is **cleared** in **AEOI mode**, **otherwise** it is **cleared by** the **EOI command** at the end of the ISR.
7) The **µP pushes** the contents of **PC onto** the **Stack** and **transfers program** to the **address of** the **ISR sent by** the **slave** 8259. **The ISR thus begins**.

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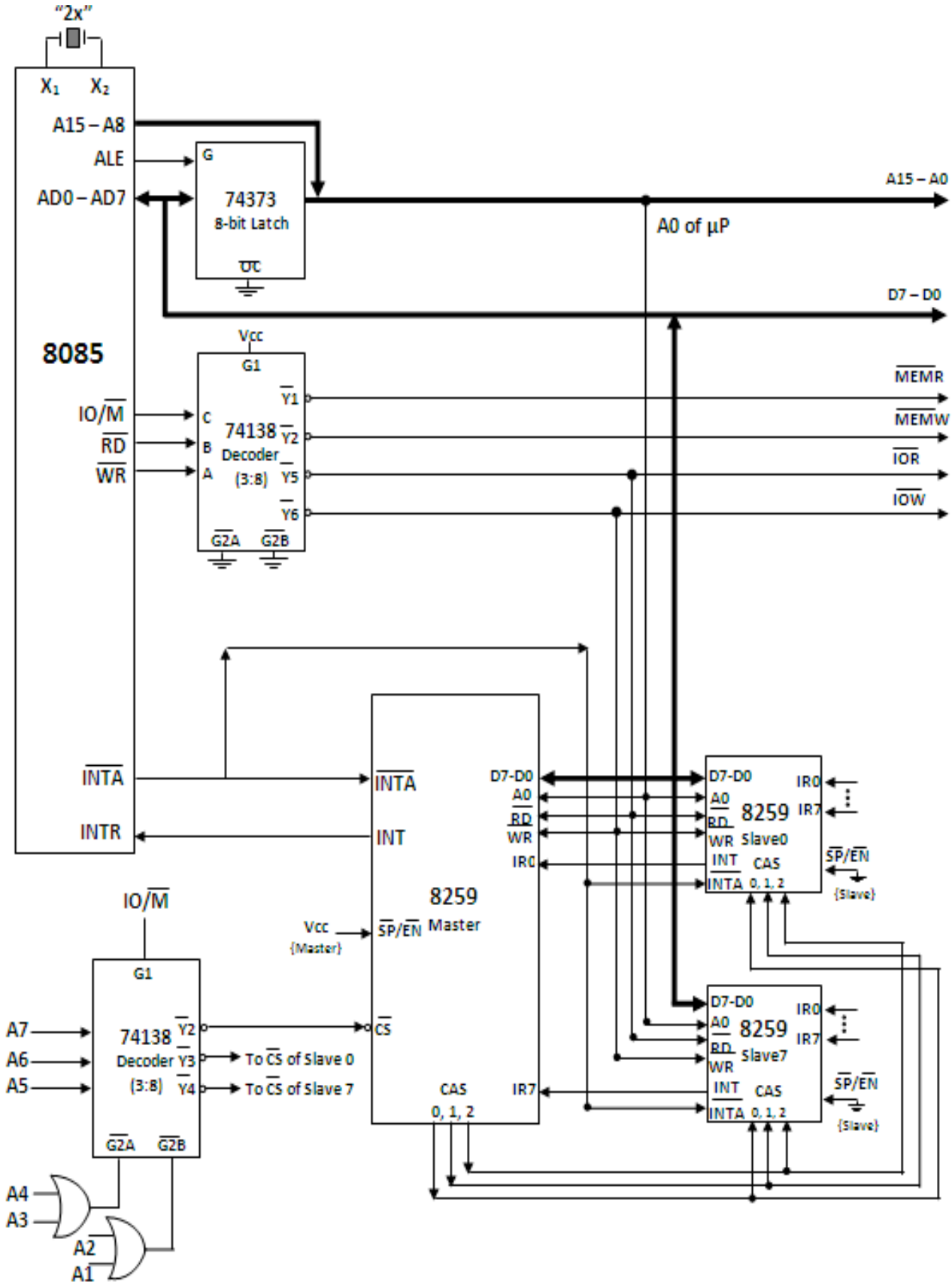

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I/O for the Cascaded Configuration

I/O Chip	Address Bus								I/O port Address
	A7	A6	A5	A4	A3	A2	A1	A0	
8259 Master									
ICW1	**0**	**1**	**0**	0	0	0	0	**0**	**40 H**
ICW2	**0**	**1**	**0**	0	0	0	0	**1**	**41 H**
8259 Slave 0									
ICW1	**0**	**1**	**1**	0	0	0	0	**0**	**60 H**
ICW2	**0**	**1**	**1**	0	0	0	0	**1**	**61 H**
8259 Slave 7									
ICW1	**1**	**0**	**0**	0	0	0	0	**0**	**80 H**
ICW2	**1**	**0**	**0**	0	0	0	0	**1**	**81 H**