

End Semester Examination (5th sem), 2021

- Subject Name : → Microprocessor and Micro Controller.
- Subject Code : → IT3101
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- Number of sheets uploaded : → 13 .

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5)

a) After Execution of each instruction the values are : →

| Initial    | A    | B  | C    | D  | E  | H  | L  | 1000 | 1001 | 1002 | 1003 | 1004 |
|------------|------|----|------|----|----|----|----|------|------|------|------|------|
| Initial    | 35   | 28 | 41   | 10 | 02 | 25 | 00 | 27   | 25   | 37   | 41   | 56   |
| LDAX D     | (37) | 28 | 41   | 10 | 02 | 25 | 00 | 27   | 25   | 37   | 41   | 56   |
| XCHG       | 37   | 28 | 41   | 25 | 00 | 10 | 02 | 27   | 25   | 37   | 41   | 56   |
| MVI M, 56H | 37   | 28 | 41   | 25 | 00 | 10 | 02 | 27   | 25   | (56) | 41   | 56   |
| MVI A, 25H | (25) | 28 | 41   | 25 | 00 | 10 | 02 | 27   | 25   | 56   | 41   | 56   |
| MOV C, D   | 25   | 28 | (25) | 25 | 00 | 10 | 02 | 27   | 25   | 56   | 41   | 56   |

b) The assembly code to transfer entire block of data to 8070H from 8050H is : →

```

LXI 8050H
LXI 8070H
MVI B, 10H
loop: MOV A, M
      STAX D
      INX H
      INX D
      DCR B
      JNZ LOOP
      HLT
  
```

(2)

(a) Difference between Compare and Subtract instruction in 8085: →

In Subtract instruction the final result is placed in accumulator.

~~for comp~~

Example: → SUB B

It updates the A with  $A - B$ .

$$A \leftarrow A - B$$

In compare instruction, accumulator does not store the final result it just compares the result with the accumulator so accumulator contents will not get updated.

Example: → CMP B.

checks if  $A > B$  or not

(b.) CALL Instruction: →

Mnemonics: →

LXI SP, 8100H. → initialize the stack pointer at 8100H.

SP ← 8100H.

CALL 8050H → call the subroutine located at 8050H.

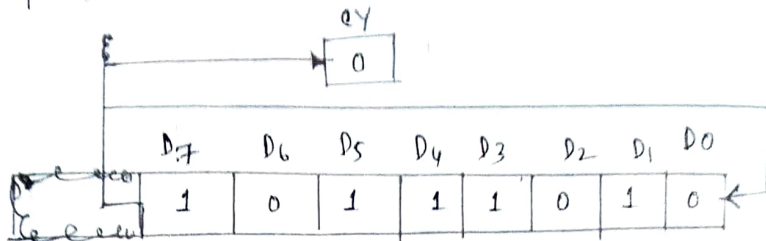
RET [returns the execution in main program].

Explanation

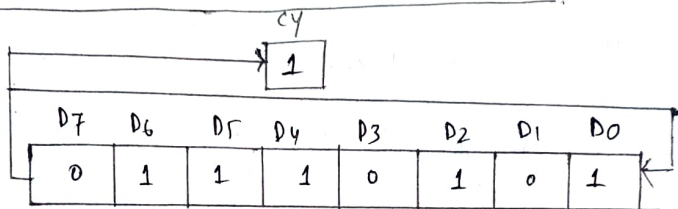
(c.)

$A = B AH$

$CY = 0$

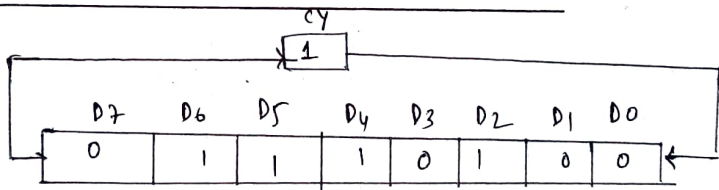


After Execution of a (RLC instruction):



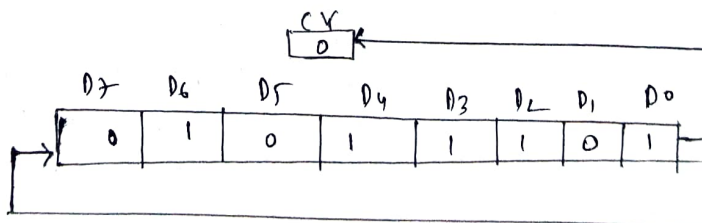
$A = 75H, CY = 1$

After Execution of b (RAL instruction):



$A = 74H, CY = 1$

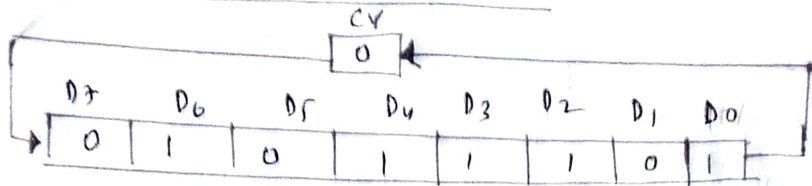
After Execution of c (RRC instruction):



$A = 5DH, CY = 0$

(A.)

After execution of ~~RRD~~ RAR) :  $\rightarrow$



A = 50H , CY = 0

(B.)

In the operation of XCHG instruction, Register HL pair and DE pair involves.

Basically, it means,

Exchange H & L with D & E.

The contents of register H are exchanged with the contents of register D & the contents of register L are exchanged with contents of register E.

5)

(a.) difference between memory mapped I/O and I/O mapped I/O : →

| Memory mapped I/O                                                                                                                                                                                                                                                    | I/O mapped I/O                                                                                                                                                                                                                                                                         |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <p>① Here I/O devices are treated as memory</p> <p>② The allotted address size is 16 bit (A<sub>0</sub>-A<sub>15</sub>)</p> <p>③ The data transfer instruction is same for memory and I/O devices</p> <p>④ Here memory read and memory write cycles are involved</p> | <p>① Here I/O devices are treated as I/O devices.</p> <p>② The allotted address size is 8 bit (A<sub>0</sub>-A<sub>7</sub>)</p> <p>③ The data transfer instruction is <del>is</del> different for memory and I/O devices</p> <p>④ Here I/O read and I/O write cycles are involved.</p> |

6.) Operating modes of 8255 programming peripheral interface : →

There are two different modes of 8255, these modes are —

- (i) Bit set reset (BSR) mode.
- (ii) Input output mode.

(i)

Bit Set Reset Mode:  $\rightarrow$ 

This mode is used to set or reset the bits of the port-c only. For BSR mode always D7 will be 0. The control register is looking like this  $\rightarrow$

| Bits | D7 | D6 | D5 | D4 | D3            | D2 | D1 | D0     |
|------|----|----|----|----|---------------|----|----|--------|
| Val  | 0  | X  |    |    | PC bit Number |    |    | 0 or 1 |

The (D3, D2, D1) will be 000 to 111.

In this mode it affects only one bit of port c at a time. when user set the bit, it remains set until user unset it. The user needs to load the bit pattern in control register to change the bit.

(ii) I/O mode:  $\rightarrow$ 

this mode is selected when the D7 bit of the control register is 1.

The mode has also three different modes:

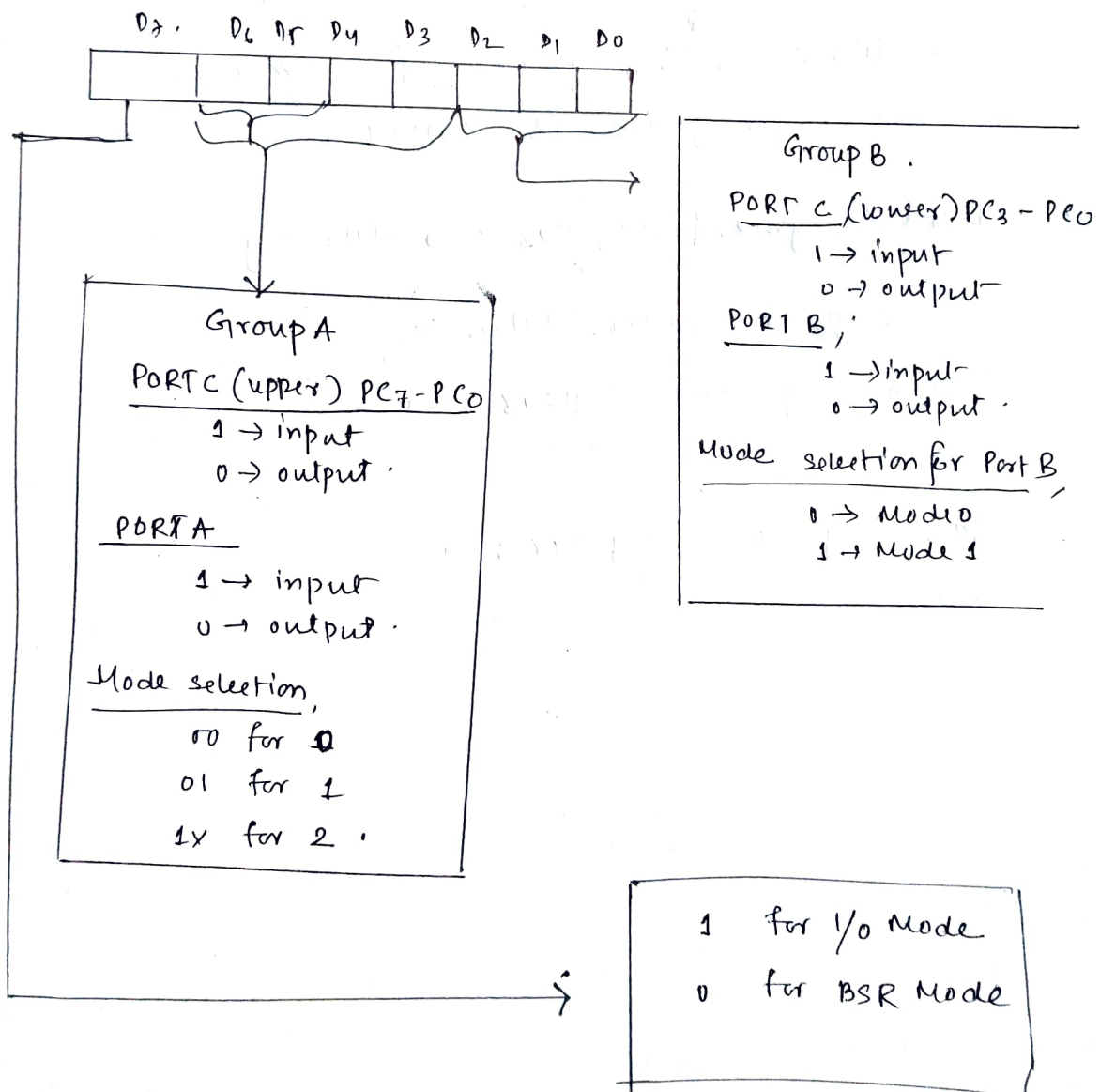
- (i) Mode 0:  $\rightarrow$  simple or basic I/O mode
- (ii) Mode 1:  $\rightarrow$  Handshake or strobed I/O
- (iii) Mode 3:  $\rightarrow$  bidirectional I/O.



## (c) Format for control word of 8255 PPI chip.

As we know, a port can be programmed to act as an input port or an output port. To tell about what we generate a bit pattern or we may say a word which is called control word. A control word is, therefore, to be formed for programming the ports of 8255A.

The format for the control word format for 8255A is below,





⑥  
a.

Segmentation is the process in which the main memory is logically divided into segments with each segment having its base address.

In 8086, there are 4 special purpose 16 bit register ~~are~~ Bus Integer Unit (BIU).

① Code Segment register : → Addressing memory

locations ~~At~~ code segment of memory, where program is stored.

② Data segment register : → data segment register stores data.

③ Extra segment register : →

④ Stack segment register : →

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## Advantages of the segmented memory : →

- (i) To generate 20 bit physical address, the processor just maintains two 16-bit registers, which are within the word length capacity of the machine.
- (ii) All these segments are logical segments. They may or may not be physically separated.

## © Physical addressing of 8086 : →

- (i) Complete physical address of 20 bits long is generated by using 16-bit segment and 16 bit offset registers.
- (ii) segment register contains 16 bit segment base address corresponding to segment.
- (iii) Any of the pointers and index registers or BX may contains offset of location to be addressed.
- (iv) For generating a physical address from the contents of these two registers, the contents of the segment register is shifted left 4 bit-wise 1 times in 20 bit address format and to this result, content of an offset register also called as offset address is added, to produce a 20 bit physical address.

(a.) Segment address —

1004H  $\rightarrow$  0001 0000 0000 0100

offset address —

5434H  $\rightarrow$  0101 0100 0011 0100

Shifted by 4 bit positions,

0001 0000 0100 0100 0000  
(10040H)

offset address.

0101 0100 0011 0100  
(5434H)

---

0001 0101 0100 0111 0100  
(15475H).

7

8 a

Loop

~~JMP~~ In loop instructions, the code is gonna execute several times. The block of codes are executed continuously till the expression is true.

Jump: In jump instruction, we ~~generate~~ is used to jump from one block of statement to another. It is used to skip some of the parts.

6) Program :→

MOV AX, 3000H ; Load 3000H in AX  
MOV DS, AX ; Initialize data segment with 3000H.  
MOV BX, [0300H] ; Move contents of addr with 0300H offset in BX

ADD [0300H], 0FH ; Add byte 0FH to contents in BX.

MOV DX, [0300H] ; store result in DX.

MOV [0400H], DX ; store result in 0400H.

HLT ; stop execution.

①

Program: →

MOV CX, 0FH ; Initialize counter (cx)  
for number of iterations.

MOV AX, 3000H ; load AX with 3000H

MOV DS, AX ; initialize data segment  
(DS) with 3000H.

MOV SI, 0300H ; initialize source pointer  
with 0300H.

MOV AX, [SI] ; load first number in  
AX

XX: INC SI ; increment source  
pointer from 0300H.

CMP AX, [SI] ; compare with next  
number.

JNC YY ; if the next  
number is not  
larger, go to YY.

MOV AX, [SI] ; replace the  
previous one  
with the next in  
AX

YY: LOOP XX ; Repeat the process for 15 times.

HLT ; Halt (stop execution)