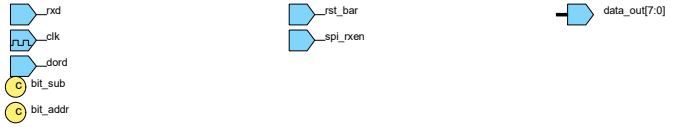
Entity: spi_rx_shifter_fsm_2
Architecture: fsm
Active-HDL Student Edition




```
output: process (present_state, rxd, clk, bit_addr, bit_sub)
        begin
          case present_state is
            when idle =>
            bit_sub <= "111";
            bit_addr <= "000";
            data_out <= "00000000";
            when ph1 =>
                if dord = '1' then
                    data_out(to_integer(bit_addr)) <= rxd;
                elsif dord = '0' then
                    data_out(to_integer(bit_sub)) <= rxd;
                end if;
            when ph2 =>
             if rising_edge(clk) then
                if dord = '0' then
                    bit_sub <= bit_sub - 1;
                elsif dord = '1' then
                    bit_addr <= bit_addr + 1;
                end if;
             end if;
          end case;
        end process;
```