# *Verilog with Quartus*

# *Tools*

You need two things

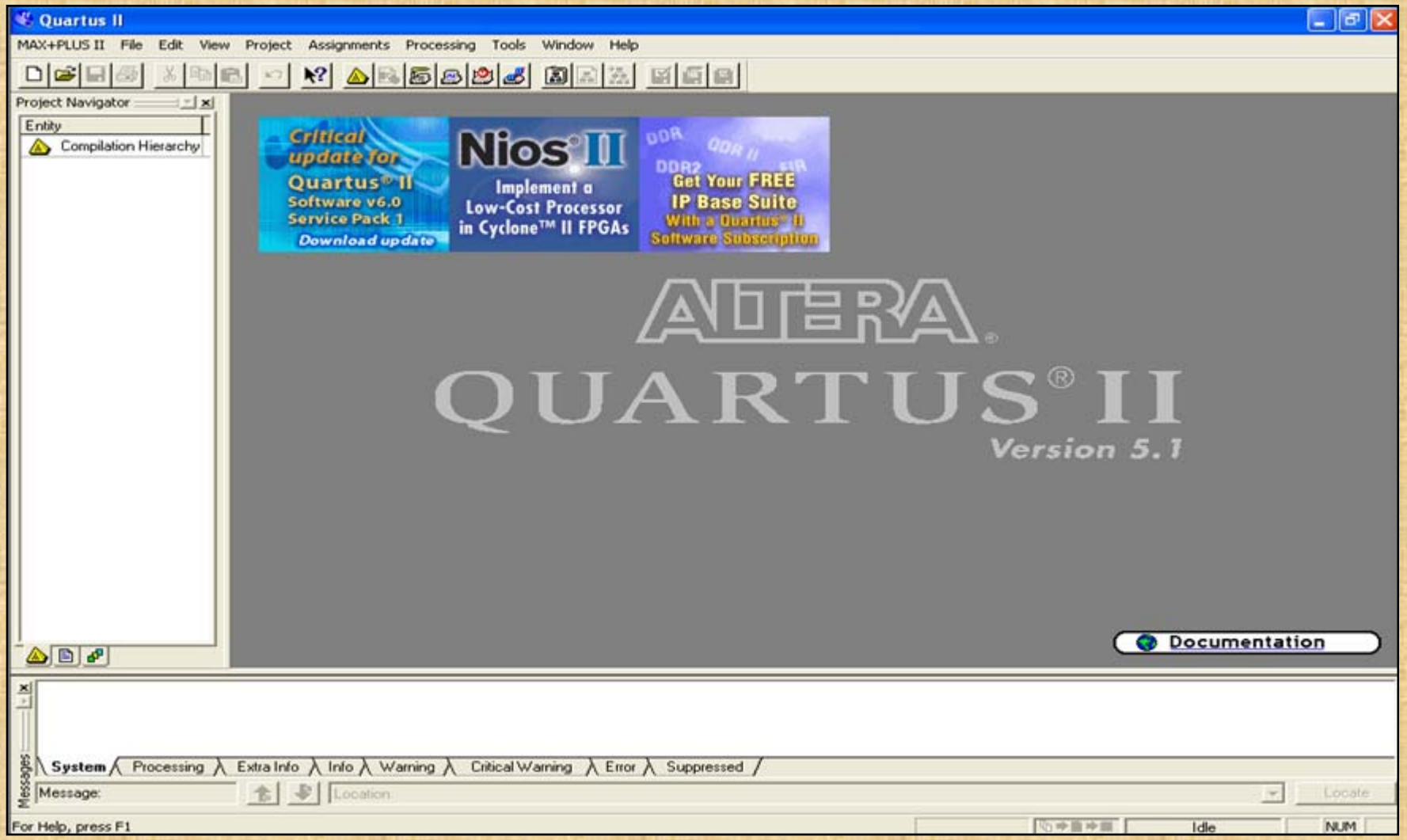
1. **Editor**

   Quartus II 5.1sp2 Web Edition Full

2. **Simulators**

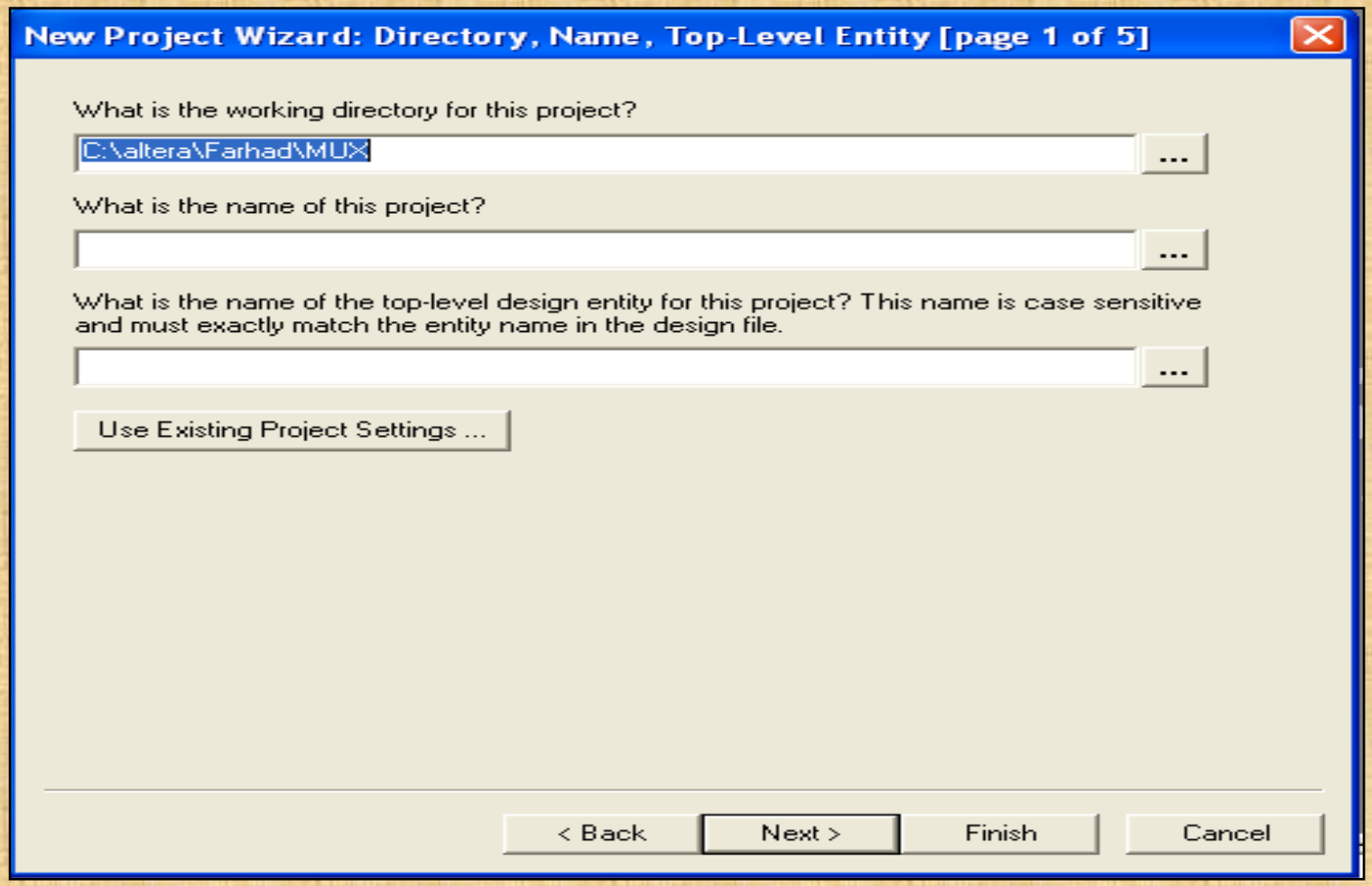
   Quartus II 5.1sp2 Web Edition Full

# Quartus IDE

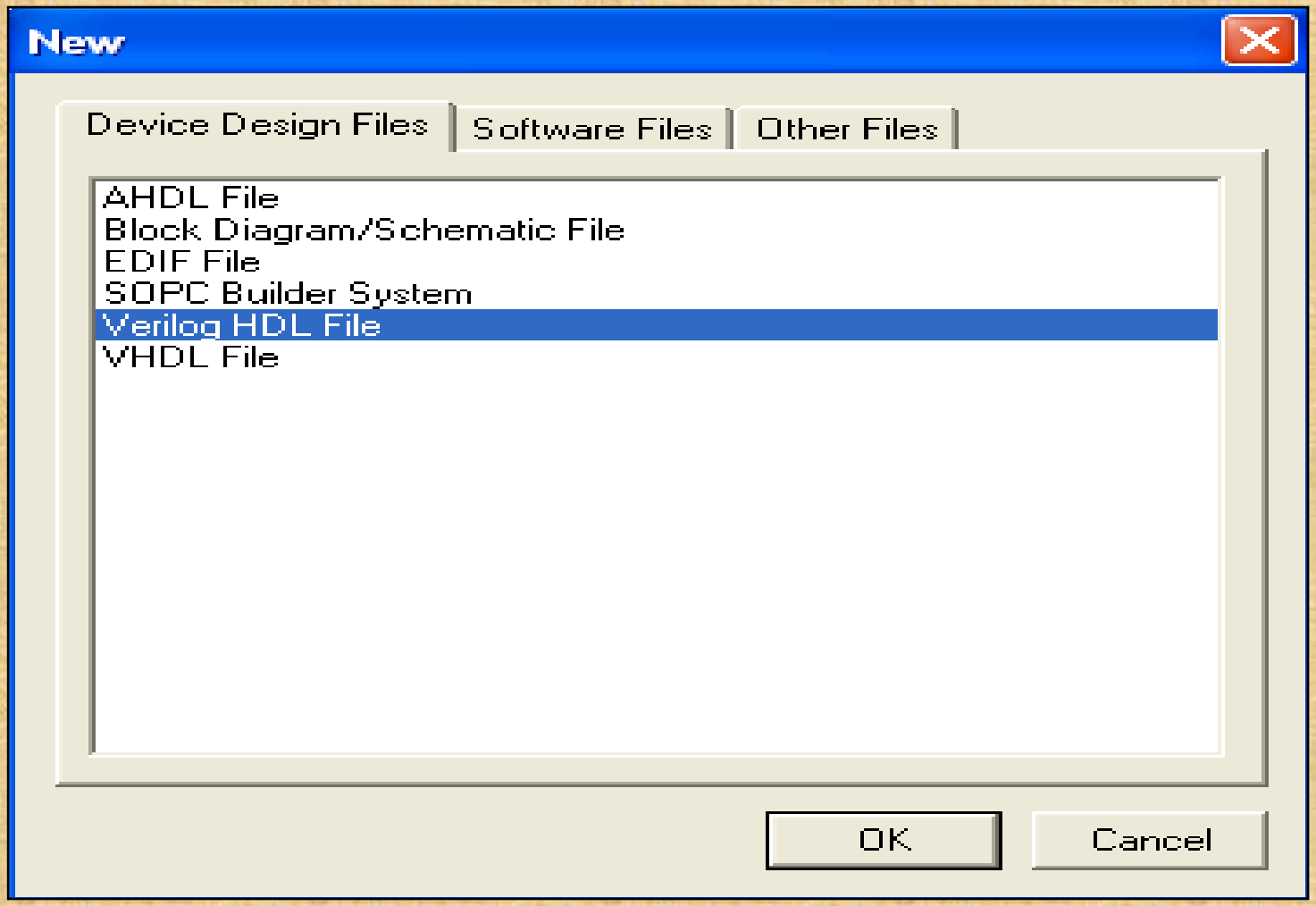

Quartus II
MAX+PLUS II File Edit View Project Assignments Processing Tools Window Help
Project Navigator
Entity
Compilation Hierarchy
Critical update for Quartus® II Software v6.0 Service Pack 1
Download update
Nios® II
Implement a Low-Cost Processor in Cyclone™ II FPGAs
Get Your FREE IP Base Suite With a Quartus® II Software Subscription
ALTERA
QUARTUS® II
Version 5.1
Documentation
Messages
System Processing Extra Info Info Warning Critical Warning Error Suppressed
Message:
Location
Locate
For Help, press F1
Idle
NUM

# *Example of MUX 2/1*

- Create a project



# *Create/Add verilog file to the project*



# *Structural*

```
module mux21(a, b, s, y);
    input a, b, s;
    output y;
    wire m, n, p;
    and g1(m, b, s);
    not g2(n, s);
    and g3(p, a, n);
    or g4(y, m, p);
endmodule
```

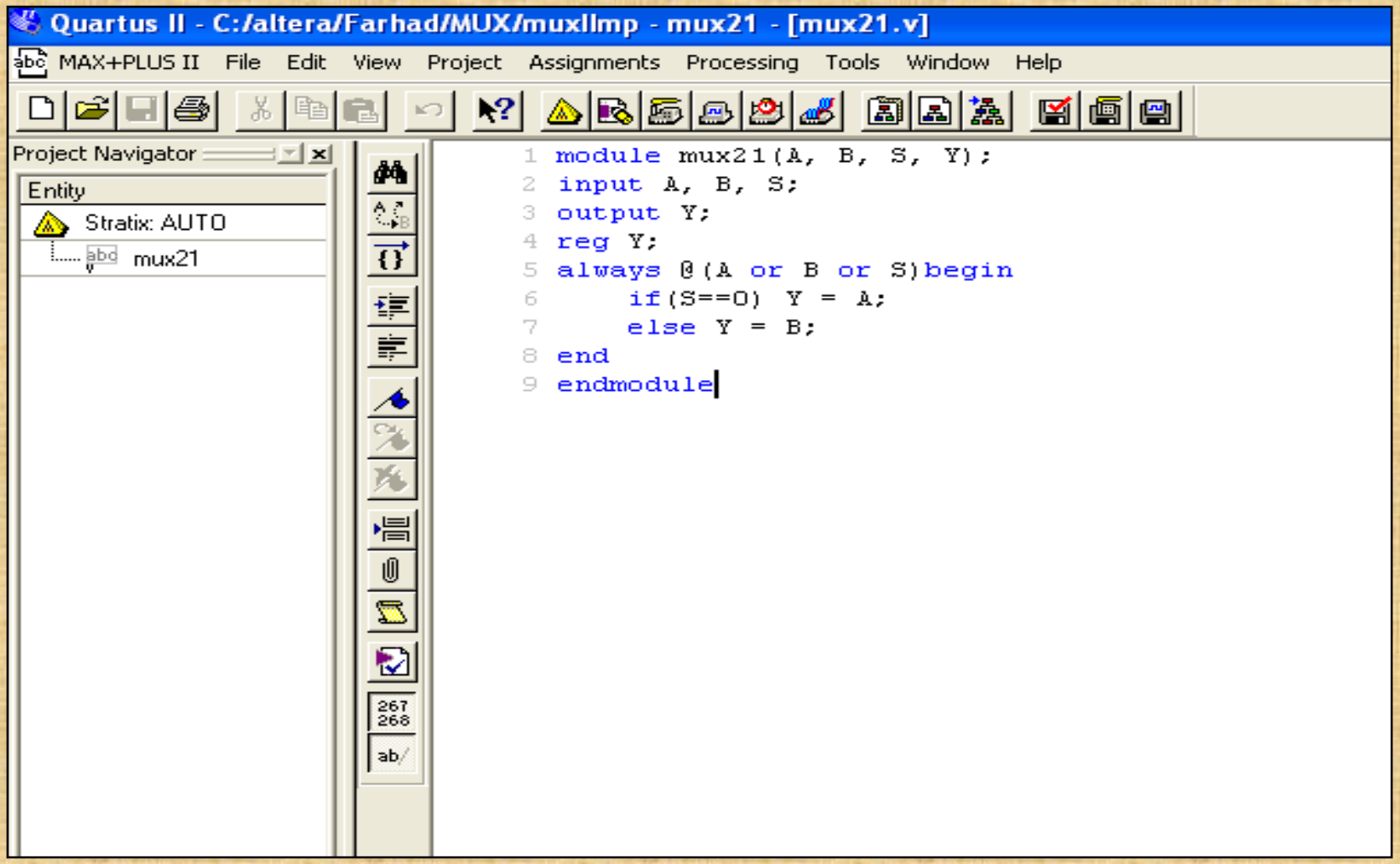
# *RTL*

```
module mux21(a, b, s, y);
    input a, b, s;
    output y;
    assign y = s ? b : a;
endmodule
```

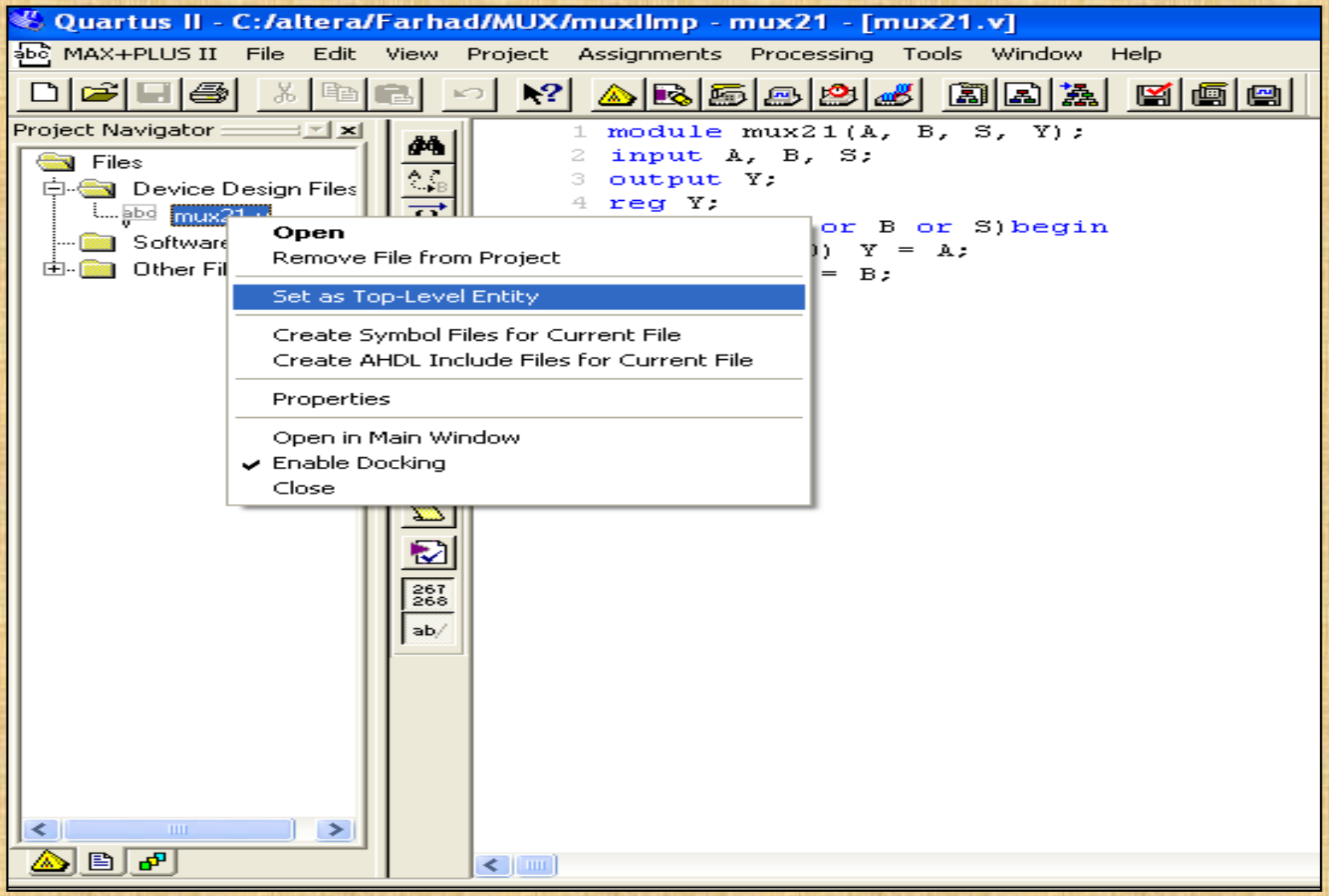
# *Behavioral*

```
module mux21(A, B, S, Y);
   input A, B, S;
   output Y;
   reg Y;
   always @(A or B or S)begin
        if(S==0) Y = A;
        else Y = B;
   end
endmodule
```

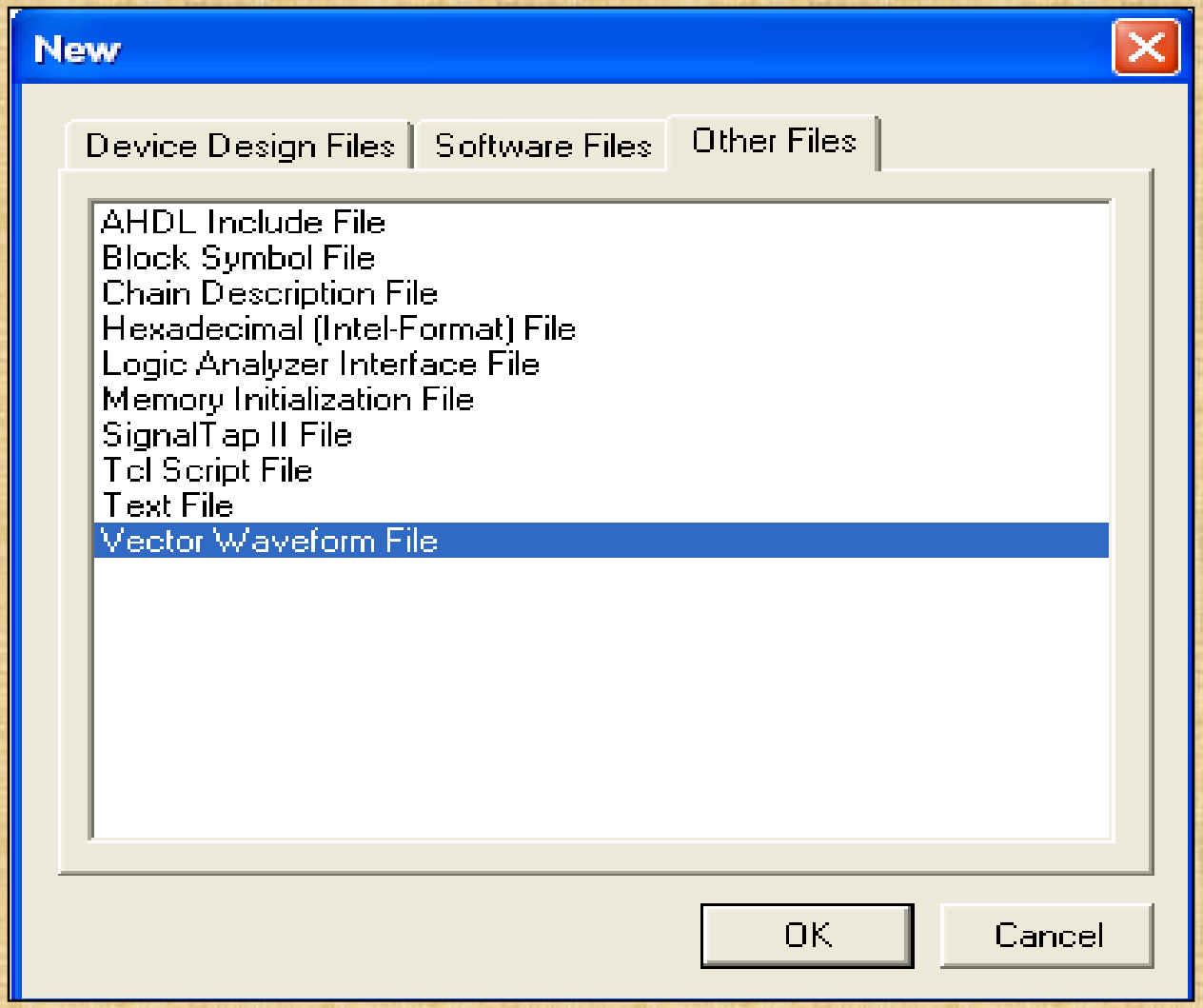
# File is added to the project



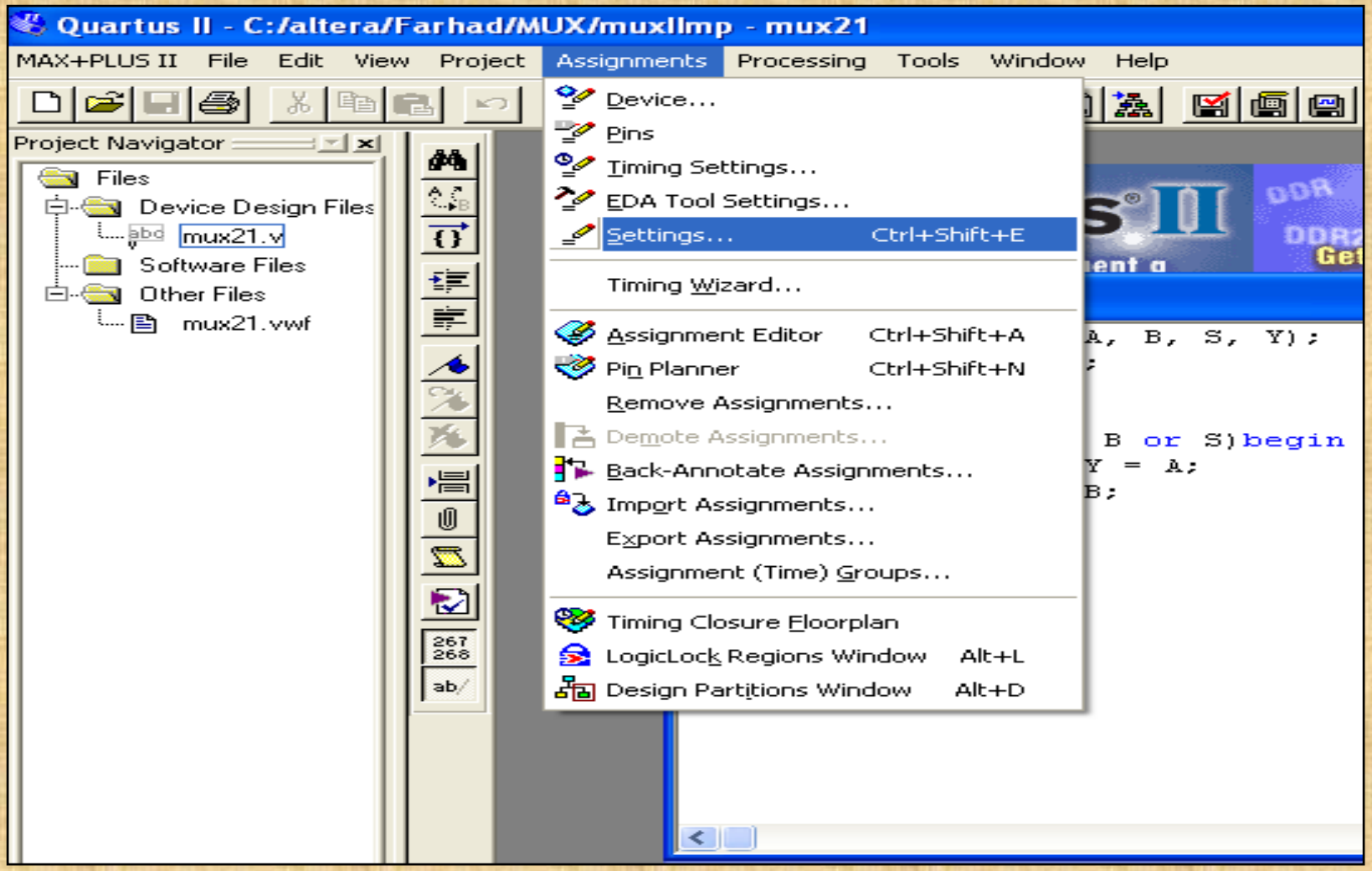
# *Set the file as top level entity*



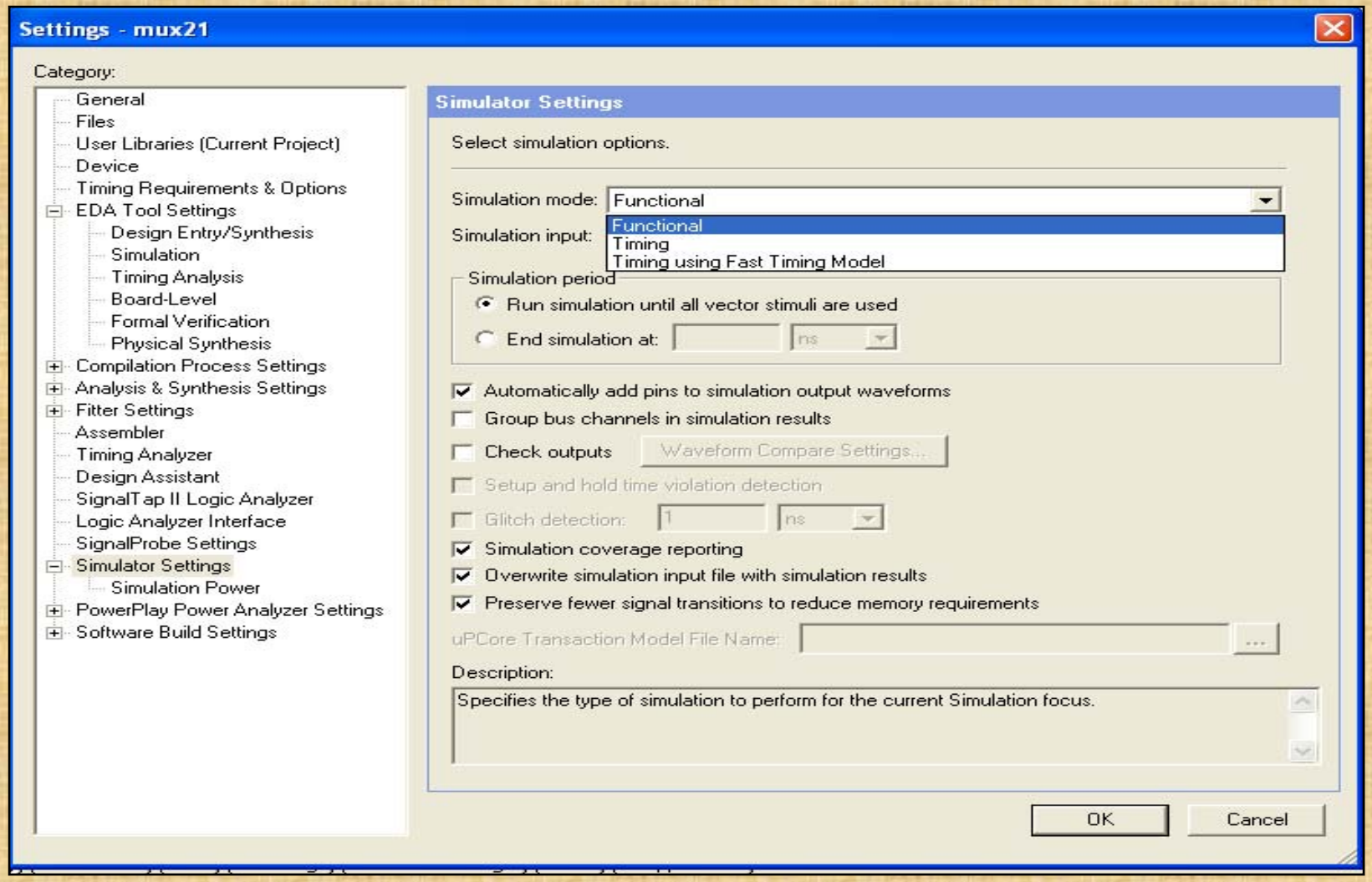
# *Create a vector waveform file to synthesize and add to the project*



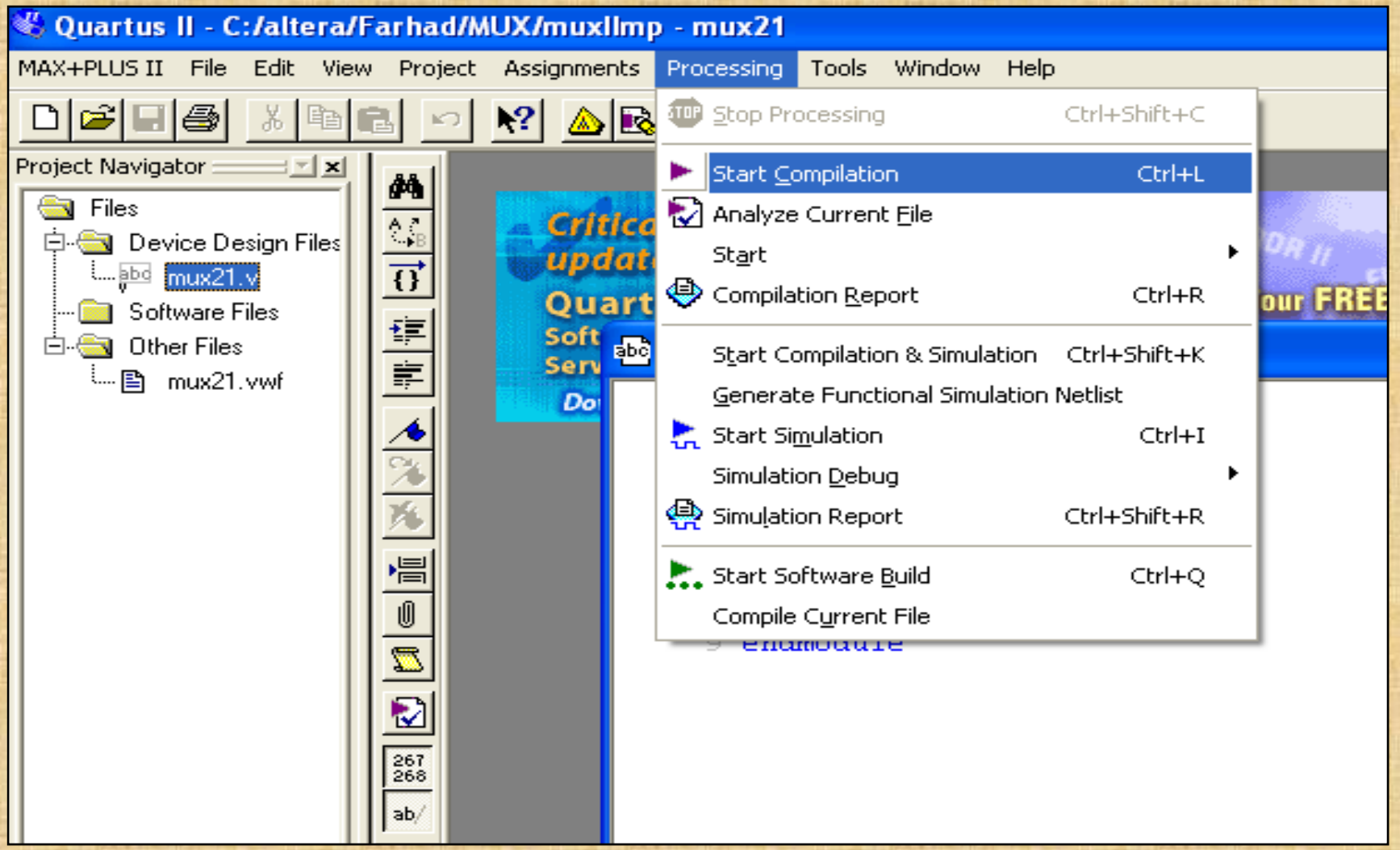
# Settings


Quartus II - C:/altera/Farhad/MUX/muxIImp - mux21
MAX+PLUS II
File
Edit
View
Project
Assignments
Processing
Tools
Window
Help
Project Navigator
Files
Device Design Files
mux21.v
Software Files
Other Files
mux21.vwf
Device...
Pins
Timing Settings...
EDA Tool Settings...
Settings... Ctrl+Shift+E
Timing Wizard...
Assignment Editor Ctrl+Shift+A
Pin Planner Ctrl+Shift+N
Remove Assignments...
Demote Assignments...
Back-Annotate Assignments...
Import Assignments...
Export Assignments...
Assignment (Time) Groups...
Timing Closure Floorplan
LogicLock Regions Window Alt+L
Design Partitions Window Alt+D
A, B, S, Y);
B or S)begin
Y = A;
B;

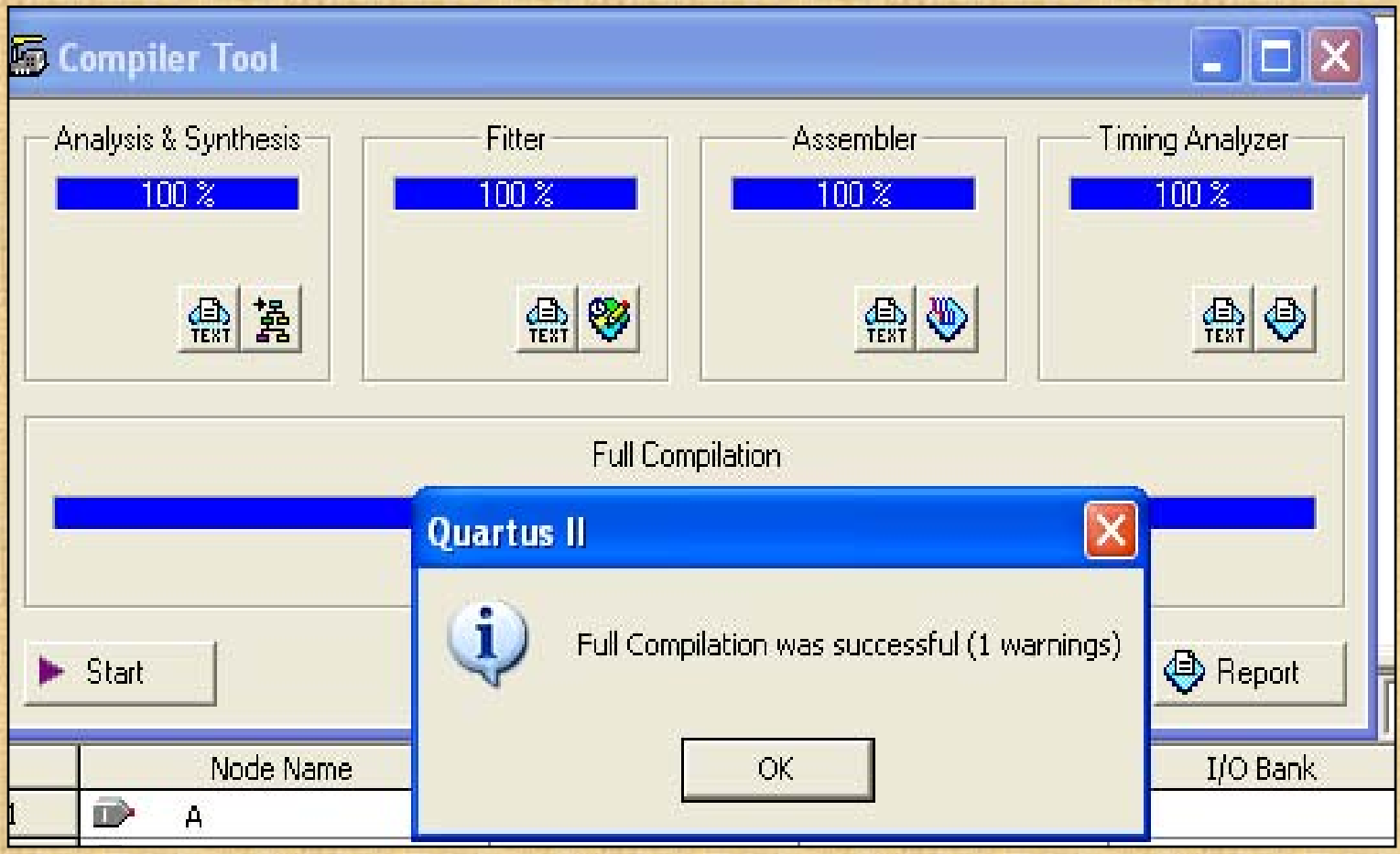
# *Functional Simulation*



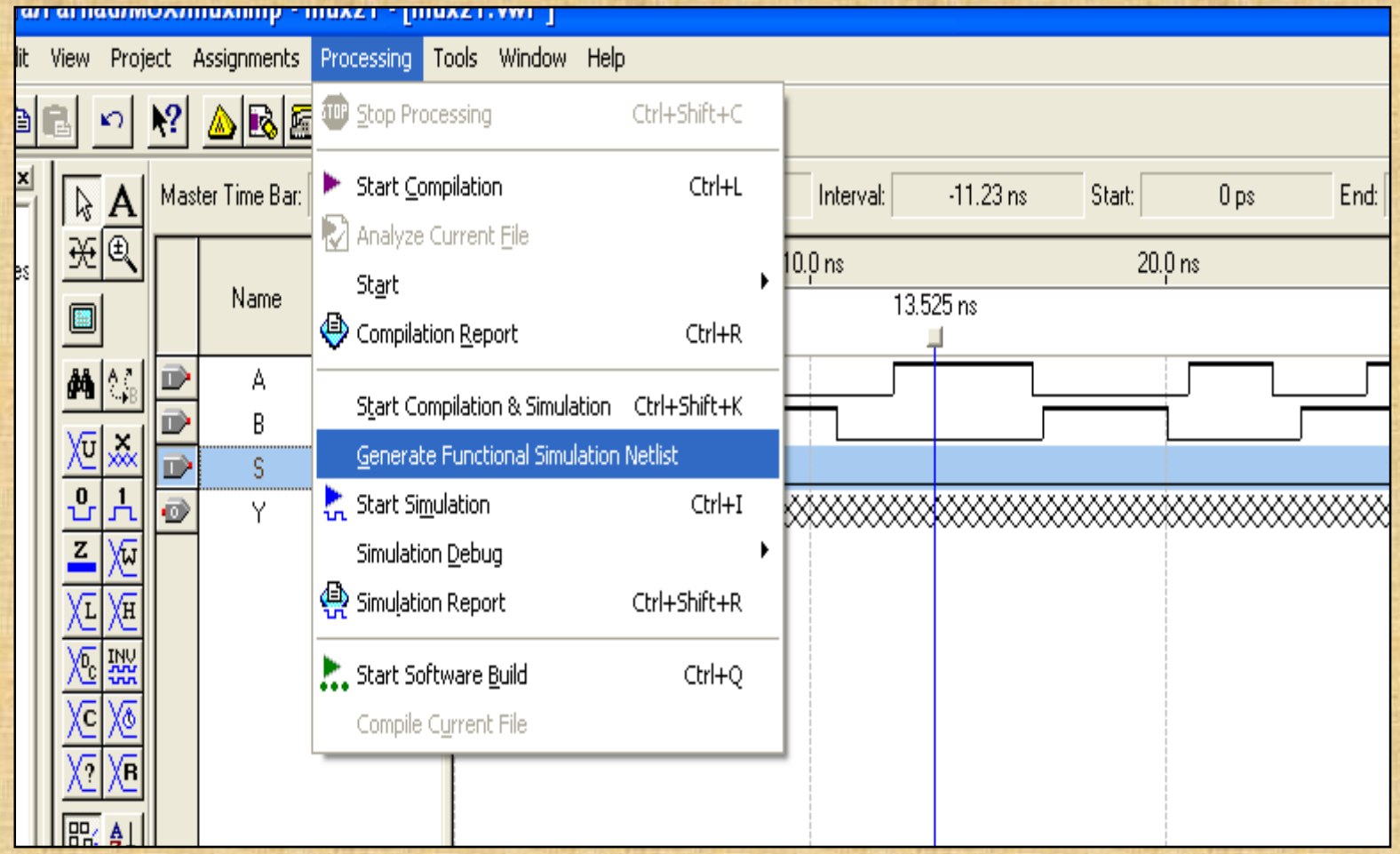
# Compilation Start



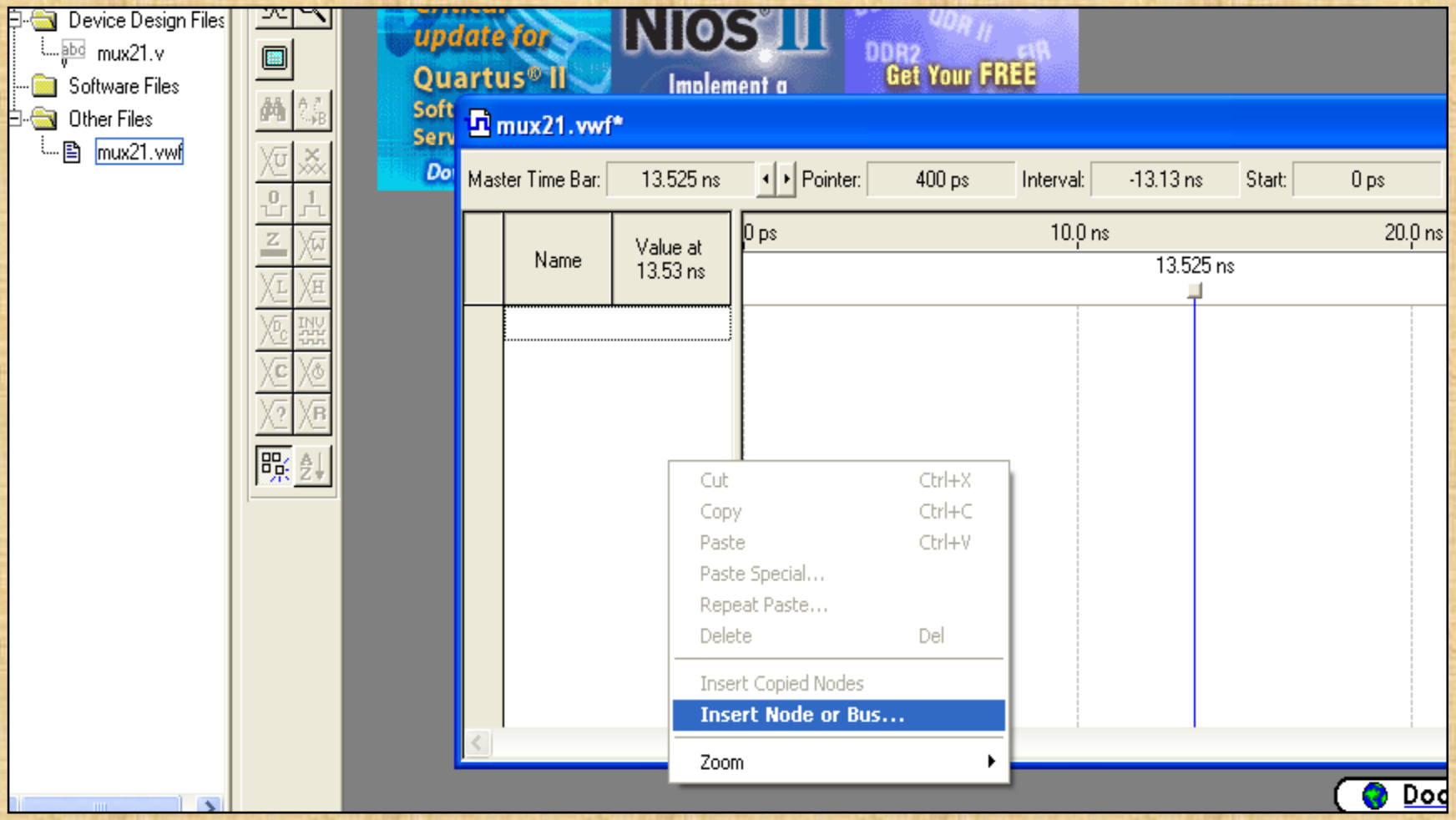
# Compilation Successful



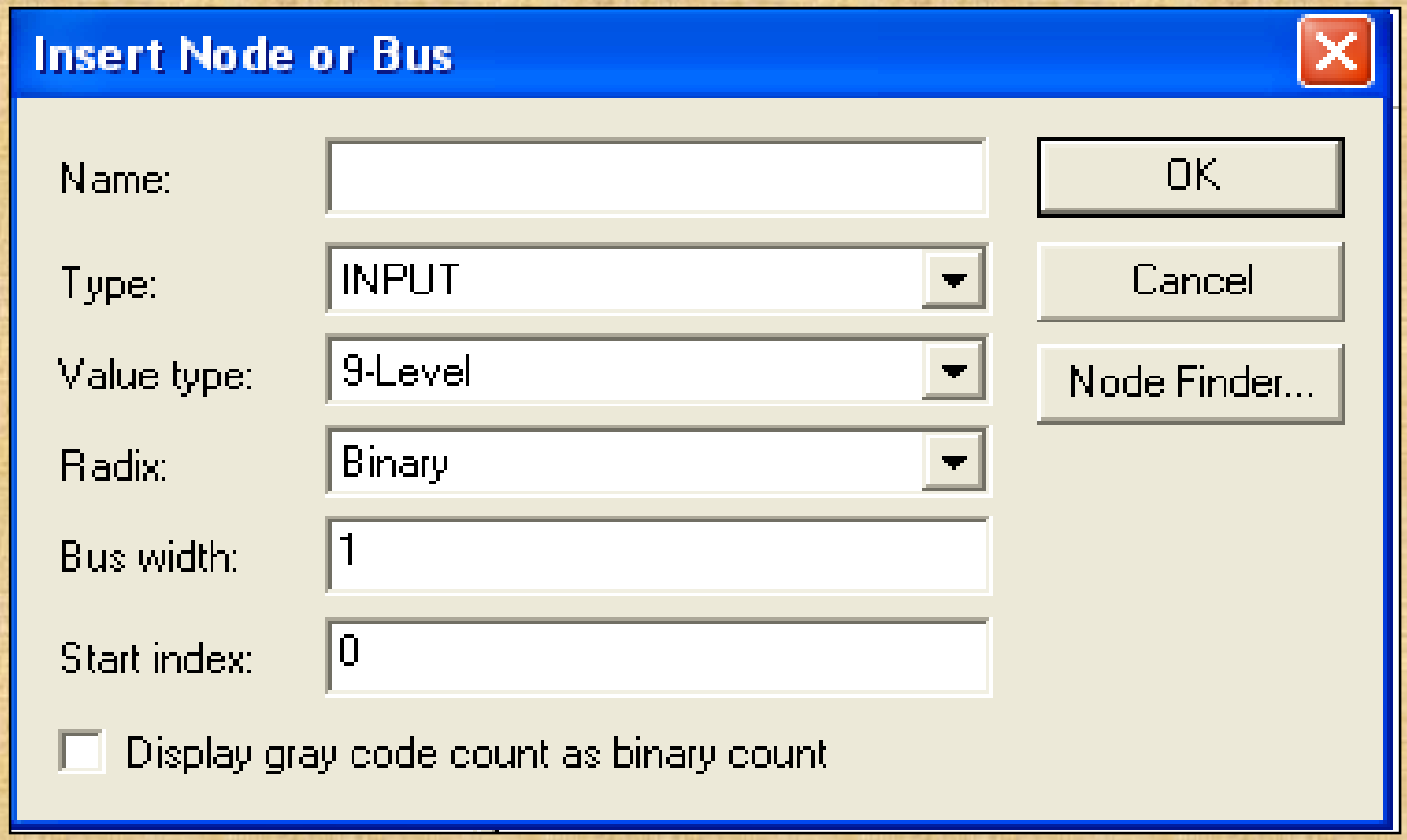
# Generate Simulation Netlist



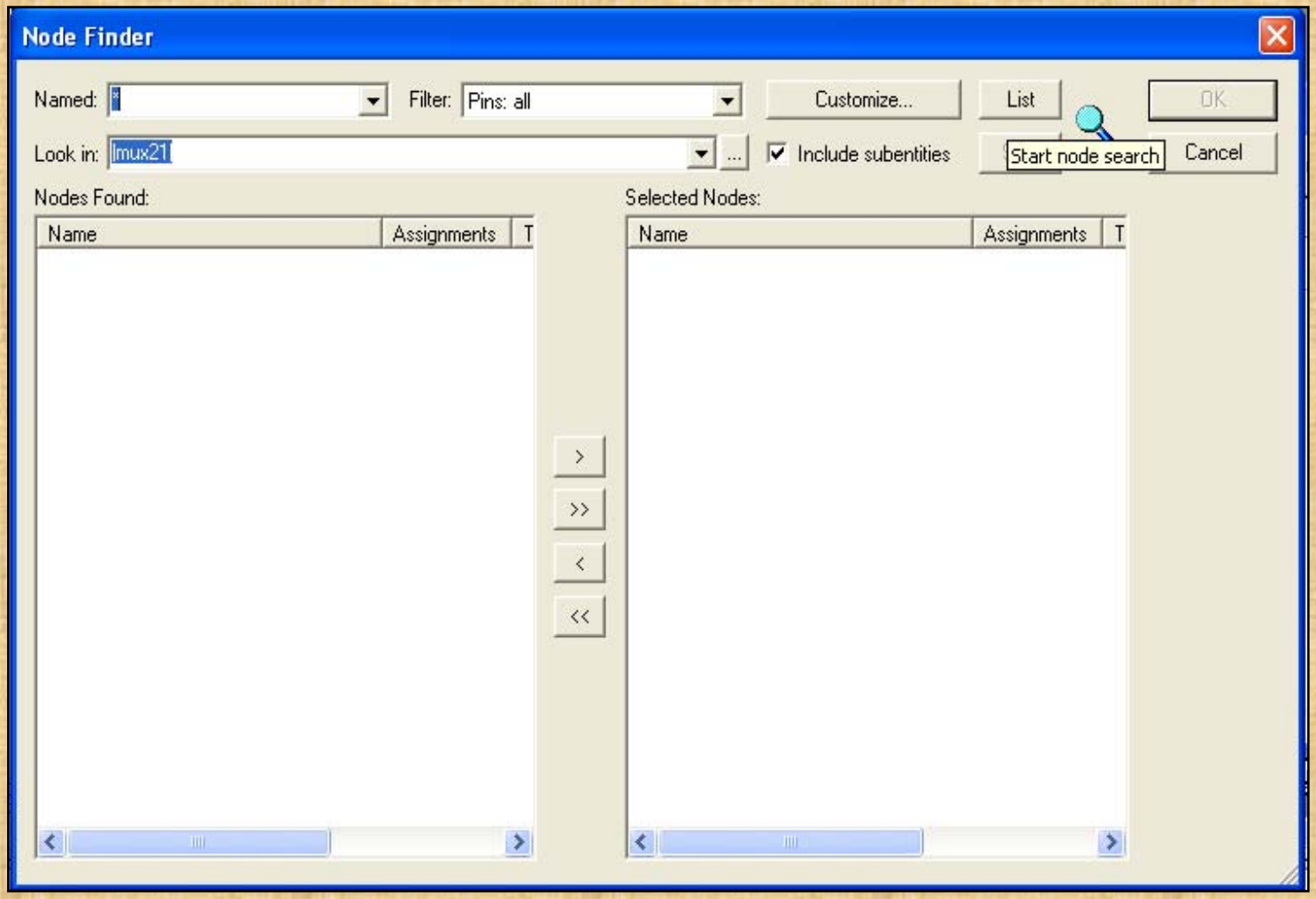
# Insert Node


Device Design Files
mux21.v
Software Files
Other Files
mux21.vwf
update for
Quartus® II
NIOS® II
Implement a
DDR2
Get Your FREE
mux21.vwf*
Master Time Bar: 13.525 ns
Pointer: 400 ps
Interval: -13.13 ns
Start: 0 ps
Name
Value at 13.53 ns
0 ps
10.0 ns
20.0 ns
13.525 ns
Cut Ctrl+X
Copy Ctrl+C
Paste Ctrl+V
Paste Special...
Repeat Paste...
Delete Del
Insert Copied Nodes
Insert Node or Bus...
Zoom

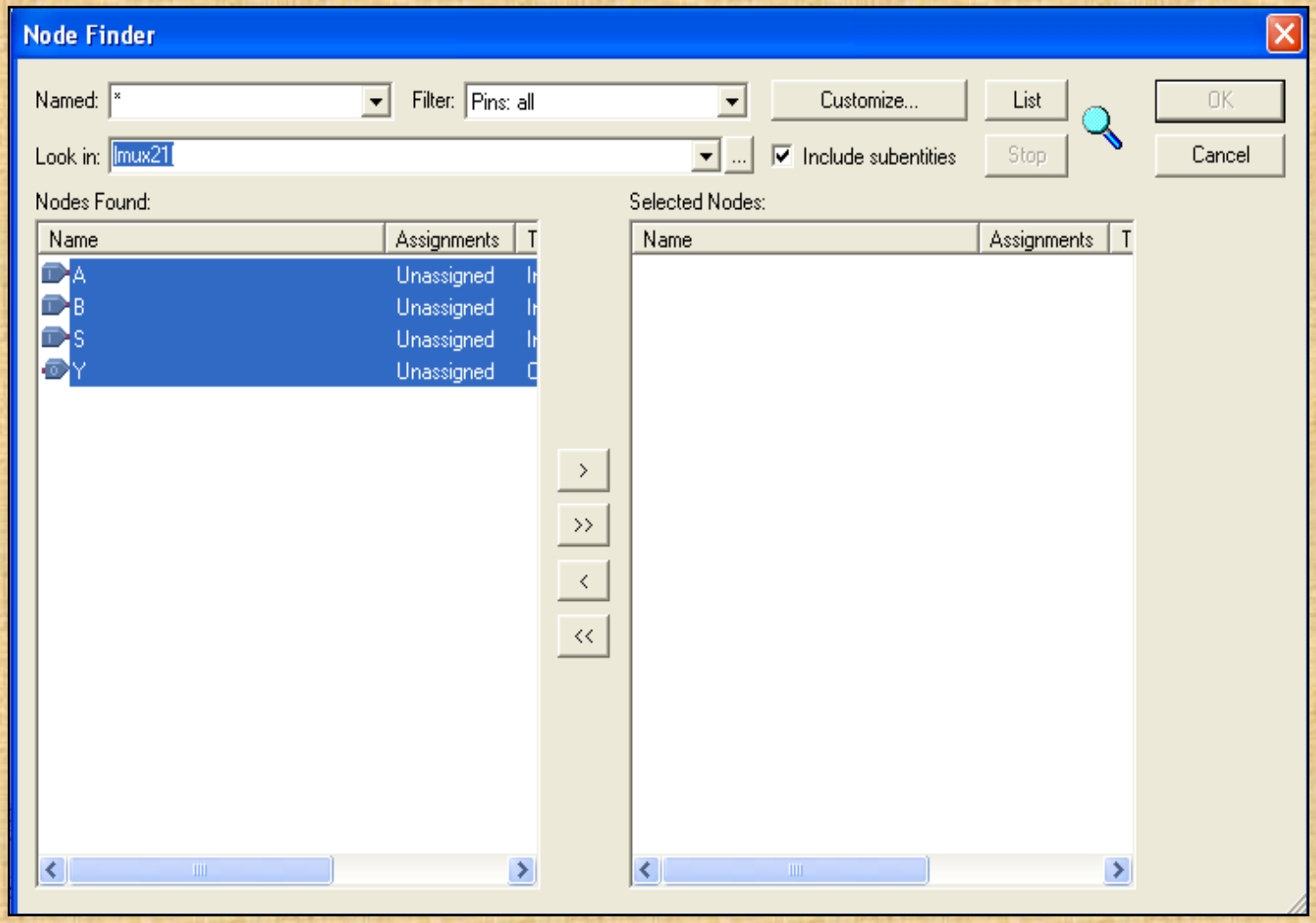
# *Setup Node*


Insert Node or Bus
Name:
Type:
INPUT
Value type:
9-Level
Radix:
Binary
Bus width:
1
Start index:
0
Display gray code count as binary count
OK
Cancel
Node Finder...

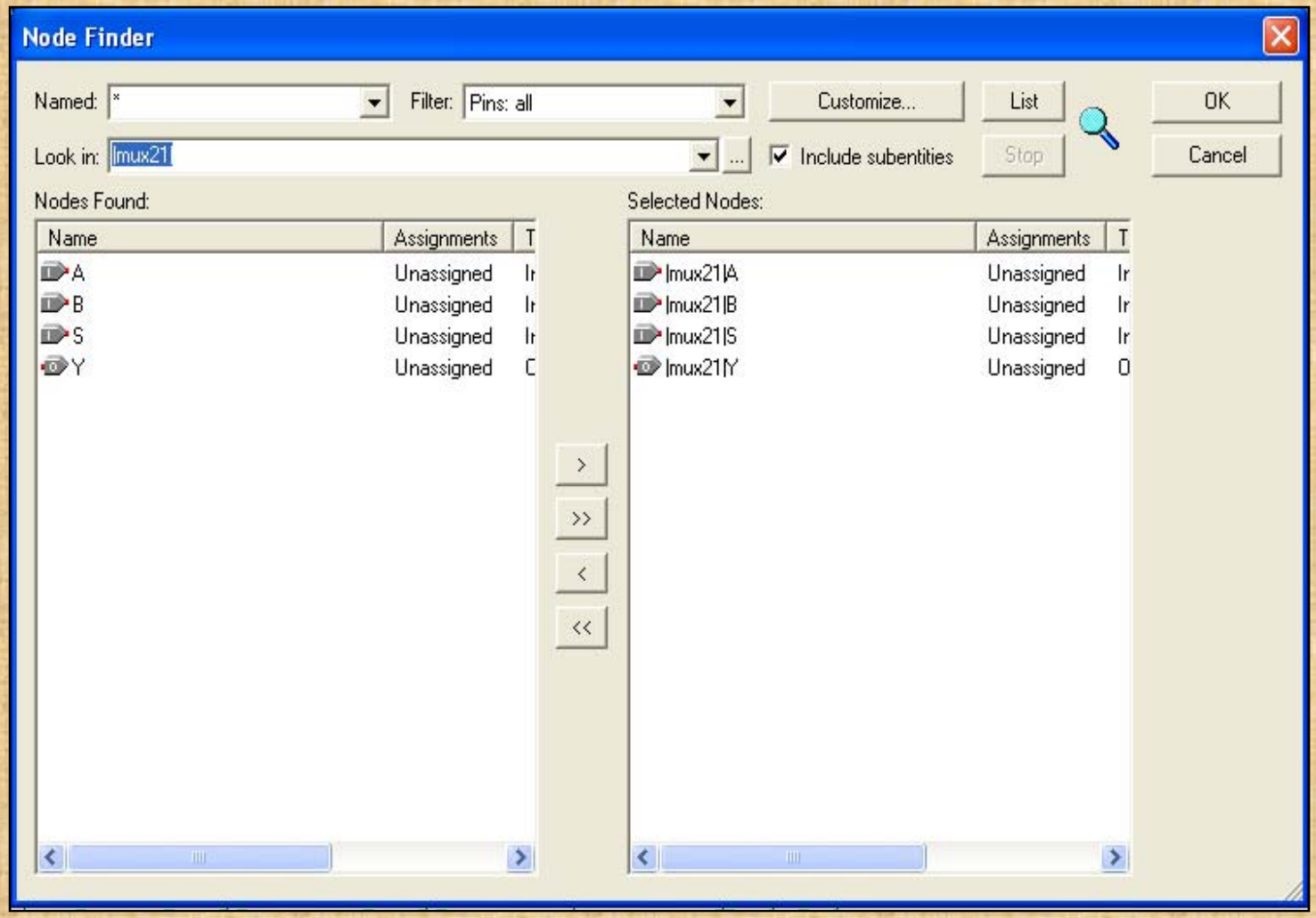
# Select Node


Node Finder
Named:
*
Filter:
Pins: all
Customize...
List
OK
Look in:
lmux21
...
Include subentities
Start node search
Cancel
Nodes Found:
Name
Assignments
T
Selected Nodes:
Name
Assignments
T
>
>>
<
<<

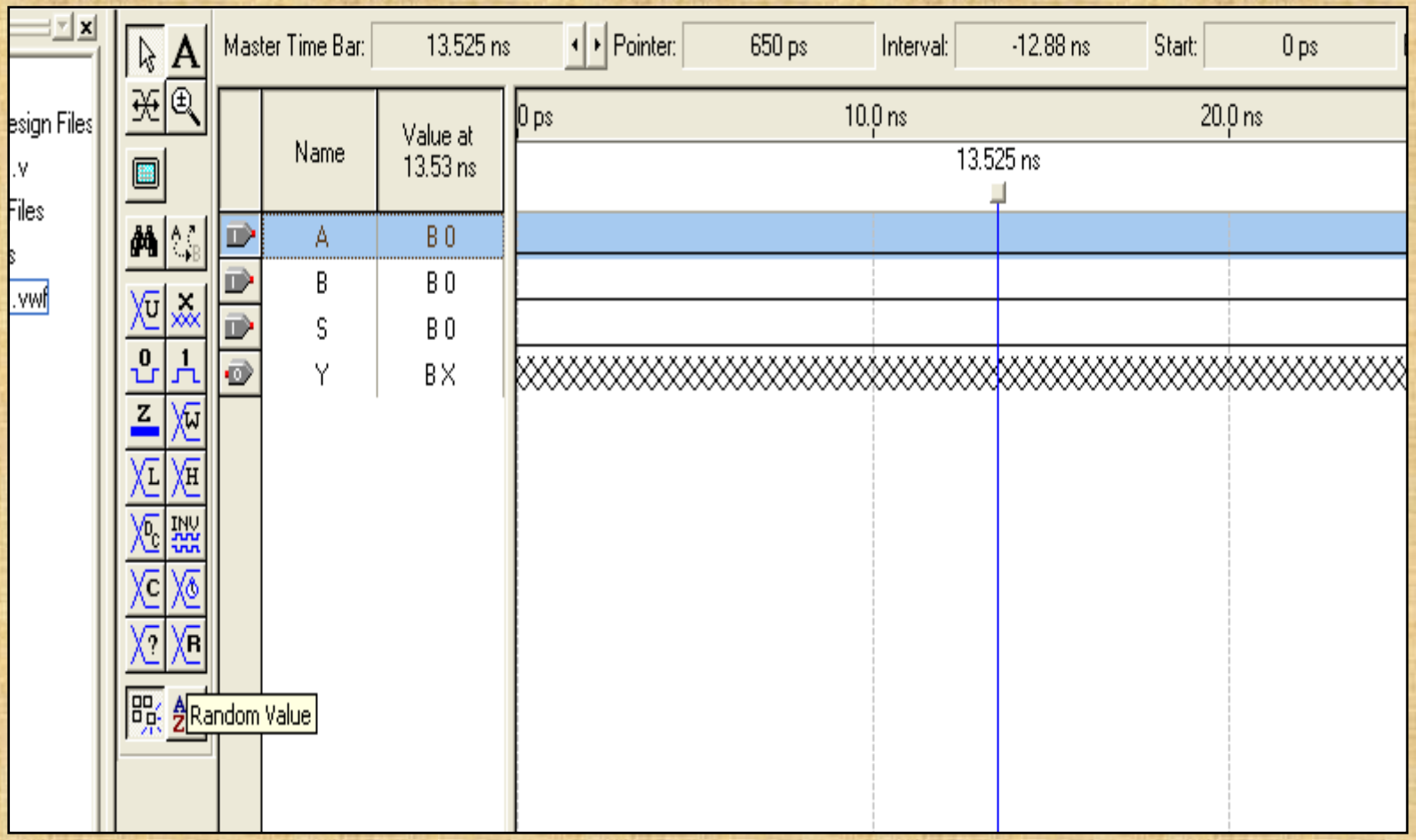
# Select Node


Node Finder
Named:
*
Filter:
Pins: all
Customize...
List
OK
Look in:
lmux21
...
Include subentities
Stop
Cancel
Nodes Found:
Name
Assignments
A
Unassigned
B
Unassigned
S
Unassigned
Y
Unassigned
>
>>
<
<<
Selected Nodes:
Name
Assignments

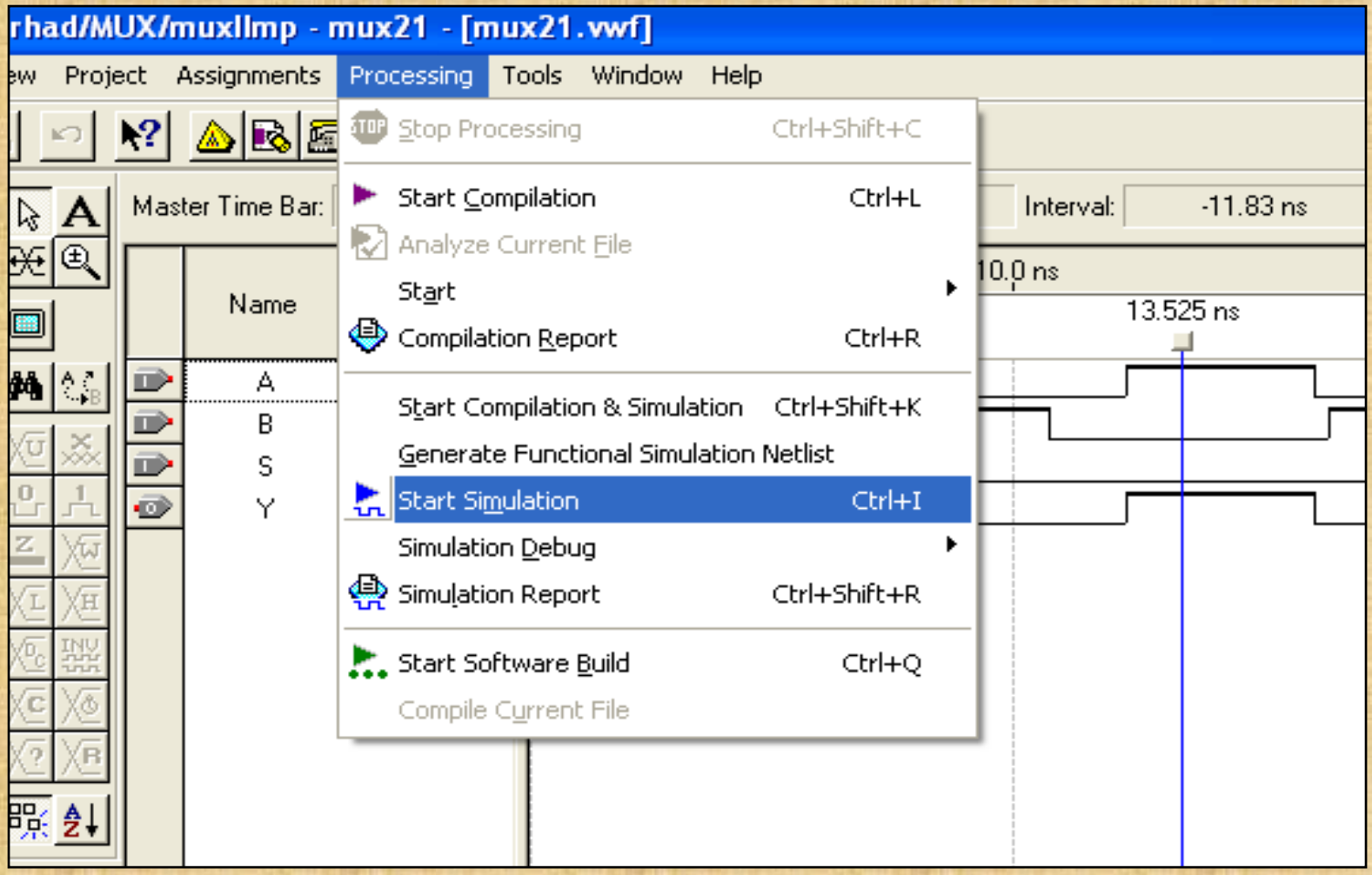
# Select Node


Node Finder
Named: *
Filter: Pins: all
Customize...
List
OK
Look in: |mux21
Include subentities
Stop
Cancel
Nodes Found:
Name
Assignments
A
Unassigned
B
Unassigned
S
Unassigned
Y
Unassigned
Selected Nodes:
Name
Assignments
|mux21|A
Unassigned
|mux21|B
Unassigned
|mux21|S
Unassigned
|mux21|Y
Unassigned

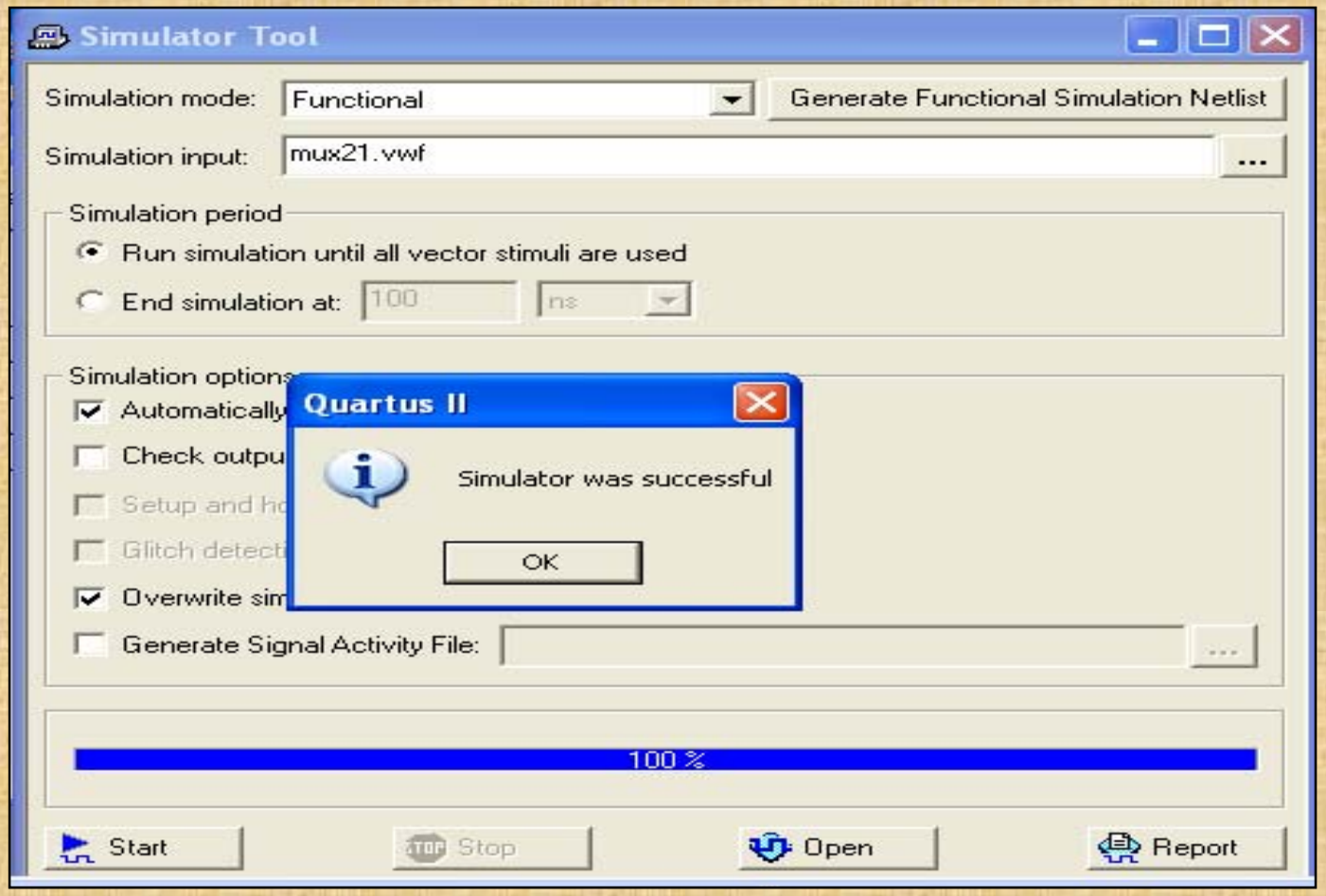
# *Assign Value to the Node*



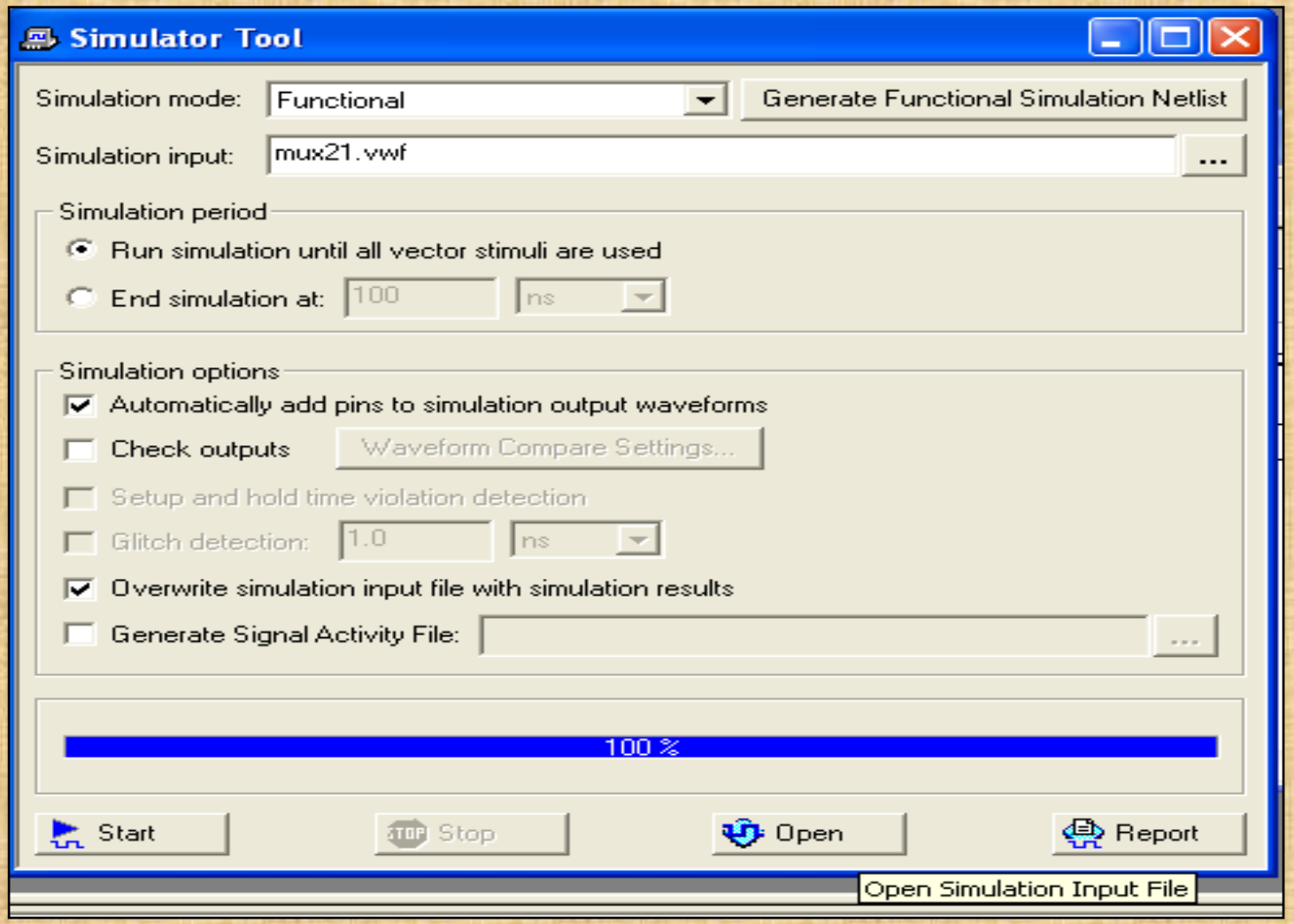
# Start Simulation



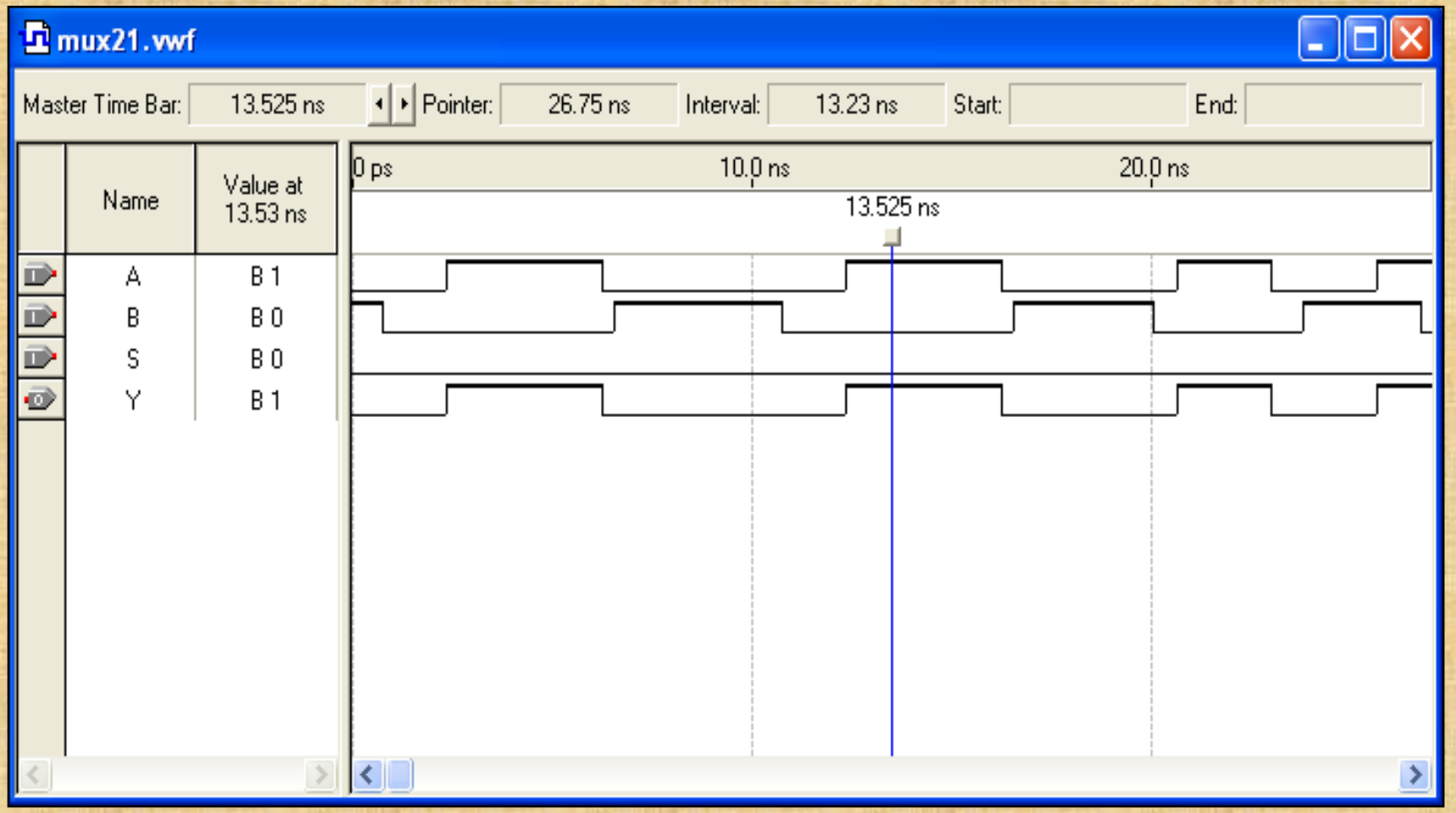
# *Simulation Successful*



# *Simulation Waveform*



# *Simulation Output*



***The End***