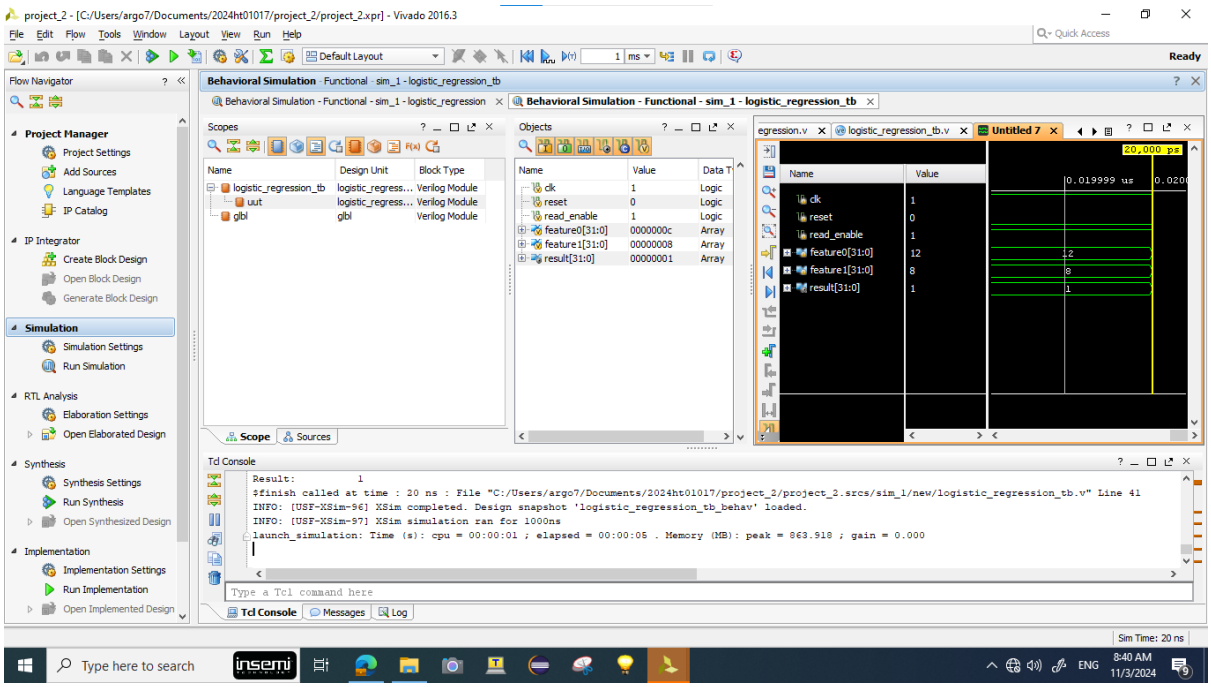
Output for class =1



Interpretation of the output

feature0 = 12

feature1 = 8

weight0 = 5

weight1 = -3

bias = 1

Linear Combination Calculation:

z= (weight0×feature0) + (weight1×feature1) +bias

z= (5×12)+(−3×8)+1 =60−24+1=37

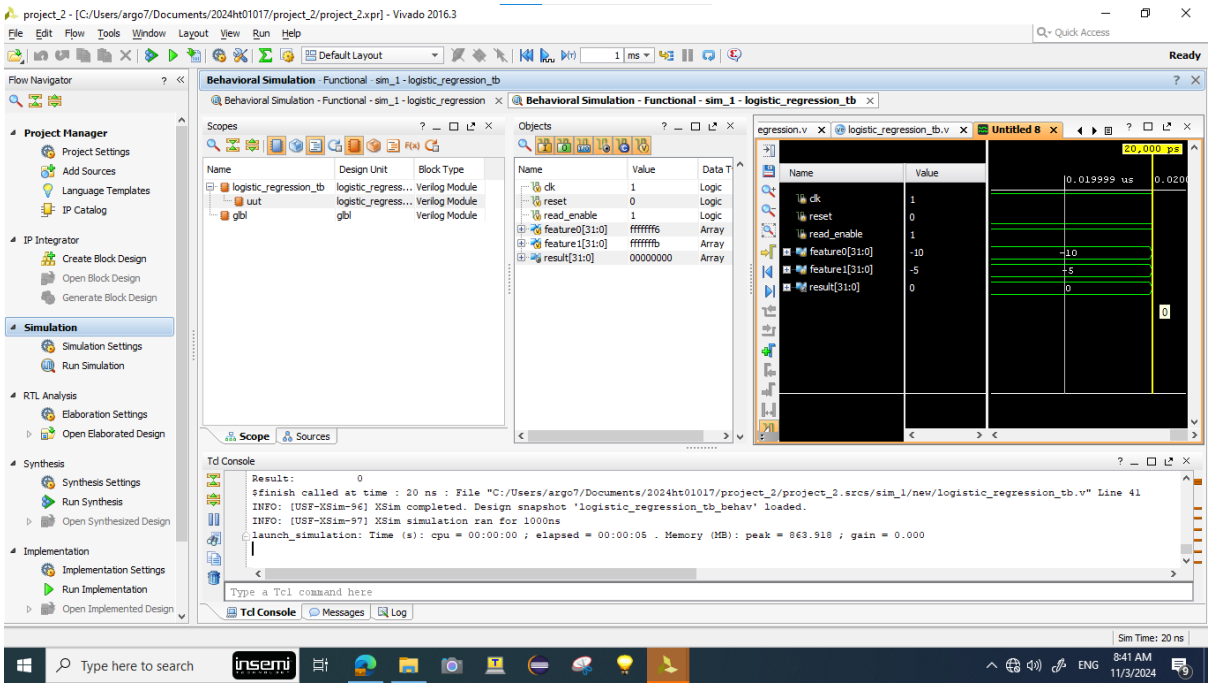
Sigmoid Approximation:

If z>0, then result=1

If z<0, then result =0

z=37>0 ----> result =1

Output for class =0



Interpretation of the output

feature0 = -10

feature1 = -5

weight0 = 5

weight1 = -3

bias = 1

Linear Combination Calculation:

z= (weight0×feature0) + (weight1×feature1) +bias

z= (5×−10) + (−3×−5)+1 = −50+15+1=−34

Sigmoid Approximation:

If z>0, then result=1

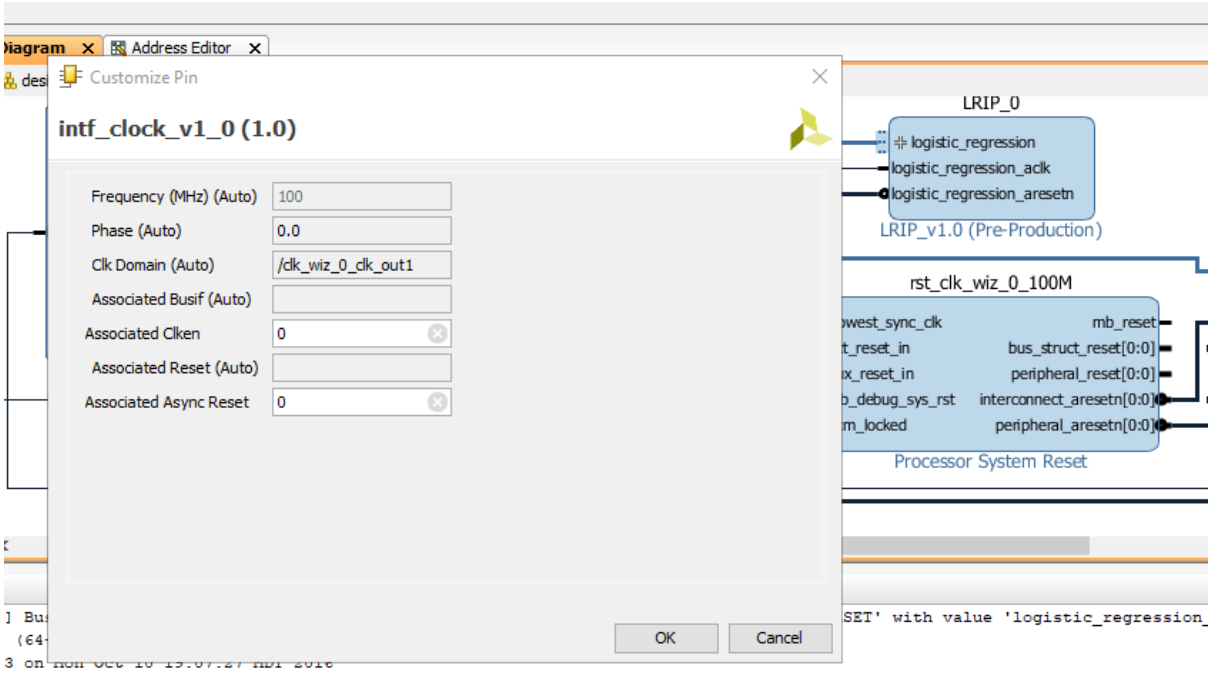
If z<0, then result =0

z=-34<0 --> so result =0

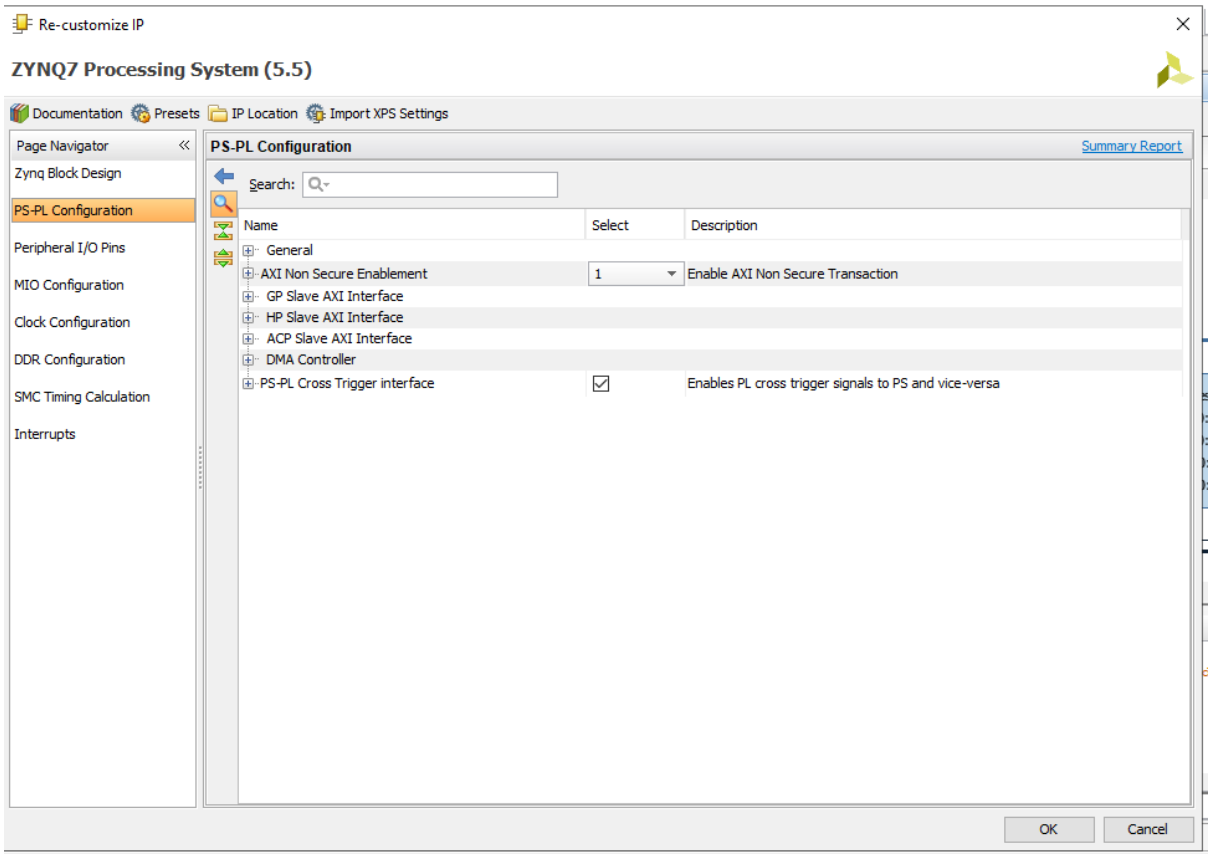
Test Results

Incorporating the custom Logic into the IP and re-packaging: An IP named LRIP is created. The LRIP_v1_0_logical_regression.v code in the 'hdl' folder is replace with customized code. The IP is repackaged before adding it into the system design.

Clock Configuration Using Clocking Wizard: A stable clock signal was critical for the synchronous operation of LRIP in the PL. The Clocking Wizard was configured to generate the appropriate frequency, manually connected to the aclk input of the LRIP. This process included selecting the clock output from the wizard, checking frequency compatibility with the LRIP, and validating the connection through Vivado's interface.

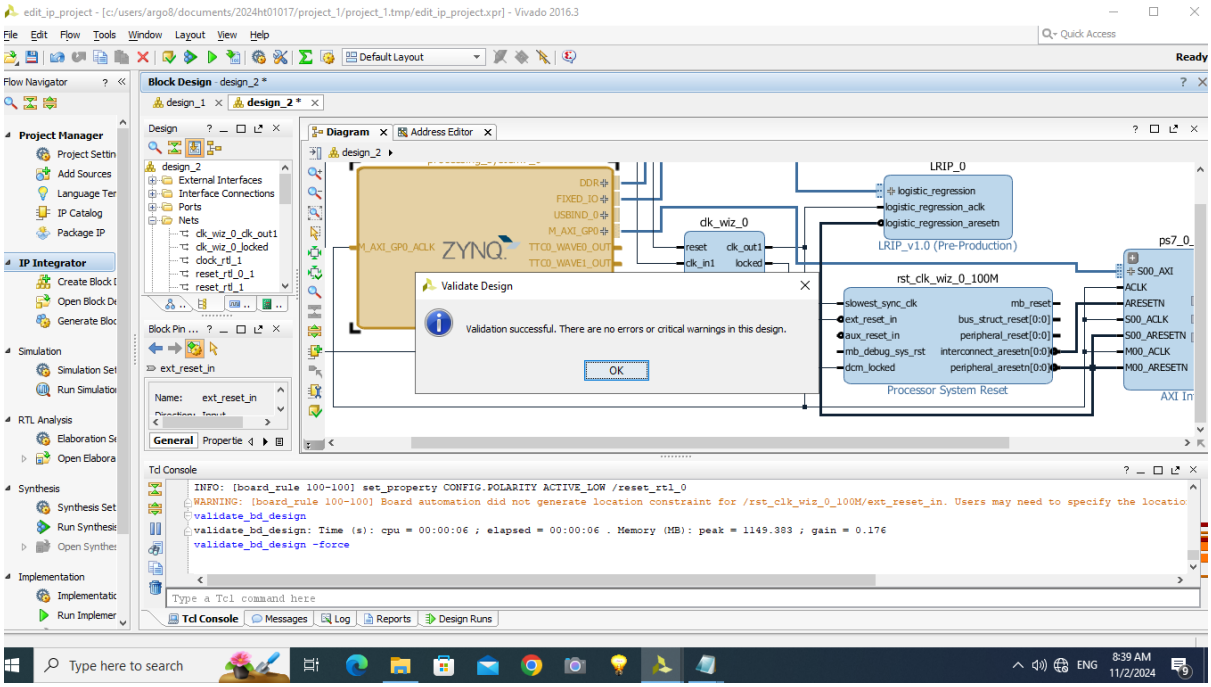


PS-PL Configuration: System integration required enabling specific interfaces between the PS and PL to ensure seamless interaction. The PS configuration in Vivado involved activating the GP AXI interfaces, bridging the ARM core and PL. This configuration allowed the ARM SoC to communicate directly with the LRIP by reading from and writing to the AXI memory-mapped registers of the LRIP.



AXI Connections for Data Flow: To ensure smooth data flow between the PS and PL, AXI GP ports were enabled and mapped in Vivado. The ARM core, acting as an AXI master, communicates with the LRIP (configured as the AXI slave). The GP interface was carefully configured and tested to ensure LRIP's various input/output pins, such as awaddr and wdata, were correctly connected to handle data inputs and outputs as expected.

Design Validation: The implemented logistic regression model, integrated with the IP, clocking wizard, and Zynq Processing System to manage PS-PL interactions, successfully passed validation in Vivado. The design showed no errors or critical warnings, indicating correct configuration of all IP blocks, clock connections, and AXI interfaces, readying the system for simulation and hardware deployment.


edit_ip_project - [c:/users/argo8/documents/2024ht01017/project_1/project_1.tmp/edit_ip_project.xpr] - Vivado 2016.3
File Edit Flow Tools Window Layout View Help
Quick Access
Default Layout
Ready
Flow Navigator
Project Manager
Project Settin
Add Sources
Language Ter
IP Catalog
Package IP
IP Integrator
Create Block I
Open Block De
Generate Bloc
Simulation
Simulation Set
Run Simulatio
RTL Analysis
Elaboration Se
Open Elabora
Synthesis
Synthesis Set
Run Synthesis
Open Synthes
Implementation
Implementatic
Run Implemer
Block Design - design_2 *
design_1
design_2 *
Design
design_2
External Interfaces
Interface Connections
Ports
Nets
clk_wiz_0_clk_out1
clk_wiz_0_locked
clock_rtl_1
reset_rtl_0_1
reset_rtl_1
Block Pin ...
ext_reset_in
Name: ext_reset_in
General
Diagram
Address Editor
design_2
DDR
FIXED_IO
USBIND_0
M_AXI_GP0
TTC0_WAVE0_OUT
TTC0_WAVE1_OUT
M_AXI_GP0_ACLK
ZYNQ
clk_wiz_0
reset
clk_in1
clk_out1
locked
LRIP_0
logistic_regression
logistic_regression_aclk
logistic_regression_aresetn
LRIP_v1.0 (Pre-Production)
ps7_0_
S00_AXI
ACLK
ARESETN
S00_ACLK
S00_ARESETN
M00_ACLK
M00_ARESETN
AXI In
rst_clk_wiz_0_100M
slowest_sync_clk
ext_reset_in
aux_reset_in
mb_debug_sys_rst
dcm_locked
mb_reset
bus_struct_reset[0:0]
peripheral_reset[0:0]
interconnect_aresetn[0:0]
peripheral_aresetn[0:0]
Processor System Reset
Validate Design
Validation successful. There are no errors or critical warnings in this design.
OK
Tcl Console
INFO: [board_rule 100-100] set_property CONFIG.POLARITY ACTIVE_LOW /reset_rtl_0
WARNING: [board_rule 100-100] Board automation did not generate location constraint for /rst_clk_wiz_0_100M/ext_reset_in. Users may need to specify the locatio
validate_bd_design
validate_bd_design: Time (s): cpu = 00:00:06 ; elapsed = 00:00:06 . Memory (MB): peak = 1149.383 ; gain = 0.176
validate_bd_design -force
Type a Tcl command here
Tcl Console
Messages
Log
Reports
Design Runs
Type here to search
ENG
8:39 AM
11/2/2024