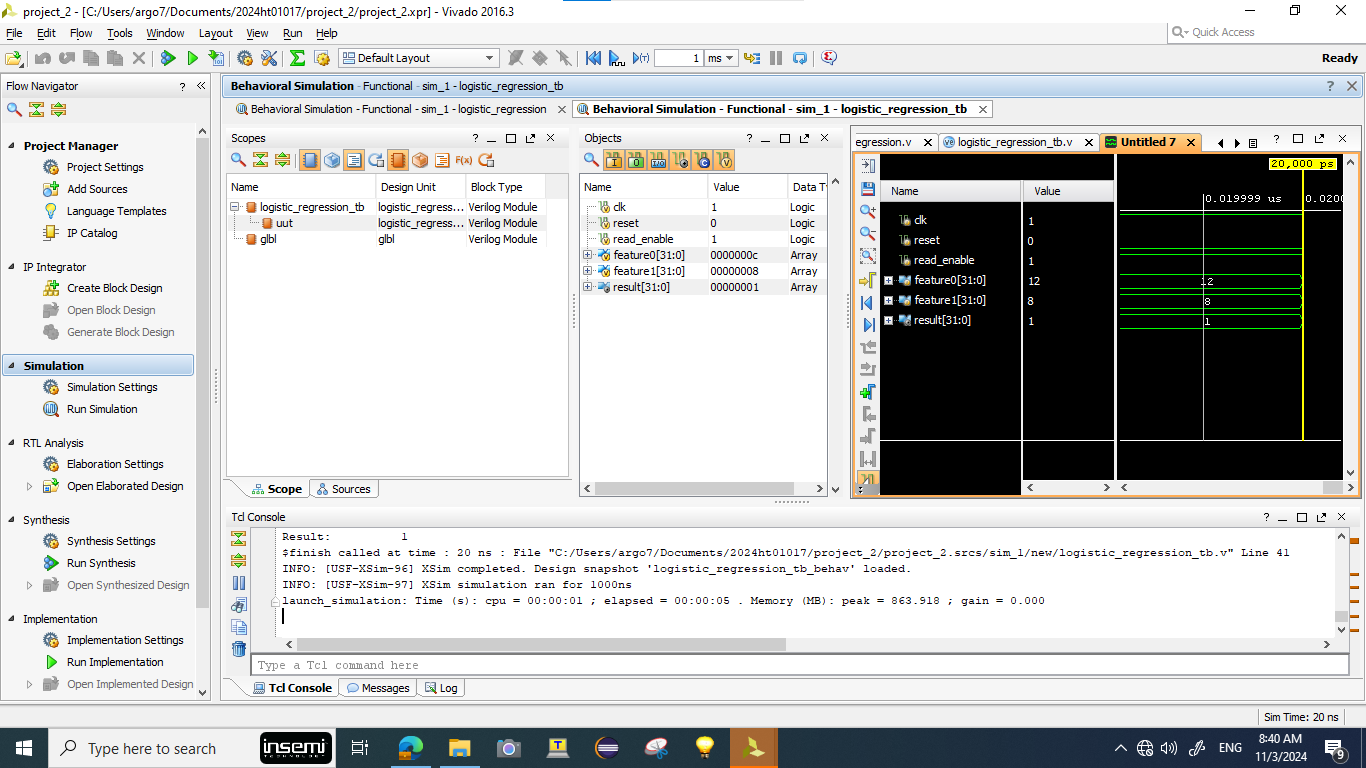
## Output for class =1



### Interpretation of the output

feature0 = 12

feature1 = 8

weight0 = 5

weight1 = -3

bias = 1

**Linear Combination Calculation:**

z= (weight0×feature0) + (weight1×feature1) +bias

z= (5×12)+(−3×8)+1 =60−24+1=37

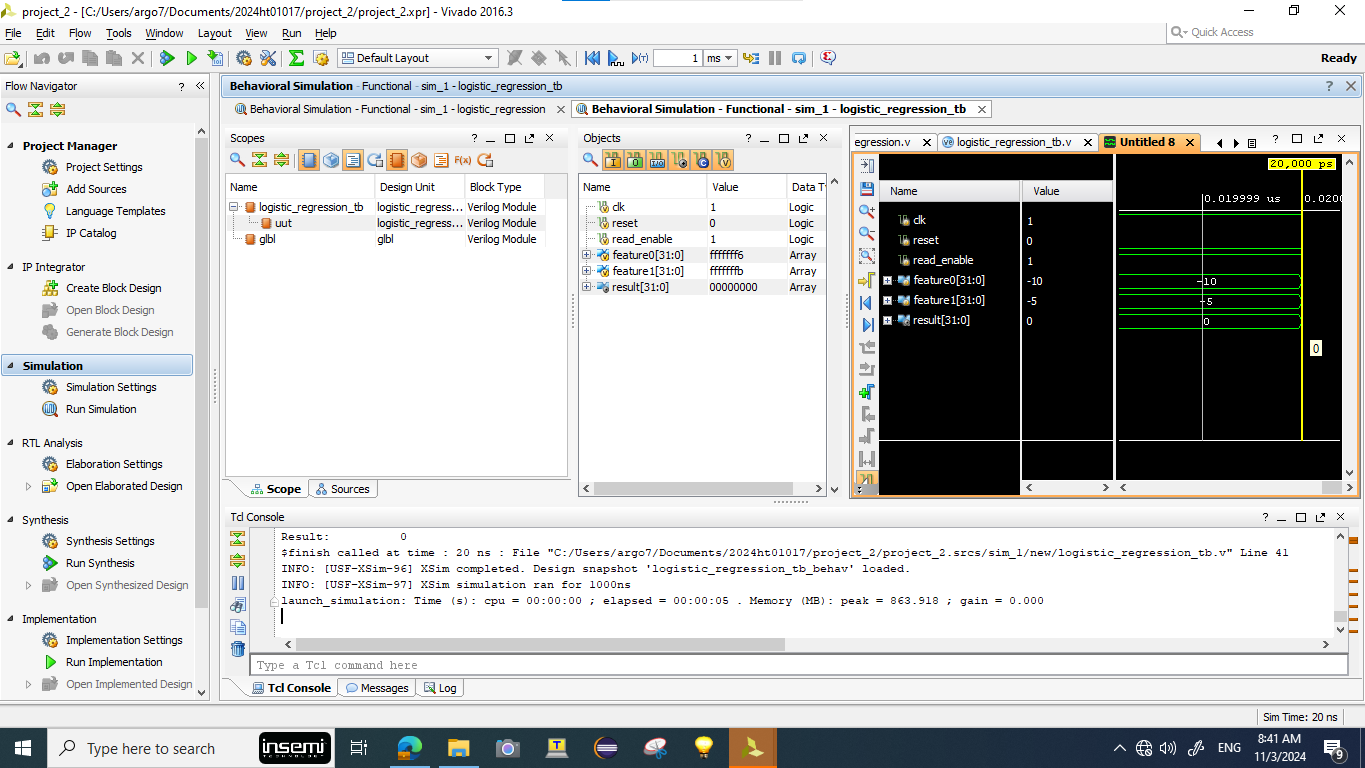
**Sigmoid Approximation:**

If z>0, then result=1

If z<0, then result =0

z=37>0 ----> result =1

## Output for class =0



### Interpretation of the output

feature0 = -10

feature1 = -5

weight0 = 5

weight1 = -3

bias = 1

**Linear Combination Calculation:**

z= (weight0×feature0) + (weight1×feature1) +bias

z= (5×−10) + (−3×−5)+1 = −50+15+1=−34

**Sigmoid Approximation:**

If z>0, then result=1

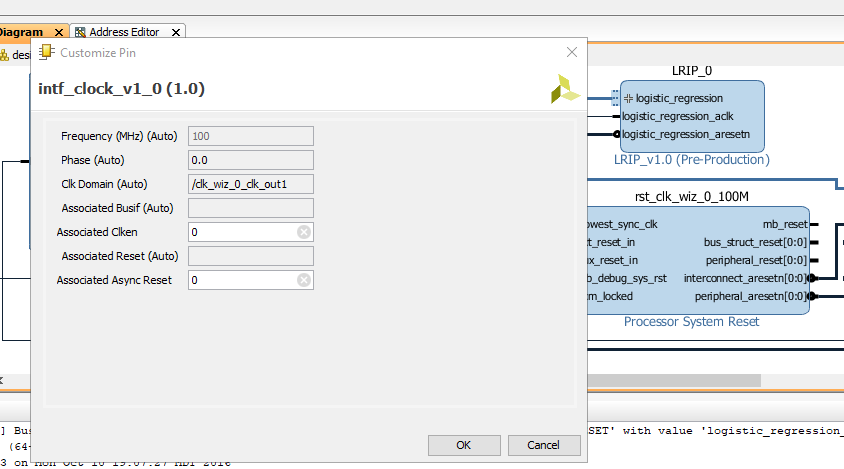
If z<0, then result =0

z=-34<0 --> so result =0

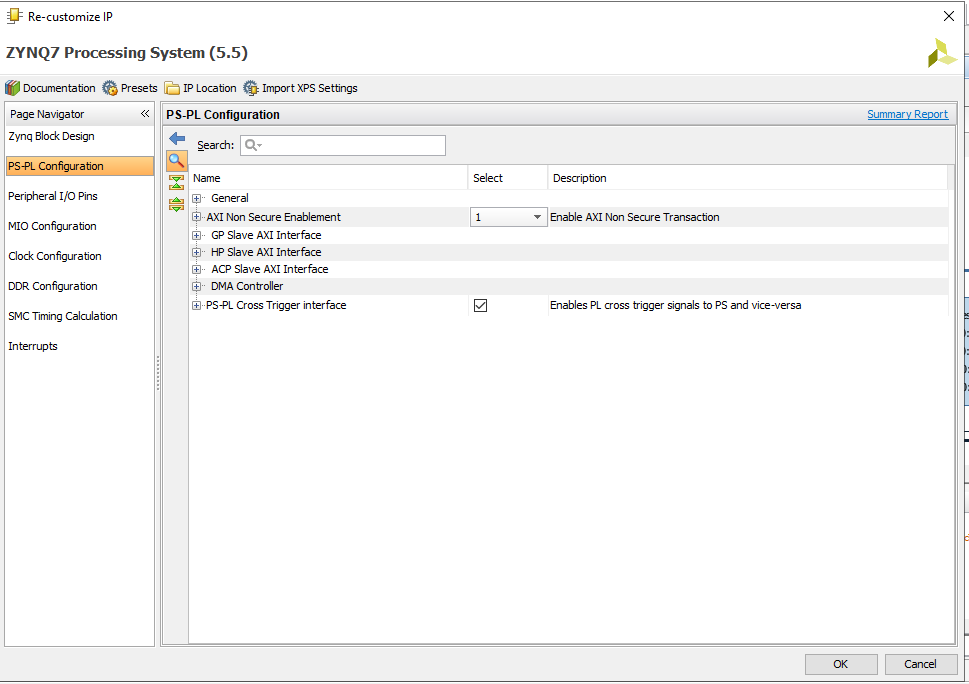
# Test Results

**Incorporating the custom Logic into the IP and re-packaging:** An IP named LRIP is created.The LRIP\_v1\_0\_logical\_regression.v code in the ‘hdl’ folder is replace with customized code. The IP is repackaged before adding it into the system design.

**Clock Configuration Using Clocking Wizard**: A stable clock signal was critical for the synchronous operation of LRIP in the PL. The Clocking Wizard was configured to generate the appropriate frequency, manually connected to the aclk input of the LRIP. This process included selecting the clock output from the wizard, checking frequency compatibility with the LRIP, and validating the connection through Vivado’s interface.



**PS-PL Configuration**: System integration required enabling specific interfaces between the PS and PL to ensure seamless interaction. The PS configuration in Vivado involved activating the GP AXI interfaces, bridging the ARM core and PL. This configuration allowed the ARM SoC to communicate directly with the LRIP by reading from and writing to the AXI memory-mapped registers of the LRIP.



**AXI Connections for Data Flow**: To ensure smooth data flow between the PS and PL, AXI GP ports were enabled and mapped in Vivado. The ARM core, acting as an AXI master, communicates with the LRIP (configured as the AXI slave). The GP interface was carefully configured and tested to ensure LRIP’s various input/output pins, such as awaddr and wdata, were correctly connected to handle data inputs and outputs as expected.

**Design Validation:** The implemented logistic regression model, integrated with the IP, clocking wizard, and Zynq Processing System to manage PS-PL interactions, successfully passed validation in Vivado. The design showed no errors or critical warnings, indicating correct configuration of all IP blocks, clock connections, and AXI interfaces, readying the system for simulation and hardware deployment.

