

$$b = 8.786 \times 10^{-9} \text{ cm}$$

FIELD EFFECT TRANSISTOR (FET):

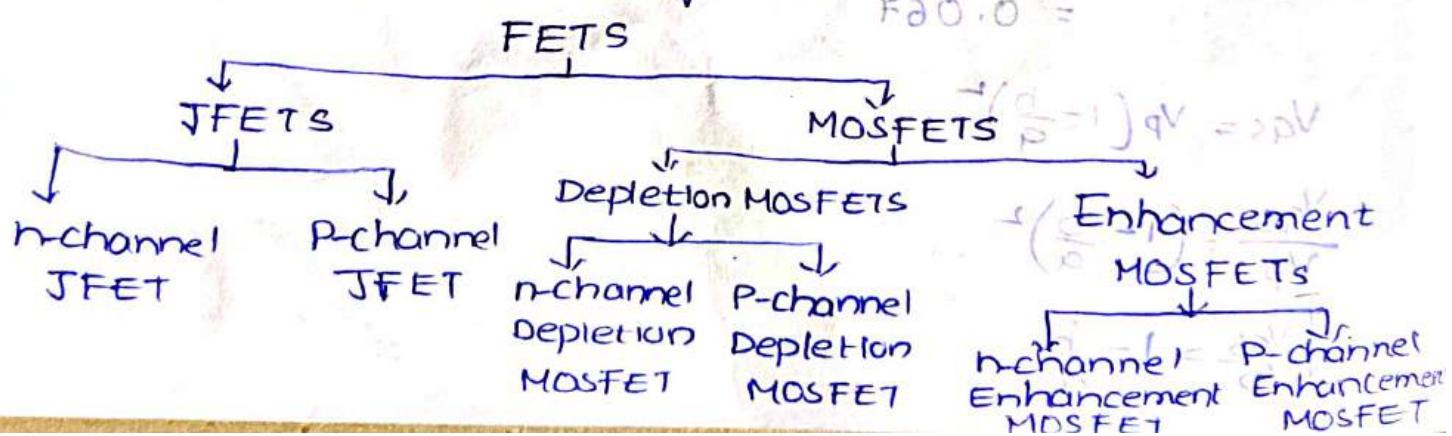
Introduction:-

The FET stands for field effect Transistor. It is a three-terminal solid state semiconductor device in which output current is controlled by an applied electric field. It is also called a unipolar transistor because in it the current is carried by only one type of carrier either electrons or holes, specially the majority carrier. The three terminals of a FET named as Drain (D), source (S) and gate (G).

The FET's are broadly classified into two categories

- i) Junction Field Effect Transistor (JFET) and
- ii) Metal Oxide Semiconductor Field Effect Transistors (MOSFET). It is also called Insulated Gate Field Effect Transistor (IGFET).

The FET's are categorised as:



Junction Field Effect Transistor (JFET)

(A) Symbols and Terminals:

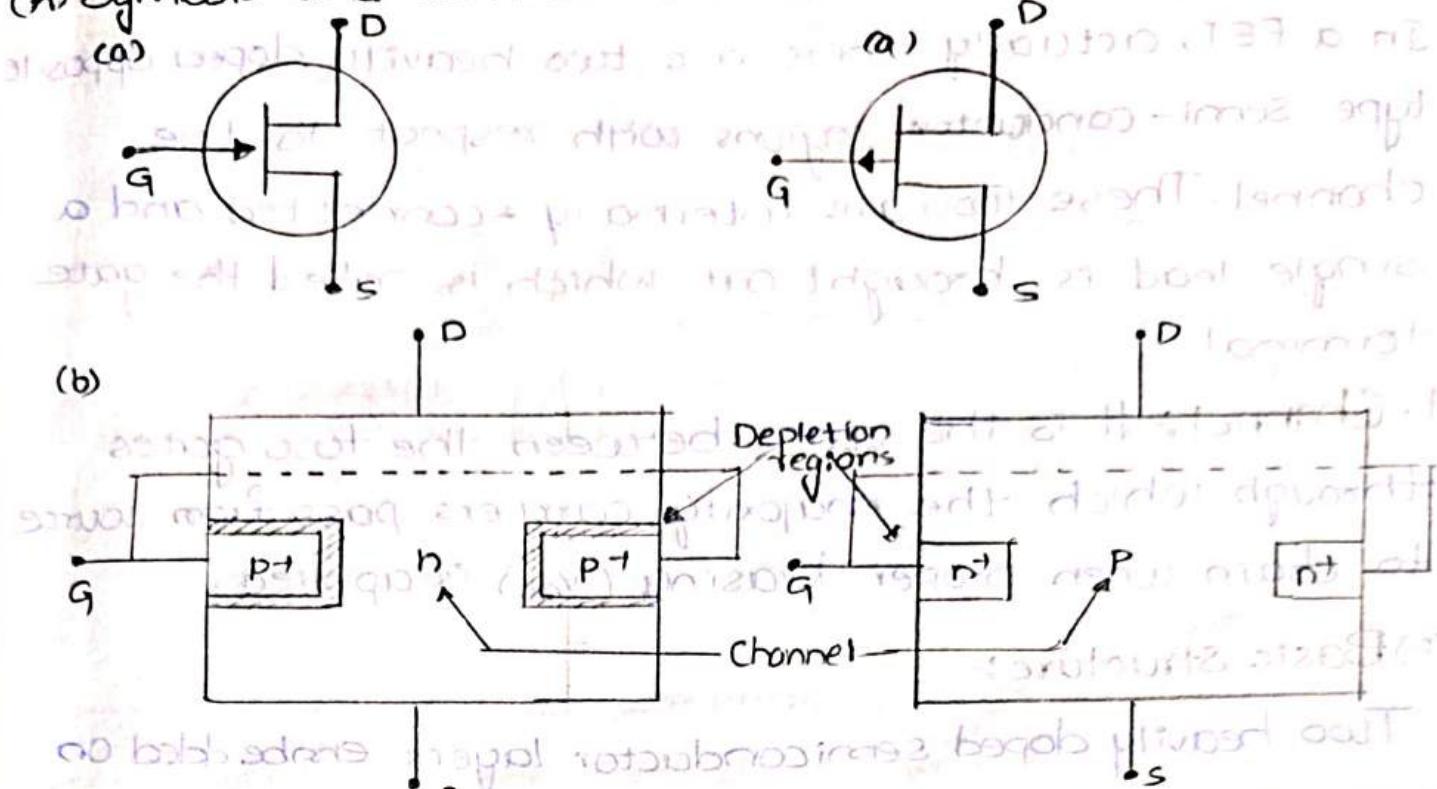


Fig: n-channel JFET

Fig: p-channel JFET

(a) Schematic symbol

(b) Schematic symbol

(b) Structure

The terminals of any FET, i.e., source, drain and gate, corresponds to the emitter, collector and base in BJT as follows:-

1. Source :- This is the terminal where the majority charge carriers enter the channel bar to provide current through the channel. The source corresponds to the emitter of BJT.

Source current is I_S .

2. Drain :- This is the terminal where the majority charge carriers leaves the channel bar. The drain corresponds to the collector of BJT. The drain current is I_D .

3. Gate :- This terminal corresponds to the base, terminal controls the conductance of the channel. In a FET, actually there are two heavily doped ^{opp} type semi-conductor regions with respect to the channel. These two are internally connected and single lead is brought out which is called the gate terminal.

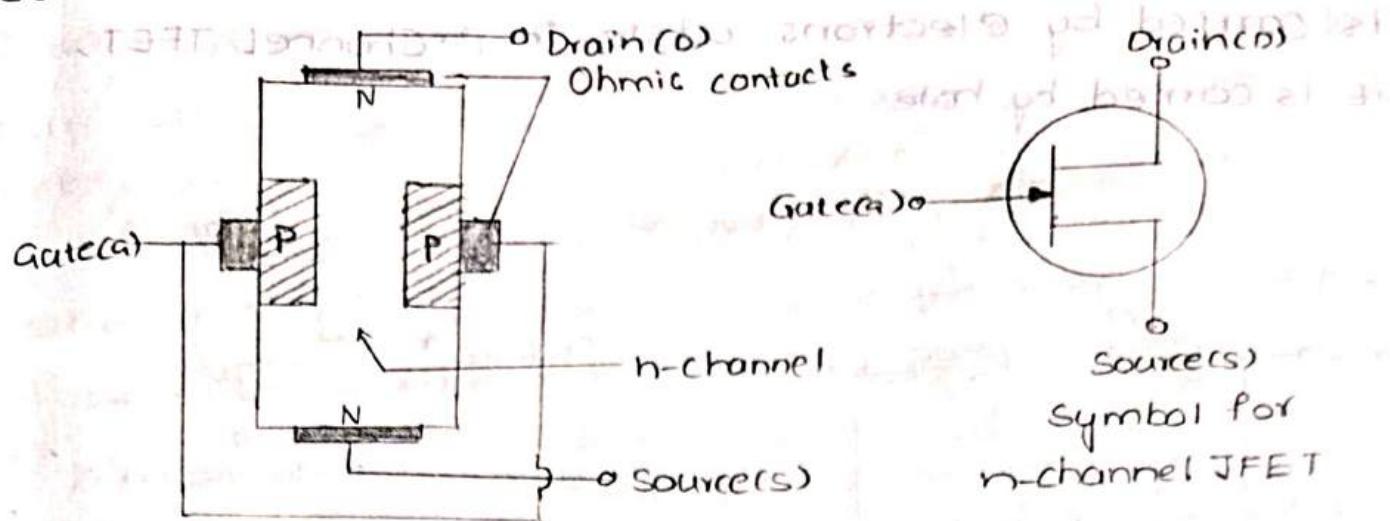
4. Channel : It is the space between the two gates through which the majority carriers pass from source to drain when proper biasing (V_{DS}) is applied.

(B) Basic Structure:-

Two heavily doped semiconductor layers embedded on both sides of small segment of lightly doped opposite semiconductor on its middle part such that two P-N junctions are formed. The area between the two opposite type semiconductors is referred to as channel. The top of the channel is connected through an ohmic contact to a terminal called Drain 'D' while the lower end of the channel is connected through an ohmic contact to a terminal called Source 'S'. The two opposite layers are internally connected and a single lead is brought out which is called the gate terminal.

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Construction of n-channel JFET:



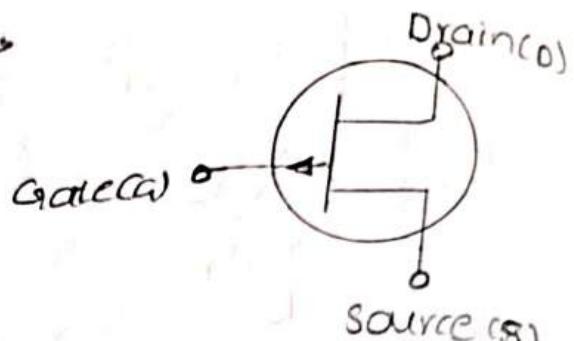
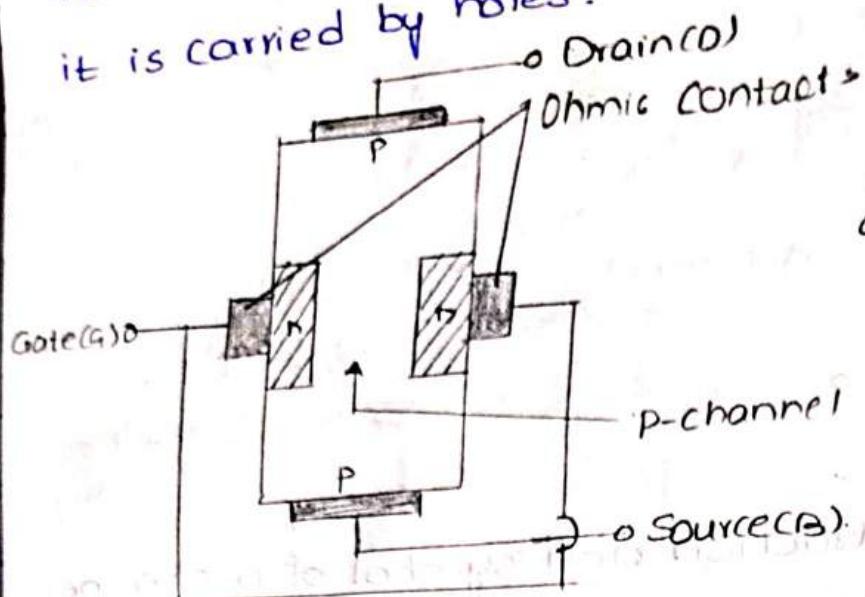
The figure shows construction and symbol of n-channel JFET. A small bar of extrinsic semiconductor material, n type is taken and its two ends, two ohmic contacts are made which is the drain and source terminals of FET. Heavily doped electrodes of P type material form P-n junctions on each side of the bar. The thin region between the two P gates is called the channel. Since this channel is in the n type bar, the FET is known as n-channel JFET.

The electrons enter the channel through the terminal called source and leave through the terminal called drain. The terminals taken out from heavily doped electrodes of p-type material are called gates. These electrodes are connected together and only one terminal is taken out, which is called gate, as shown in figure.

Construction of P-channel JFET:

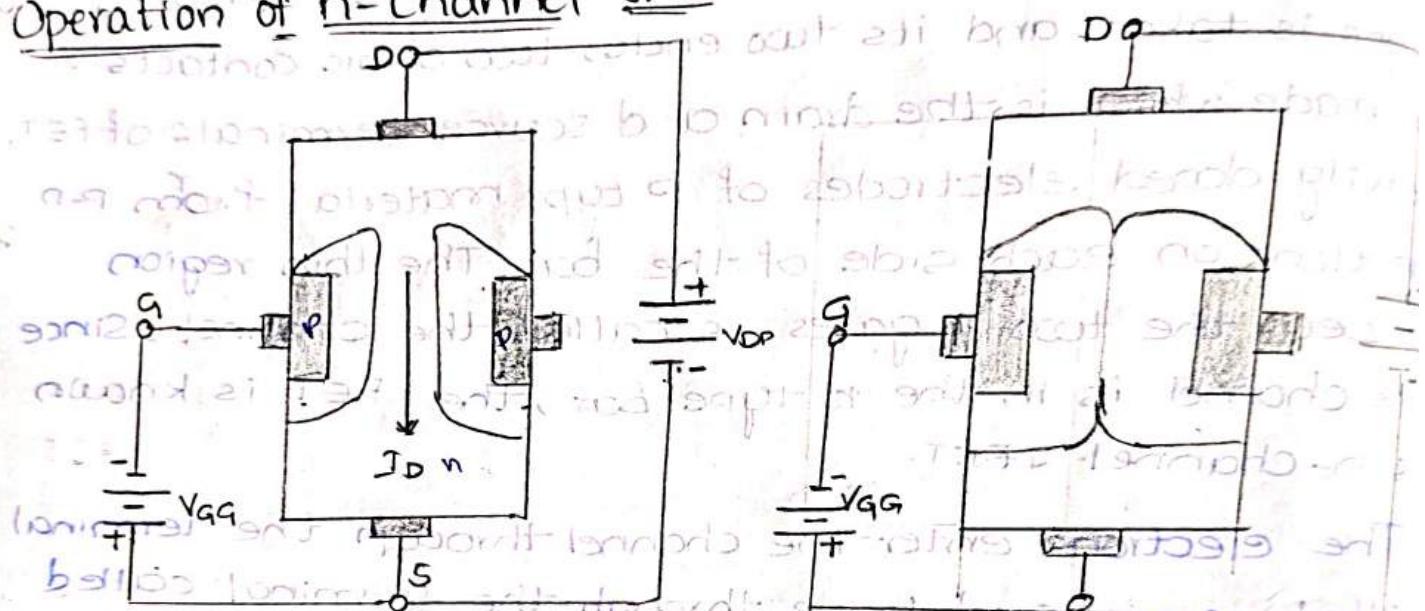
The device could be made of P type bar with two n type gates as shown in the figure. This will be P-channel JFET. The principle of working of n-channel JFET and P-channel JFET are similar. The only

difference being
is carried by electrons while
it is carried by holes.



Symbol for
p-channel JFET

Operation of n-channel JFET:



(a) V_{GS} is less (b) V_{GS} is more

Fig: Operation of n-channel JFET

→ The n-channel JFET is biased as shown in fig. The supply voltage given to the drain and source is called V_{DD} and the one that is applied between gate and source is called as V_{GS} . When no voltage is applied between drain and source or between gate and source, the channel width remains the same as there is no change in the depletion region width.

When a voltage is applied between the drain and source with a supply voltage V_{DD} , the electrons tend to flow from source to drain through the narrow channel that exists between the depletion regions. This causes drain current I_D to peak when no external voltage is applied between the gate and the source as it is called as I_{DSS} . This is illustrated in figure (a).

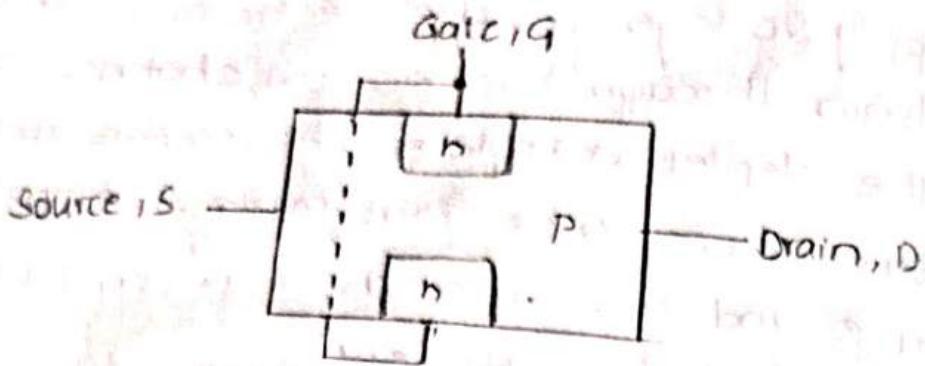
keeping the drain-to-source voltage V_{DS} at zero and V_{GS} decreasing it from zero, the reverse bias across the gate source junction is increased. Hence, the thickness of the depletion region increases. The voltage drop in the channel is greater at the source than at the drain.

Further, increases in V_{GS} along with increased reverse bias led to contact between the two depletion regions. In this state, the channel is said to be cutoff, and the drain current is reduced to zero. The gate-to-source voltage V_{GS} at which the drain current is zero is known as pinch-off voltage and is denoted by V_{POT} or $V_{GS(off)}$. This is illustrated in fig (b).

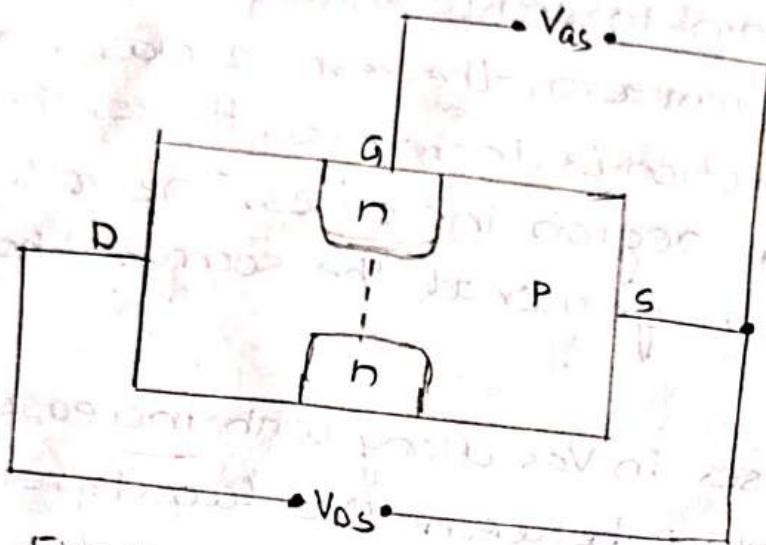
The value of pinch-off voltage is negative for n-channel JFETs. It depends on the doping of the channel regions and the width of the original channel. The operation of an p-channel JFET is similar to that of an n-channel JFET except that the current carriers are holes, and the polarities of the supply voltage are reversed.

JFETs can be used to switch off the circuit.

Operation of P-channel JFET:-



Fig(a): Layered structure of P-channel JFET



Fig(b): P-channel JFET in a biased state

Fig1 shows the layered structure of a p-channel JFET, and fig2 shows p-channel JFET in a biased state. The p-channel JFET exhibits a mode of operation that is similar to that of its counterpart, the n-channel JFET, except for a few differences.

In case of a p-channel JFET, the major portion of the device is made of p-type, into which are embedded the two small n-type regions. Thus, it has an n-type gate terminal and a p-type source and drain, causing the channel to be of the p-type, where the holes will be the majority charge carriers. Next, the direction of the arrow in its circuit symbol is pointing outward unlike in case of n-channel JFETs.

Similar to the case of n-channel JFETs, the working of these devices also depends upon the voltages applied at their terminals.

case - (i): If $V_{DS} = 0$ and $V_{GS} = 0$, the device will be idle with no current, i.e., $I_{DS} = 0$.

case - (ii): Now consider V_{GS} to be negative while V_{DS} is 0. At this state, the current flows from the source to the drain (as per conventional direction) as the holes within the p-substrate move towards the drain while being repelled from the source. The value of this current is restricted only by the channel resistance and is seen to increase with a decrease in V_{GS} (ohmic region). However, once the Pinch-off occurs ($V_{DS} = V_P$), the current I_{DS} saturates at a particular level of I_{DSS} , during which the device acts like a constant current source.

case - (iii): Next, let V_{GS} be positive while V_{DS} is negative. Here the effect exhibited is similar to that in case (ii) with the fact that the saturation occurs at a faster rate as the V_{GS} becomes more and more positive. Similar to that seen in n-channel JFETs, even here the current ceases to flow as the value of V_{DS} becomes equal to V_P , turning the device into an off state.

Clamping Circuit Theorem:

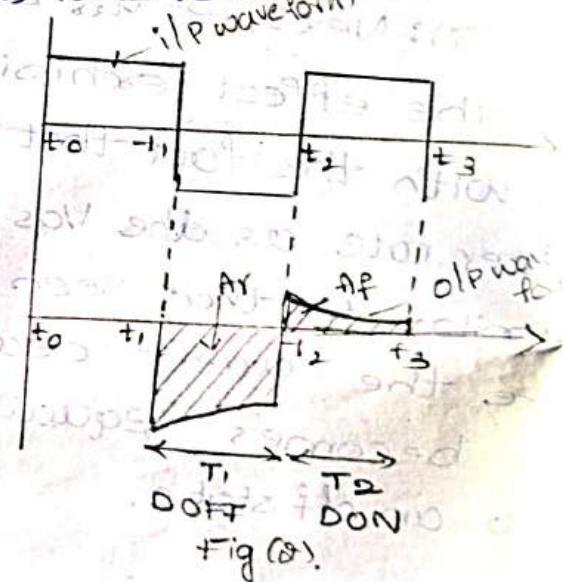
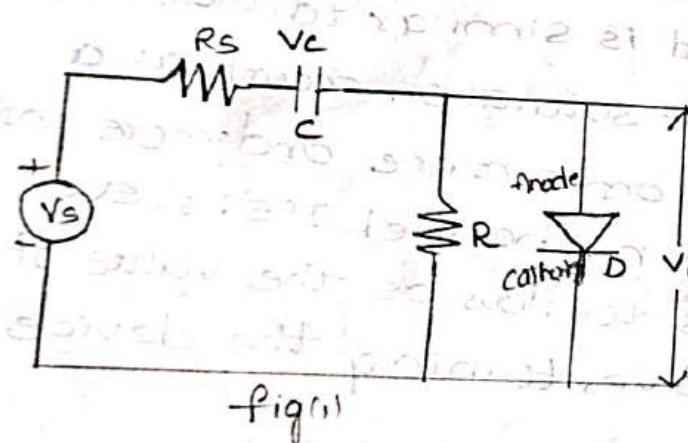
The theorem is related to the area under waveform in forward direction and the area under output waveform in reverse direction under steady condition.

Statement: Under steady state condition for any waveform the ratio of the area under the output curve in forward direction (when diode conducts) to the area under the output curve in reverse direction (when the diode doesn't conduct) is given by $\frac{A_f}{A_r} = \frac{R_f}{R}$

where A_f = Area under output waveform in forward direction
 A_r = Area under output curve in reverse direction

R_f = Forward resistance of the diode

R = Shunt resistance (or) load resistance.



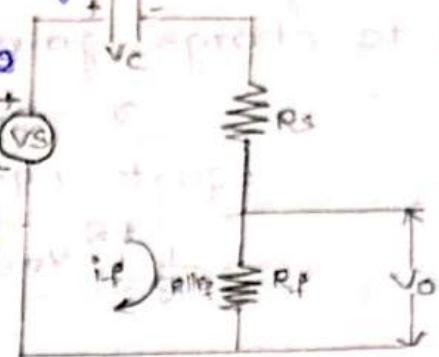
Proof:-

Consider the clamping circuit shown in the figure 1. The input applied is a square wave which produces the output waveform as shown in figure 2.

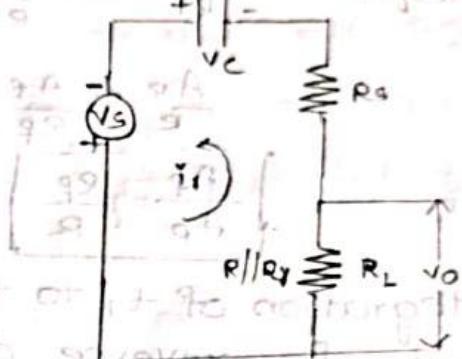
Let for first half cycle of input signal diode be ON, the equivalent circuit is shown in figure 3.

During period T_1 that is from t_1 to t_2 the diode is off.

Hence the capacitor discharges. Let i_f is the discharging capacitor current.



Fig(3)



→ The charge lost in the interval t_1 to t_2 is given by

$$Q_L = \int_{t_1}^{t_2} i_R dt$$

$$= \int_{t_1}^{t_2} \frac{V_R}{R} dt$$

$$Q_L = \frac{1}{R} \int_{t_1}^{t_2} V_R dt \quad \textcircled{1}$$

Where V_R = Reverse o/p voltage.

In the interval t_2 to t_3 the diode is ON the capacitor charges and regains the charge lost. Thus, if I_f is the charging current diode then charge gained

$$Q_L = \int_{t_2}^{t_3} i_f dt$$

$$= \int_{t_2}^{t_3} \frac{V_P}{R_P} dt$$

$$Q_L = \frac{1}{R_P} \int_{t_2}^{t_3} V_P dt \rightarrow \textcircled{2}$$

Where R_F = Forward resistance of diode
 Under study state conditions charge lost must be equal to charge gained that is,

$$Q_L = Q_C$$

equate eqn(1) & (2)

$$\frac{1}{R} \int_{t_1}^{t_2} V_F dt = \frac{1}{R_F} \int_{t_1}^{t_2} V_P dt$$

$$\frac{1}{R} \cdot A_R = \frac{1}{R_F} \cdot A_F$$

$$\frac{A_R}{R} = \frac{A_F}{R_F}$$

$$\boxed{\frac{A_F}{A_R} = \frac{R_F}{R}}$$

But integration of t_1 to t_2 $V_F dt$ equal to area under o/p for reverse direction when diode is OFF. i.e. equal to A_F .
 $\int_{t_2}^{t_3} V_F dt$ area under o/p forward direction when diode is ON. i.e A_F .

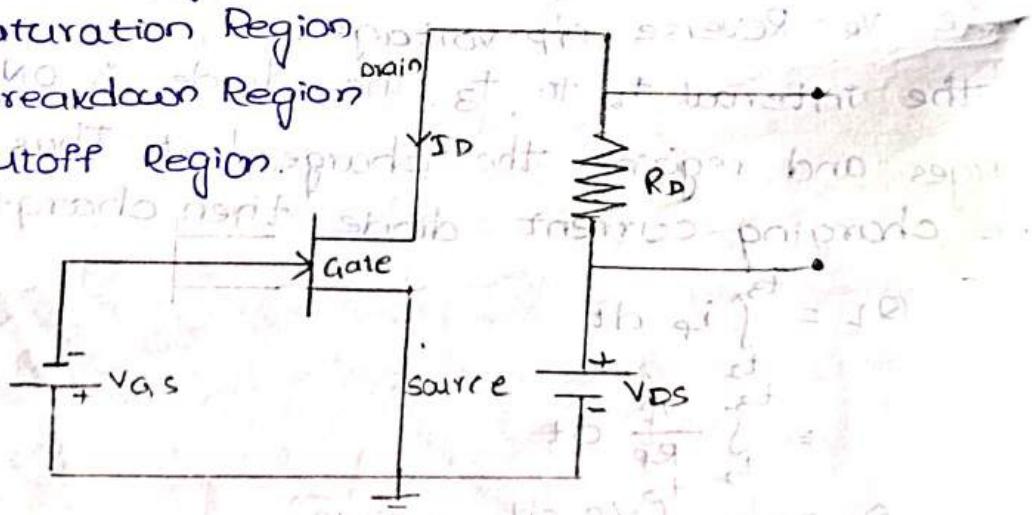
JFET as voltage variable Resistor:

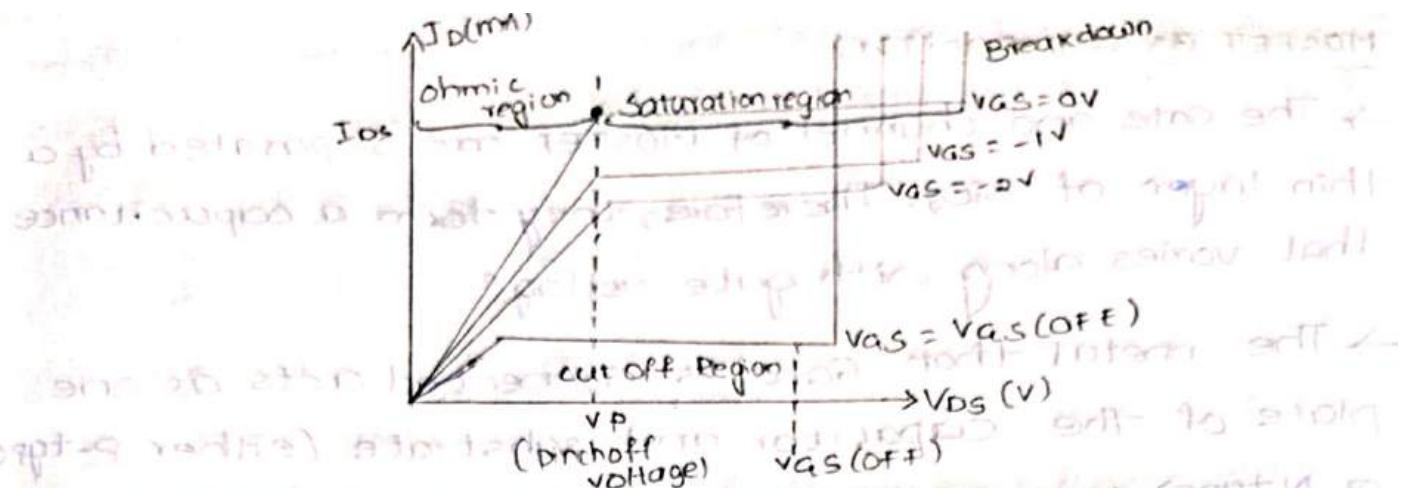
→ A JFET is a device that is usually operated in four regions i) Ohmic Region

ii) Saturation Region

iii) Breakdown Region

iv) Cutoff Region.





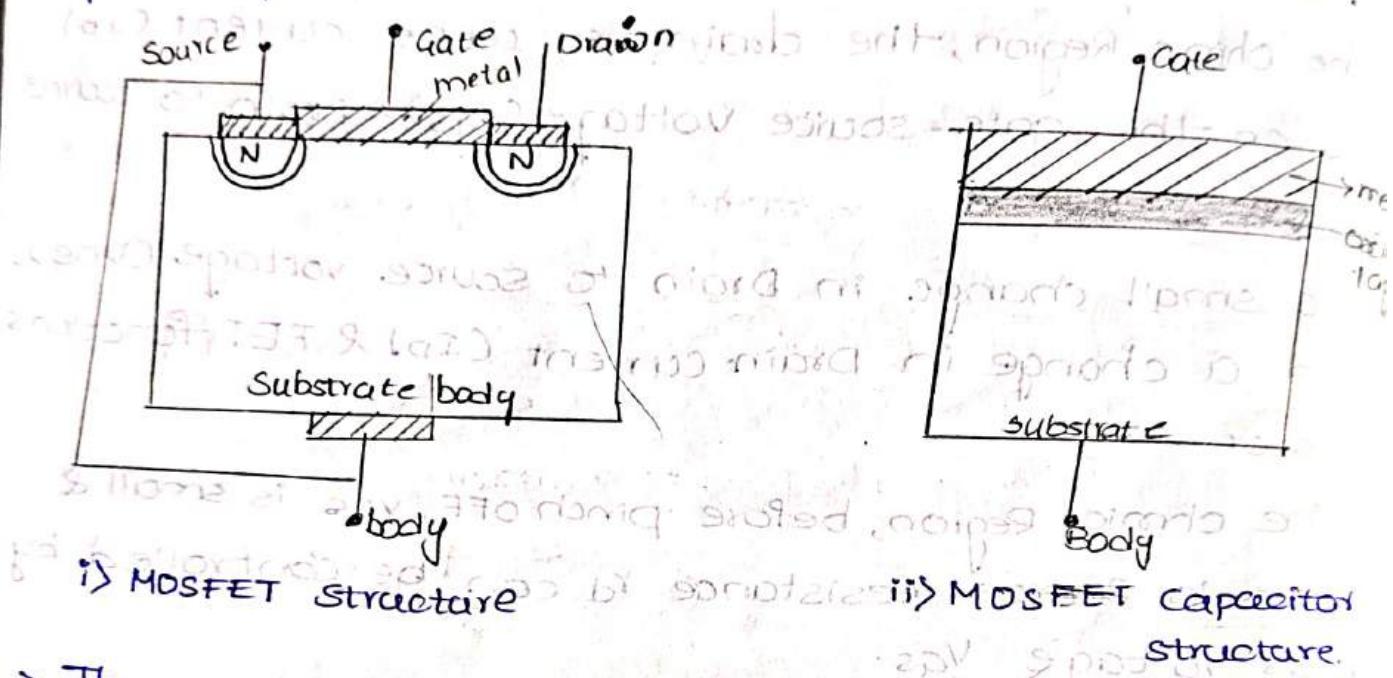
- In ohmic Region JFET acts as a voltage variable Resistor.
- In the ohmic Region, the drain-to source current (I_D) depends on the gate-source voltage (V_{GS}) & drain to source voltage (V_{DS}).
- For a small change in drain to source voltage (ΔV_{DS}), there is a change in drain current (ΔI_D) & FET functions as a resistor.
- In the ohmic Region, before pinch off, V_{DS} is small & the drain-to source Resistance r_d can be controlled by the bias voltage V_{GS} .
- The variation of Resistance with V_{GS} can be expressed as
$$r_d = \frac{r_0}{(1 + \frac{V_{GS}}{V_p})^2}$$

r_d = Particular drain Resistance
 r_0 = drain resistance at zero gate bias ($V_{GS} = 0$)
 V_{GS} = Gate to source voltage.
 V_p = Pinch off voltage

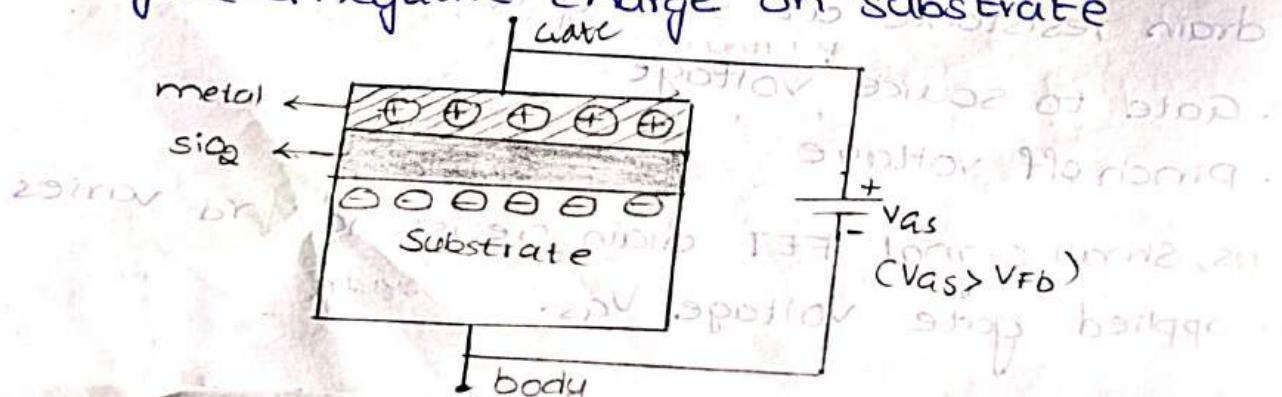
- Thus, Small signal FET drain resistance r_d varies with applied gate voltage V_{GS} .

MOSFET as a capacitor:

- The gate and channel of MOSFET are separated by thin layer of SiO_2 . Therefore, they form a capacitor that varies along with gate voltage.
- The metal that Gate is connected acts as one plate of the capacitor and substrate (either P or N type) acts as another plate and SiO_2 between capacitor plates acts as a dielectric constant.



- The capacitance of the mos capacitor depends upon the gate terminal voltage (i.e., +ve gate voltage).
- When the applied voltage is greater than the flat band voltage, the positive charge is accumulated on metal gate & negative charge on substrate.



→ When the applied gate voltage is larger than the flat band voltage, then negative charge is accumulate on metal gate & positive charge on substrate.

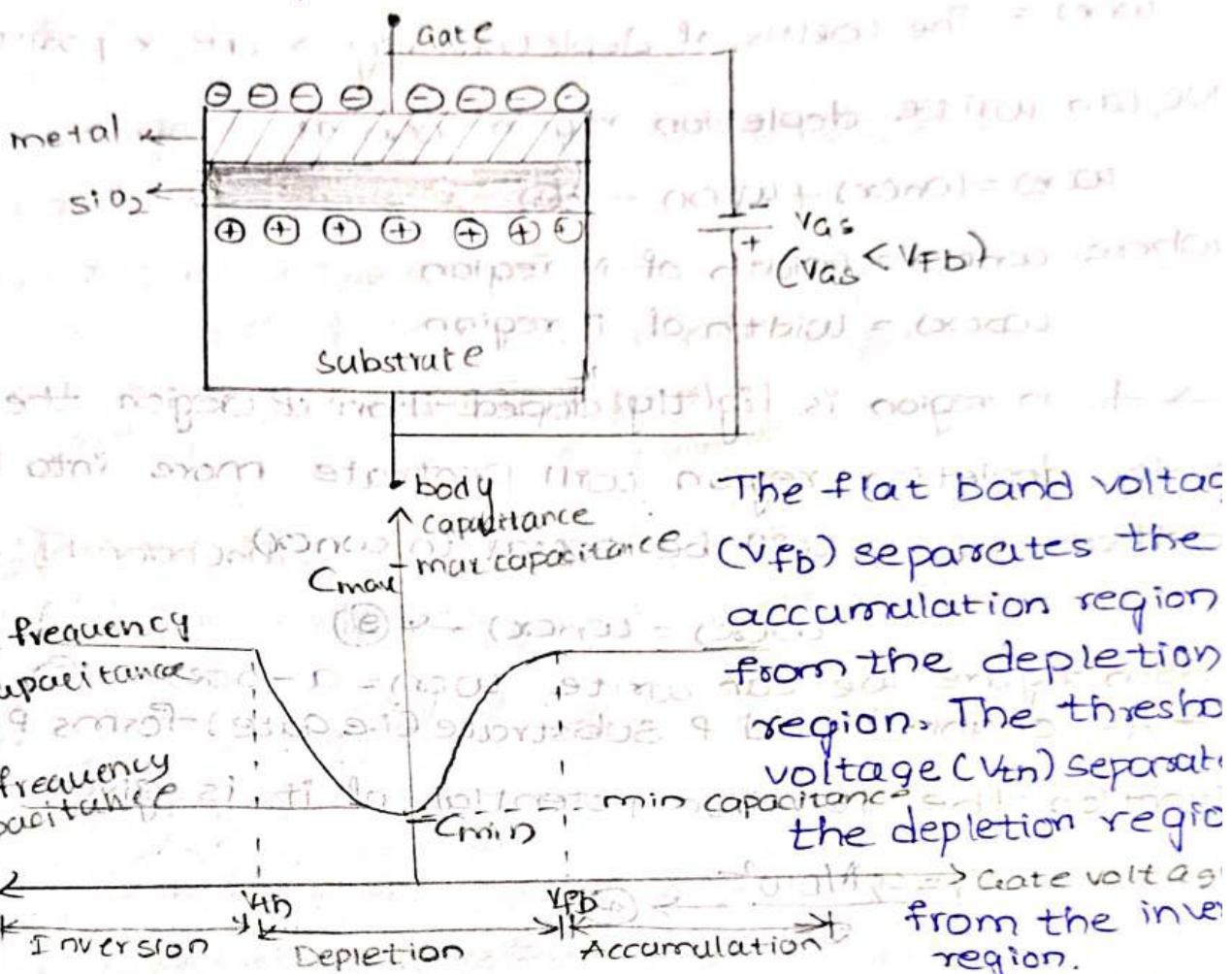
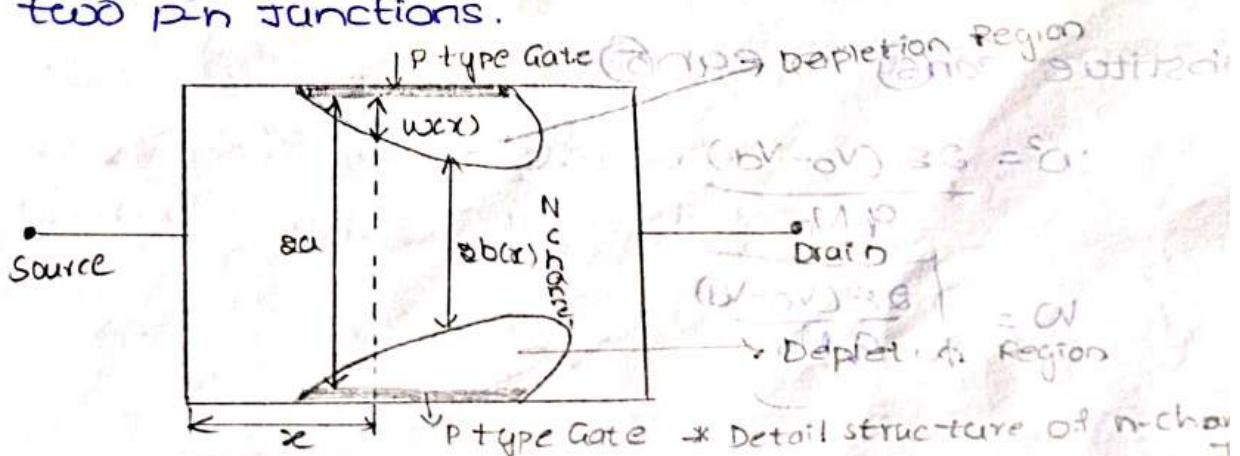


Fig: capacitance versus Gate voltage of a MOS capacitor.

Pinch off voltage (V_p) of JFET:

→ In N-channel JFET N type channel is sandwiched between two heavily doped P type substrate and create two PN junctions.



→ In the above figure,

$2a$ = Maximum available channel width

$2b(x)$ = Effective channel width

$w(x)$ = The width of depletion region at x position

We can write depletion region $w(x)$ as

$$w(x) = w_n(x) + w_p(x) \rightarrow ①$$

where $w_n(x)$ = width of N region

$w_p(x)$ = width of P region

→ As n region is lightly doped than P region the w of the depletion region will penetrate more into N. So that $w(x)$ will be equal to $w_n(x)$

$$w(x) = w_n(x) \rightarrow ②$$

From figure we can write $w(x) = a - b(x)$ → ③

→ As channel and P substrate (i.e. gate) forms PN Junction the Junction potential of it is given by

$$V_j = \frac{qN_D w^2}{2\epsilon} \rightarrow ④$$

$$w^2 = \frac{2\epsilon V_j}{qN_D} \rightarrow ⑤$$

The Junction potential $V_j = V_0 - V_d \rightarrow ⑥$

Where V_0 = contact potential

V_d = Reverse potential applied

Substitute eqn ⑥ in eqn ⑤

$$w^2 = \frac{2\epsilon (V_0 - V_d)}{qN_D}$$

$$w = \sqrt{\frac{2\epsilon (V_0 - V_d)}{qN_D}}$$

W = width of the depletion Region at position x' . so we can write $W = w(x)$.

so above equation will become

$$w(x) = \sqrt{\frac{2\epsilon(V_0 - V_d)}{qN_D}}$$

V_d = reverse gate voltage of PN junction at $x = V(x)$. Then, above eqn becomes

$$w(x) = a - b(x) = \sqrt{\frac{2\epsilon(V_0 - V(x))}{qN_D}} \quad (7) \quad [\because \text{from eqn (3)} \quad w(x) = a - b(x)]$$

where ϵ = Permittivity of channel

q = charge of the electron.

V_0 = Junction contact potential

$V(x)$ = Applied reverse voltage across depletion region at x' .

$a - b(x)$ = Penetration of depletion region into channel at x' .

Assume that Pinchoff occurs and when pinch off occurs effective channel width $b(x)$ will be zero and $V(x) = V_p$

Now equation (7) becomes

$$a = \sqrt{\frac{2\epsilon(V_0 - V_p)}{qN_D}}$$

Squaring on both sides

$$a^2 = \frac{2\epsilon(V_0 - V_p)}{qN_D}$$

$$a^2 q N_D = 2\epsilon (V_0 - V_p)$$

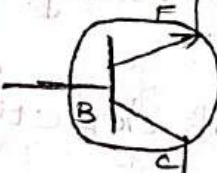
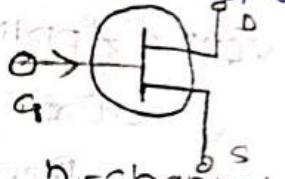
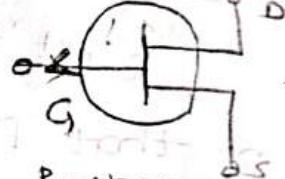
$$V_0 - V_p = \frac{q N_D a^2}{2\epsilon}$$

$V_0 \ll V_p$ so we can neglect V_0 . then,

$$-V_p = \frac{q N_D a^2}{2\epsilon}$$

$$|V_p| = \frac{q N_D a^2}{2\epsilon}$$

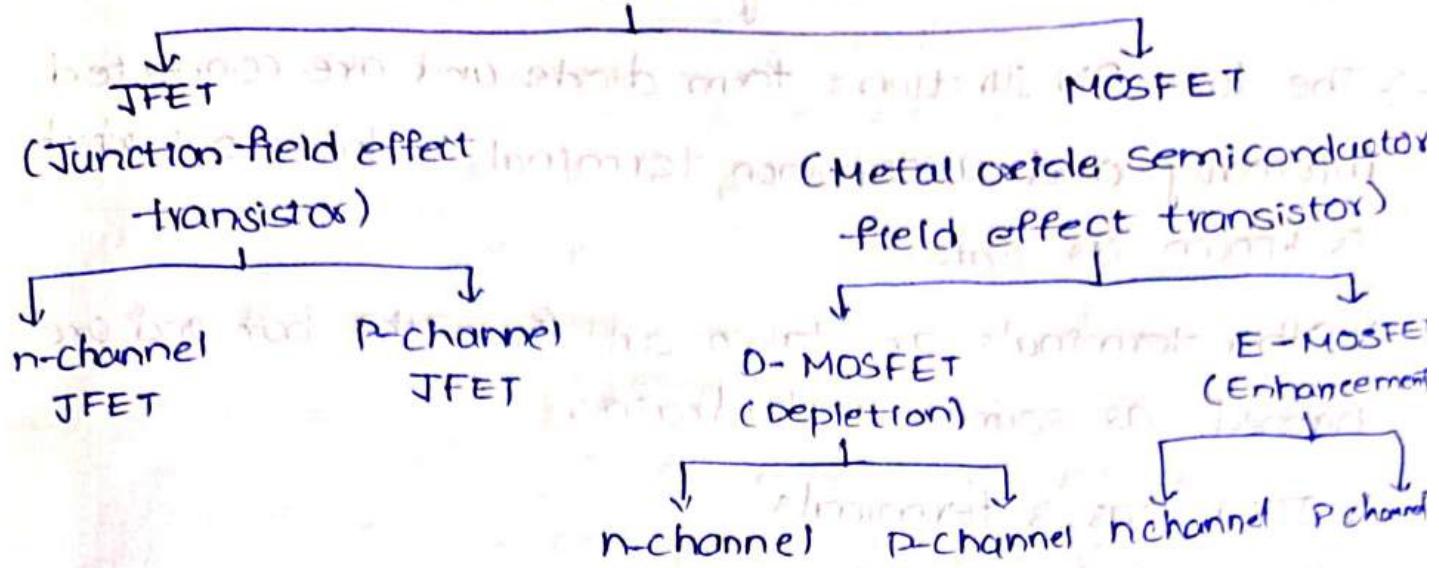
Comparison of BJT and FET:

S.No	Parameter	BJT	FET
1.	control element	current controlled device i/p current I_B controls o/p current I_C	voltage controlled device i/p voltage V_{GS} controls o/p current I_D
2.	Device type	current flows due to both majority and minority carriers, hence bipolar device	current flows due to majority carriers and hence unipolar device
3.	Types	NPN and PNP	n-channel & p-channel
4.	Symbols	 	 
5.	configurations	CB, CE, CC	CD, CS, CG
6.	Input resistance	less	high
7.	Size	Bigger than JFET	Smaller in contrast than BJT, thus making them useful in integrated circuits
8.	sensitivity	Higher sensitivity to changes in the applied signals	Less sensitivity to changes in the applied voltage
9.	Thermal stability	less	more

10. Thermal runaway	Exists in BJT, because of cumulative effective drain resistance R_d of increase in I_C with increases with temperature resulting in the device.	Does not in JFET, because increasing temperature I_D , reducing the I_D and hence the temperature of the device.
11. Relation b/w ΔI_P & linear	ΔI_P	non-linear
12. Ratio of ΔI_P to I_P	$\beta = \frac{\Delta I_C}{\Delta I_B}$	$\eta_{ro} = \frac{\Delta I_D}{\Delta V_{GS}}$
13. Thermal noise	more in BJT, as more charge carriers cross junction.	Much lower in JFET as very few charge carriers cross the junction.

Types of field effect transistors

Different types of Field effect transistors



* JFET construction and working of N-channel JFET

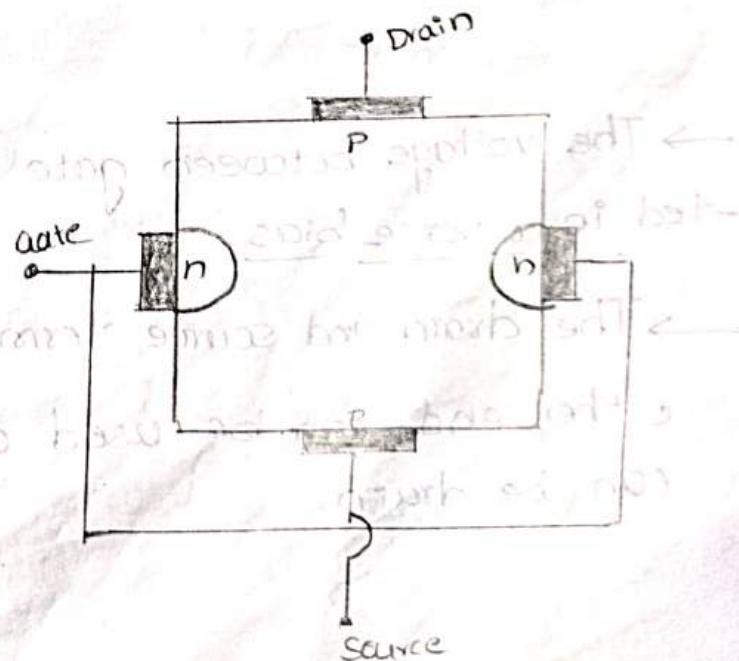
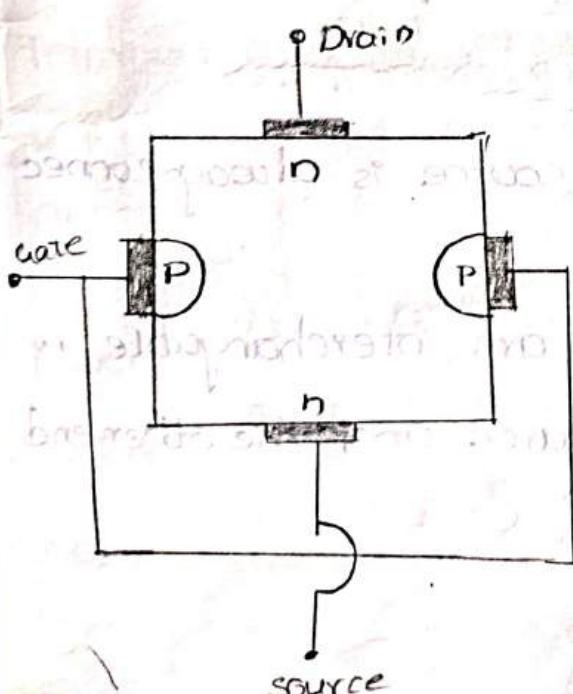
(or)

construction and operation of JFET / construction of JFET

→ A JFET consists of P-type or n-type silicon bar containing two PN junctions at the sides and this bar forms the conduction channel for the charge carriers.

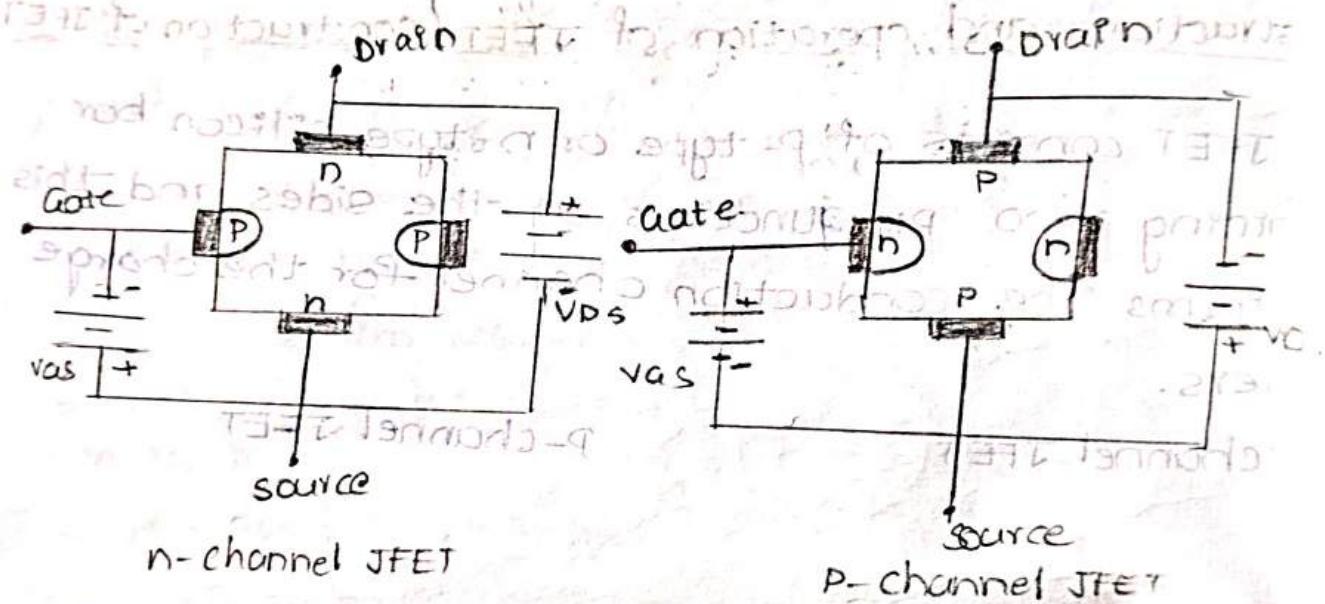
N-channel JFET

P-channel JFET



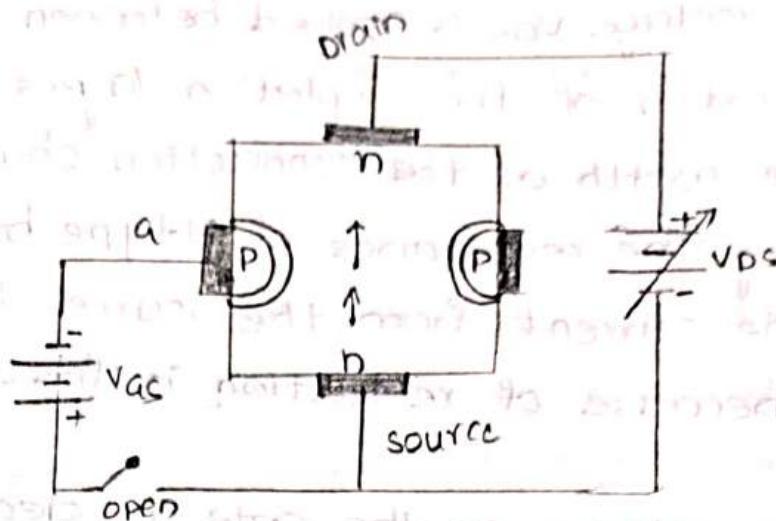
- If the bar is of n-type it is called n-channel, and if the bar is of p-type it is called p-channel;
- and if the bar is of p-type form diode and are connected.
- The two PN junctions form diode and are connected internally and a common terminal is taken out which is known as Gate.
- Other terminals are taken out from the bar and are named as source and drain.
- JFET has 3 terminals.
Drain, Gate, Source.

JFET polarities

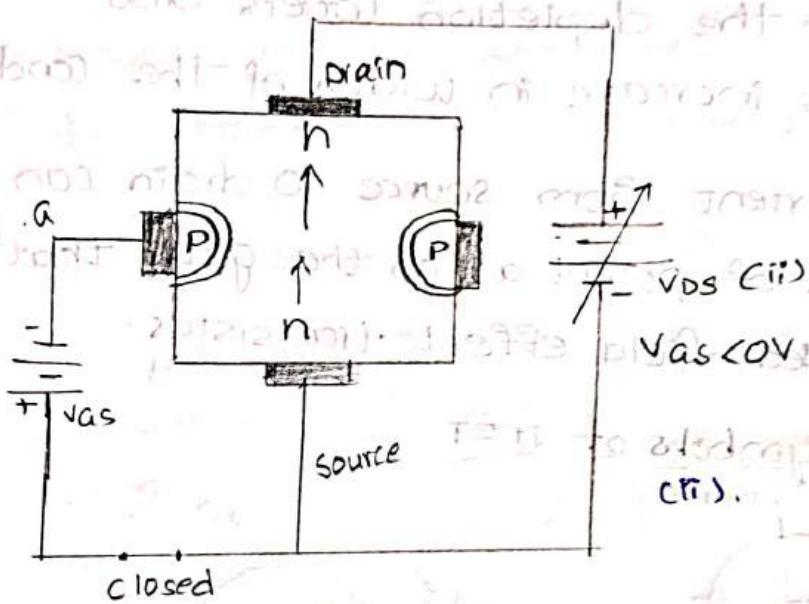


- The voltage between gate and source is always connected in reverse bias.
- The drain and source terminals are interchangeable either end can be used as source and the other end can be drain.

Working principle of JFET :-



i) $V_{GS} = 0V$



(i)

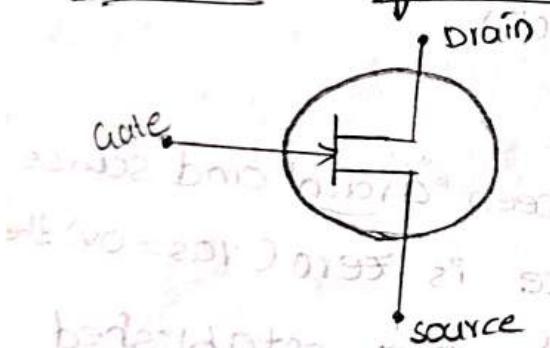
→ When a voltage V_{DS} is applied between drain and source terminals and the voltage on the gate is zero ($V_{GS}=0V$) the two PN junctions at the sides of the bar established depletion layers the electrons will flow from source to drain through a channel between the depletion layers.

→ The side of these layers determines the width of the channel and hence the current conduction through the bar is controlled.

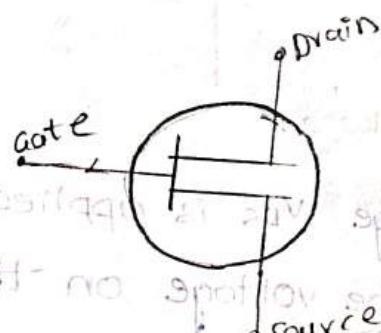
(ii)

- When a reverse voltage V_{GS} is applied between the gate and source the width of the depletion layers is increased, this reduces the width of the conduction channel thereby increasing the resistance of N-type base consequently the current from the source to drain is decreased because of reduction in the channel.
- If the reverse voltage on the gate is decreased the width of the depletion layers also decreases, hence there is increase in width of the conduction channel.
- In FET, current from source to drain can be controlled by application of potential on the gate that's why the device is called field effect transistors.

Schematic symbols of JFET



fig(i): n channel JFET



fig(ii): p - channel JFET

→ If the channel is n-type the arrow on the gate points towards the channel as shown in fig(i).

→ For p-type channel the arrow on the gate points from the channel to gate as shown in fig(ii).

Merits of JFET Over BJT

(a)

Difference between JFET and Bipolar transistor

- In a JFET there is only one type of case - Holes in the p-type channel and electrons in n-type channel. Due to this reason, it is called a unipolar transistor. In ordinary transistors, both holes and e⁻ participate in conduction so it is called a bipolar transistor.
- As the input circuit of the JFET is reverse biased, it offers high input impedance whereas the input circuit of an ordinary transistor is forward biased and offers low input impedance.
- In JFET, gate to source voltage controls the drain current. For this reason, JFET's are also called voltage control devices whereas an ordinary transistor the base current controls the output current that's why they are called as current control device.
- In JFET there are no junctions as in ordinary transistor the conduction is through an n-type or p-type semiconductor materials. For this reason, noise level in JFET is very small.
- FET's have better thermal stability.
- In integrated circuit form, FET's are fabricate and occupy less space.

Disadvantages or Limitations of JFET over BJT:

- The main draw back of JFET's is that they have smaller gain bandwidth product when compared to BJT.

(i) Application of FET:

→ 1) can be used as a buffer amplifier.

2) Phase shift oscillator.

3) In voltmeters.

As a buffer amplifier:

It isolates the preceding stage from the following cause of high input impedance and low output impedance. FET acts as an excellent buffer amplifier.

Phase shift oscillators:

The high input impedance of FET is especially valuable phase shift oscillators to minimize loading effect.

In voltmeters:

The high input impedance of FET is useful in voltmeter to act as input stage.

Applications of BJT:

1) used in logic circuits

2) used as an oscillator

3) used as an amplifiers

4) used as a multivibrator

5) used as detector or demodulator

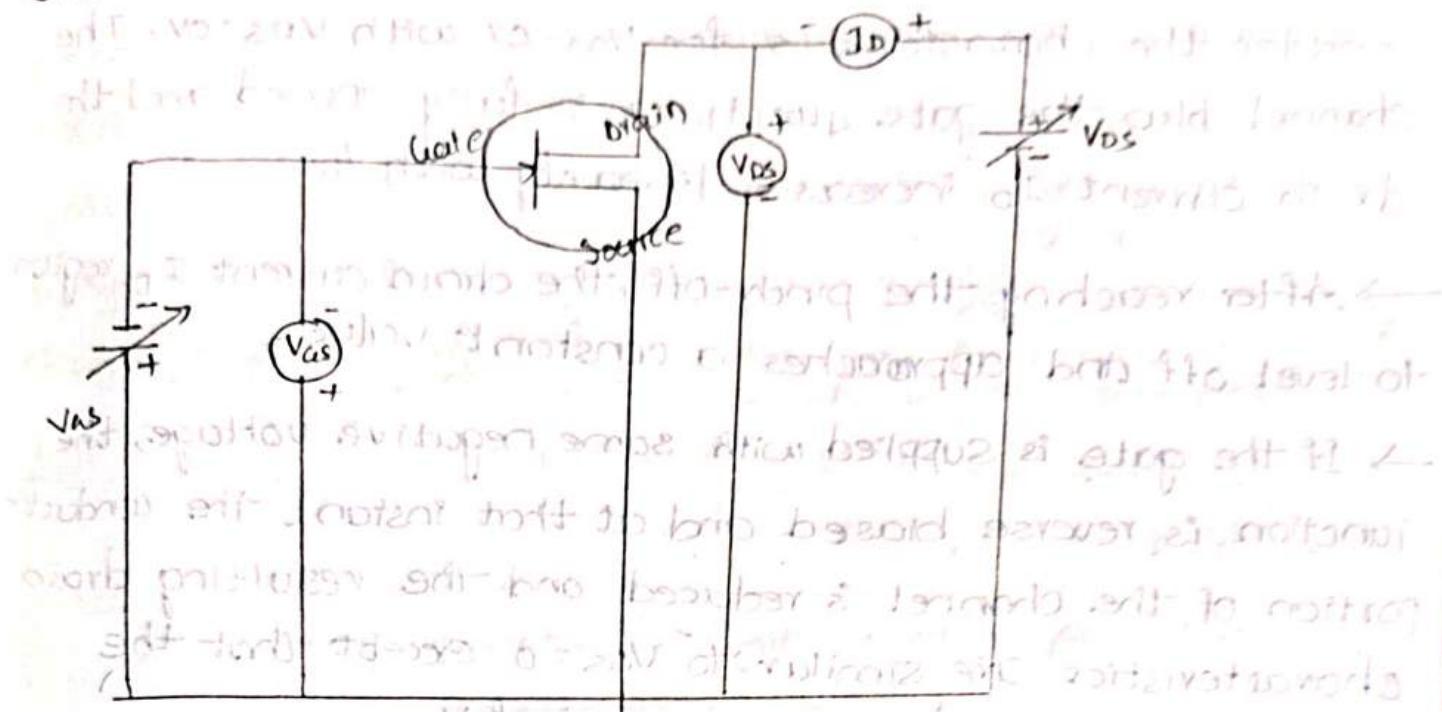
6) Also used as modulator

7) For wave shaping it is used in clipping circuits.

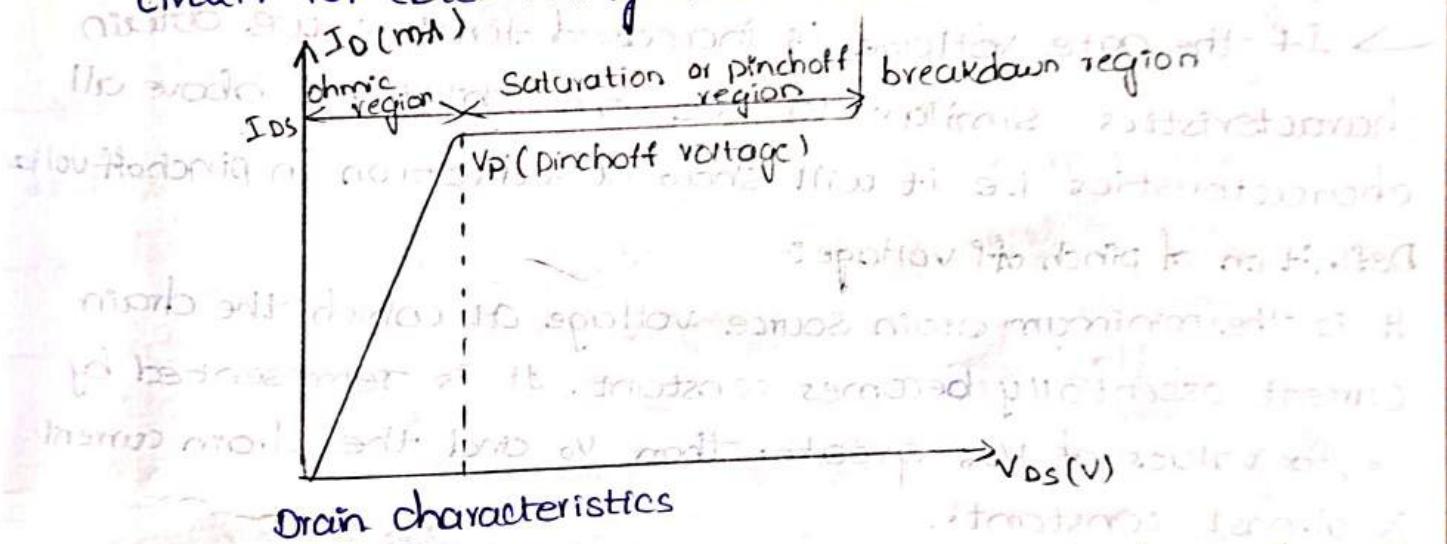
8) Used in switching circuits.

9) Used in timer and time delay circuits.

Drain characteristics of JFET:



Circuit for determining drain characteristics



- The curve between drain current (I_D) and drain source voltage (V_{DS}) of a FET at constant gate source voltage V_{GS} is called drain or output characteristics of FET.
- keep V_{GS} fixed at some value and change the drain source voltage in steps and notedown the corresponding drain current I_D . Plotting these values on a graph gives the op characteristics of FET.

→ To understand the nature of drain characteristics, let consider the characteristics for $V_{GS} = 0V$ with $V_{DS} = 0V$. If channel below the gate junctions is fully opened and drain current I_D increases linearly with V_{DS} .

→ After reaching the pinch-off, the drain current I_D begins to level off and approaches a constant value.

→ If the gate is supplied with some negative voltage, the junction is reverse biased and at that instant the conductive portion of the channel is reduced and the resulting drain characteristics are similar to $V_{GS} = 0$ except that the pinch-off occurs at smaller values of V_{DS} .

→ If the gate voltage is increased further, we obtain characteristics similar to the one obtained above all characteristics i.e. it will show a reduction in pinch-off voltage.

Definition of pinch off voltage:-
It is the minimum drain source voltage at which the drain current essentially becomes constant. It is represented by V_p , for values of V_{DS} greater than V_p and the drain current is almost constant.

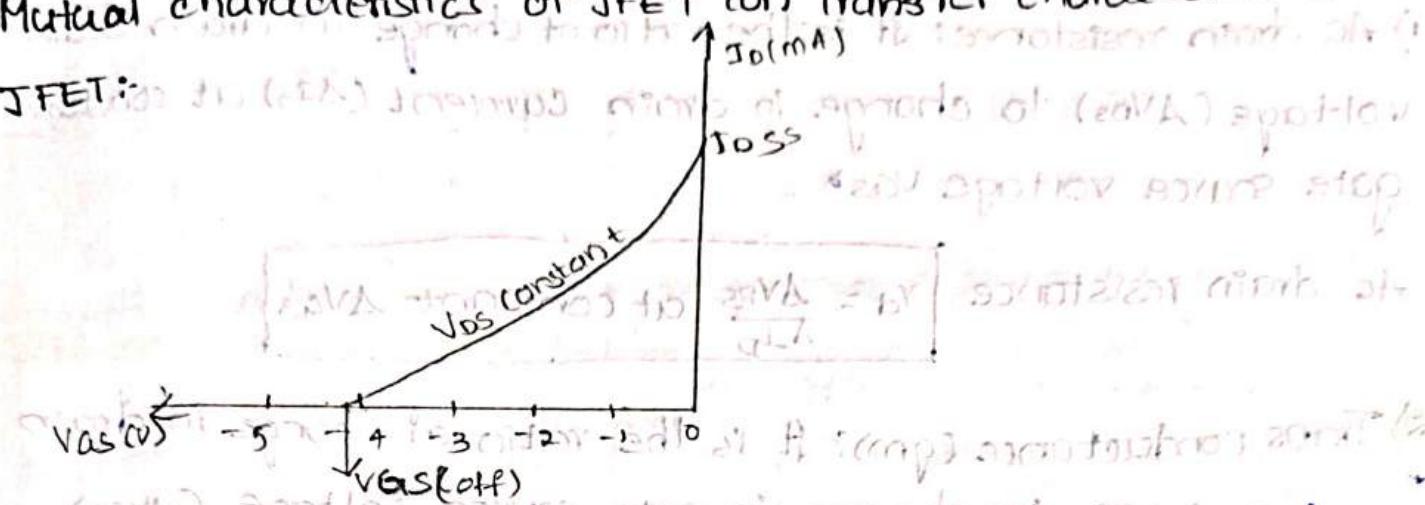
Various regions of drain characteristics:-

Ohmic region:- This part of the characteristics is linear indicating that for low values of V_{DS} current varies directly with voltage following Ohm's law.

Pinch-off region or Saturation region:- In this region JFET acts as a constant current source. It is also called as amplified region.

Breakdown region: If V_{DS} is increased beyond its value (JFET) enters into breakdown region where I_D increases to an excessive value. This happens because the reverse biased gate channel PN junction undergoes avalanche breakdown when small change in V_{DS} produces large change in I_D .

Mutual characteristics of JFET (or) Transfer characteristics of JFET:



- It is a plot of I_D versus V_{GS} for a constant value of V_{DS} .
- It is similar to the trans conductance of transistor.
- It is seen that when $V_{GS}=0$ then I_D equal to I_{DSS} ($I_D=I_{DSS}$)
- Gate to source cut off voltage i.e $[V_{GS(off)}]$ under Gate to source cut off voltage i.e $[V_{GS(off)}]$ trans characteristics is equal to the pinch off voltage V_P .
- From the figure, transfer characteristics of JFET is a part of parabola then expression for drain current is given by

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_{GS(off)}} \right]^2$$

I_D = drain current at given V_{GS}

I_{DSS} = short gate drain current

V_{GS} = gate source voltage

$V_{GS(off)}$ = gate source cutoff voltage

Parameters of JFET and relation among them.

The main parameters of JFET are:

1) Ac drain resistance (r_d)

2) Trans conductance (g_m)

3) Amplification factor

1) Ac drain resistance: It is the ratio of change in drain voltage (ΔV_{DS}) to change in drain current (ΔI_D) at constant gate source voltage V_{GS} .

Ac drain resistance

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D} \text{ at constant } \Delta V_{GS}$$

2) Trans conductance (g_m): It is the ratio of change in drain current (ΔI_D) to change in gate source voltage (ΔV_{GS}) at constant drain source voltage (ΔV_{DS}).

Trans conductance

$$g_m | g_{TS} = \frac{\Delta I_D}{\Delta V_{GS}} \text{ at constant } \Delta V_{DS}$$

3) Amplification factor (μ): It is ratio of change in drain source voltage (ΔV_{DS}) to change in gate source voltage (ΔV_{GS}) at constant drain current (ΔI_D).

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} \text{ at constant } \Delta I_D$$

Relation among JFET parameters:

We know that

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D}$$

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}$$

Multiply the numerator and denominator of μ with ΔI_D then we get,

$$\mu = \frac{\Delta V_{GS} \times \Delta I_D}{\Delta V_{DS} \times \Delta I_D}$$

$$\mu = \frac{\Delta V_{GS}}{\Delta V_{DS}} \times \frac{\Delta I_D}{\Delta I_D}$$

$$\mu = r_d \times g_m$$

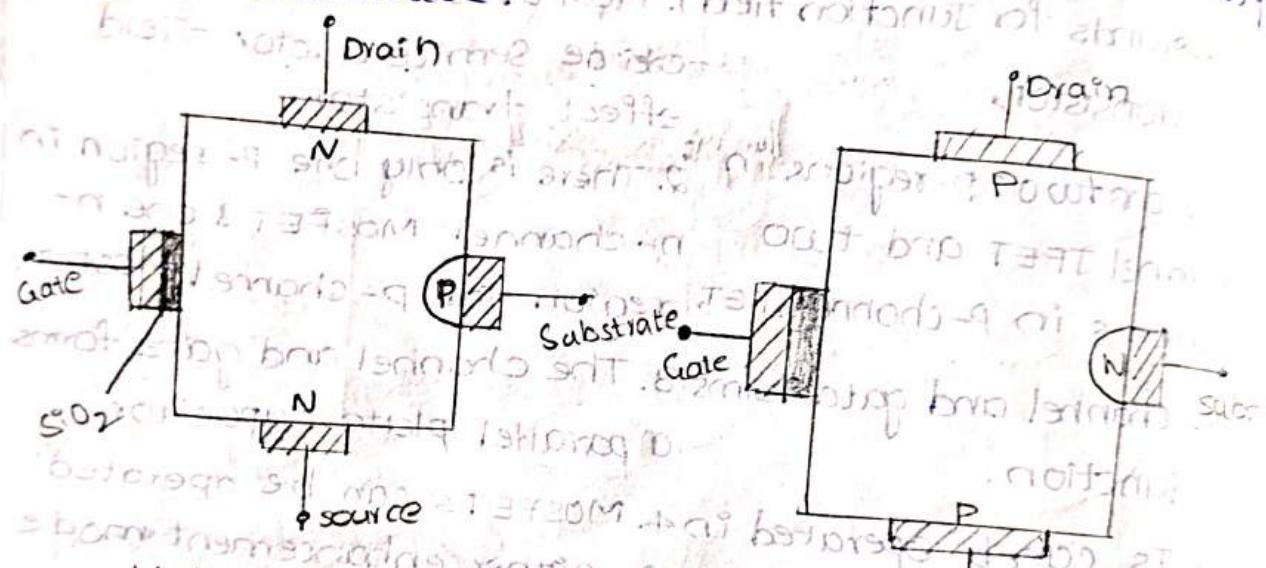
Amplification factor = Ac drain resistance \times trans conductance difference b/w JFET and MOSFET:

JFET	MOSFET
1. JFET stands for Junction field effect transistor.	1. MOSFET stands for metal oxide semiconductor field effect transistor.
2. There are two P-regions in n-channel JFET and two n-regions in P-channel JFET.	2. There is only one P-region in n-channel MOSFET & one n-region for p-channel MOSFET.
3. The channel and gate forms a pn junction.	3. The channel and gate forms a parallel plate capacitor.
4. JFETs can be operated in depletion mode.	4. MOSFETs can be operated in either enhancement mode or depletion mode.
5. In a FET, the source to drain current is controlled by the reverse bias voltage to the gate.	5. In a MOSFET the source to drain current is controlled by electric field of capacitor formed at the gate.
6. Input impedance in the range of $100\text{M}\Omega$.	6. Input impedance in the range of $10,000\text{M}\Omega$ to $10,00,000\text{M}\Omega$.
7. Manufacturing process is simple.	7. Manufacturing process is complex.

Construction and working of MOSFET :- (N-channel) & (P-channel)

Construction of MOSFET:-

- There is only single p-region in N-channel FET & single N-region in P-channel FET called as substrate.
- A thin layer of metal oxide (usually silicon dioxide) is deposited over the left side of the channel. A metal gate is deposited over the oxide layer. As silicon dioxide is an insulator, therefore gate is insulated from the channel, for this reason, MOSFET is sometimes called insulated gate FET (IGFET).
- Like JFET, a MOSFET has four terminals. Source, Drain & Substrate.



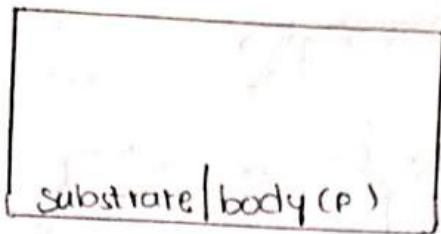
Construction and working of depletion type N-channel

construction of depletion type N-channel MOSFET:-

- In depletion type MOSFET channel is present from the beginning in between source and drain.
- Depletion type N-channel MOSFET consist of four terminals → P substrate, 2) source, 3) Gate, 4) Drain.

i)

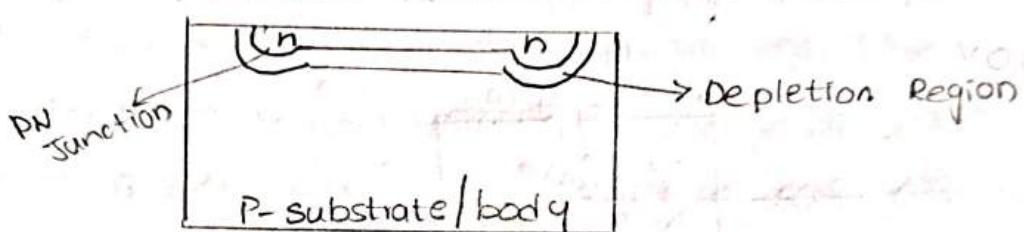
→ P-type substrate is formed by adding trivalent impurities to silicon wafer.



Formation of P-type substrate

ii)

→ Two n-type wells are induced in the p-type substrate.



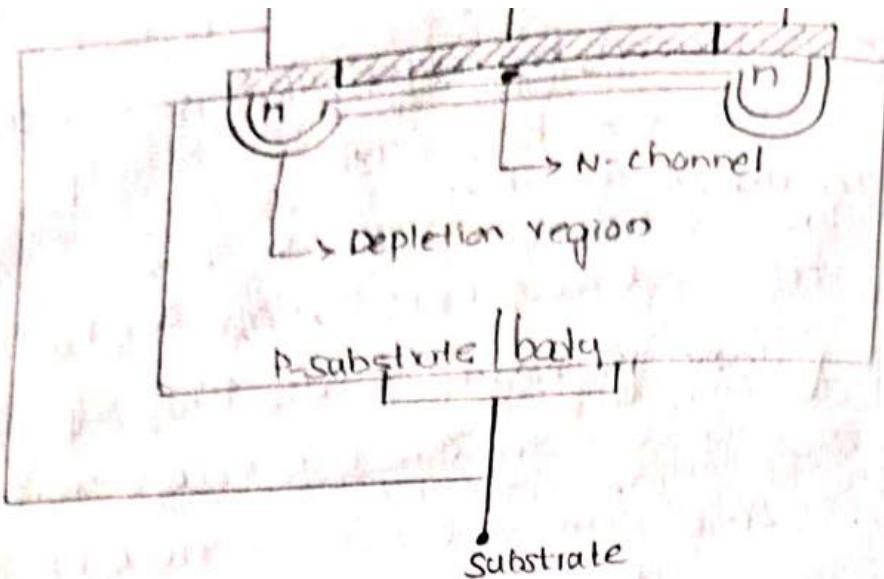
Formation of N-type wells

→ After creation of two N-type wells there is two junctions formed between two n-type materials and p-type substrate due to this two depletion region with same width will be formed.

→ One n well acts as source and other will be drain.

→ Source, drain and substrate will be taken out from the p-type substrate/body with the help of metal contact.

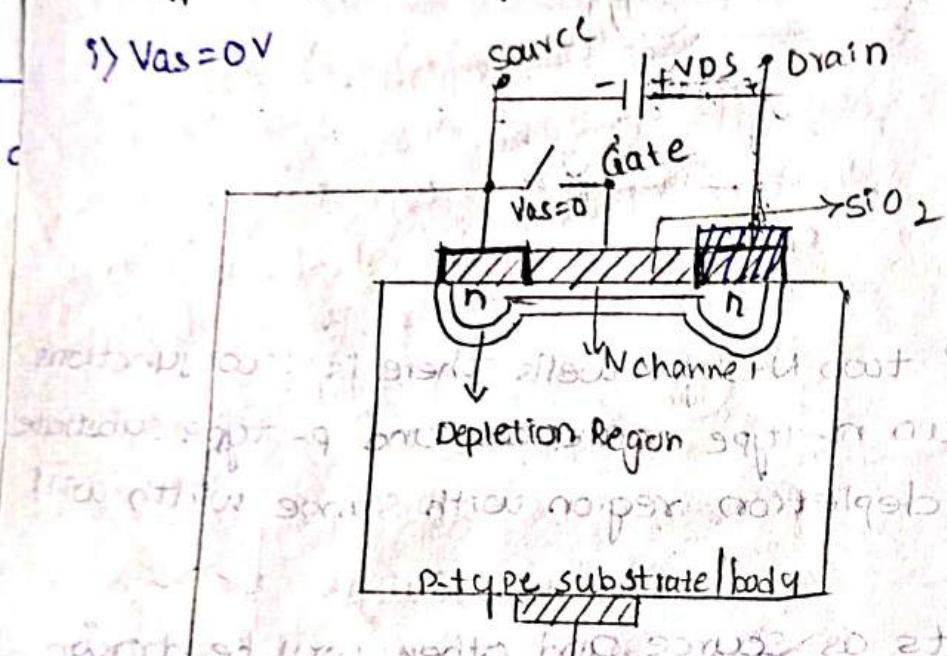
→ In MOSFET there is no direct contact in between gate terminal and channel. The gate terminal is separated from the channel by SiO_2 layer which will acts as insulator.



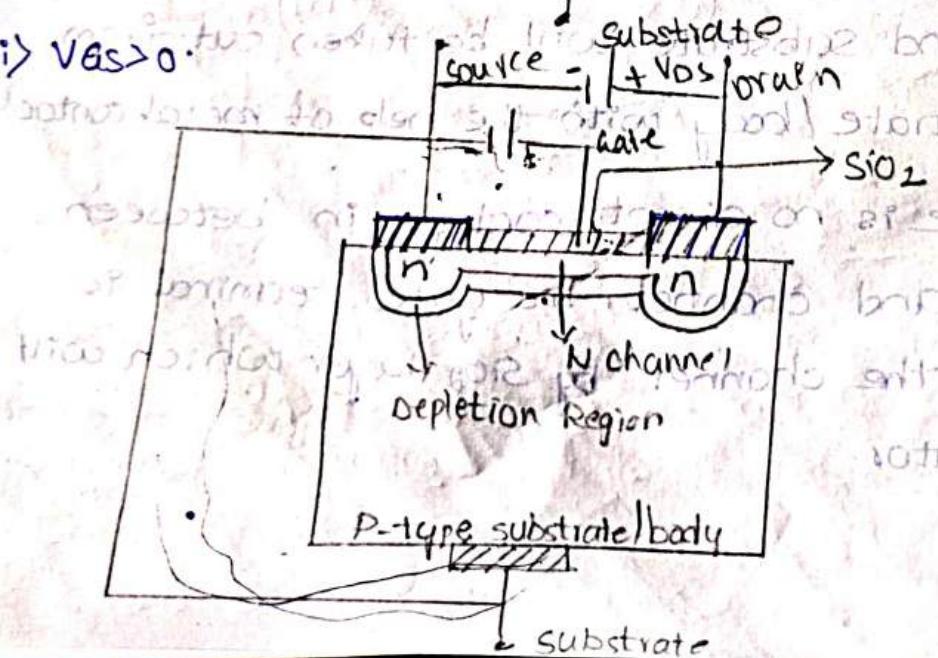
complete formation of depletion type MOSFET

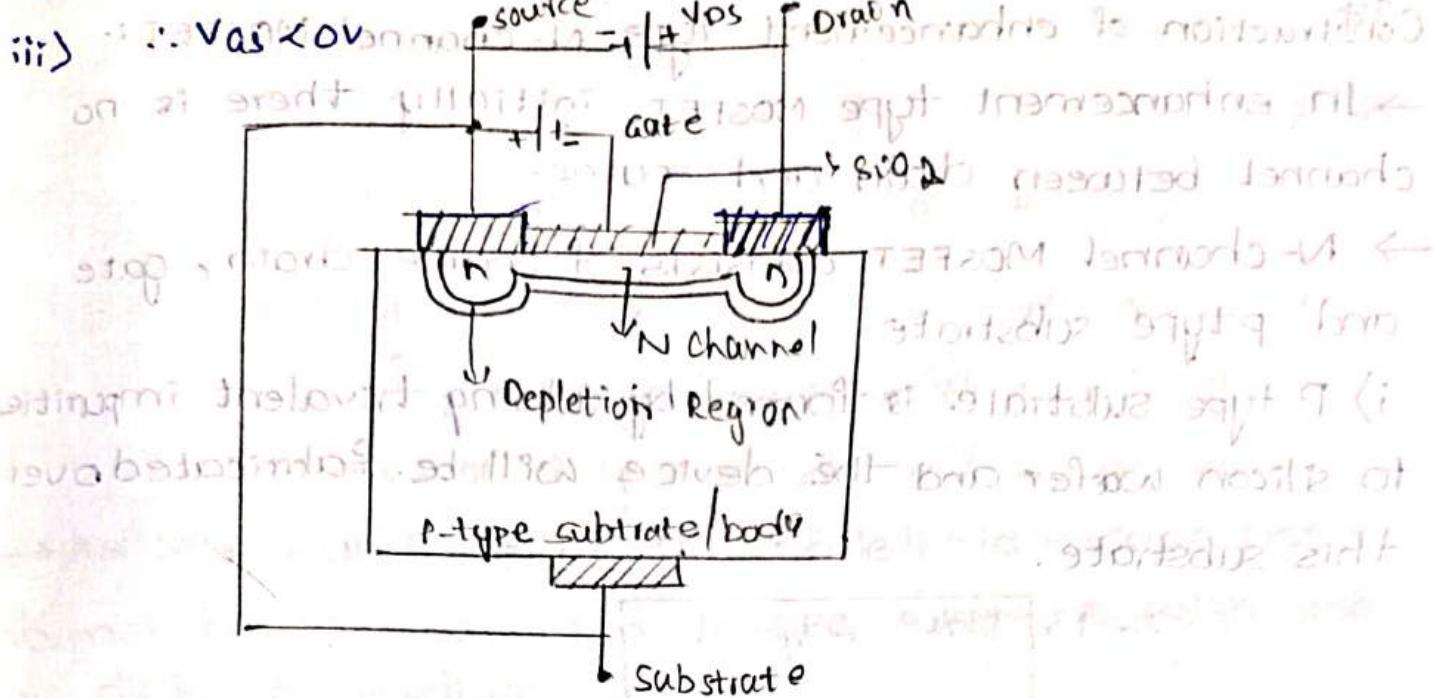
Working of depletion type N-channel MOSFET :-

i) $V_{GS} = 0V$



ii) $V_{GS} > 0$



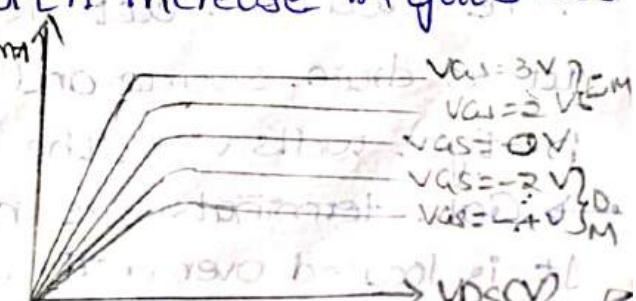


→ When $V_{AS} = 0V$ with the increase in V_{DS} the current I_D increases because drain is more positive so that more number of electrons attracts towards the drain terminal but after sometime pinchoff occurs and drain current will becomes constant even if we increase the V_{DS} .

→ When $V_{AS} > 0V$ application of positive gate voltage results induced negative polarity in the n-type channel thus the conductivity of the channel gets increased so that drain current also increases.

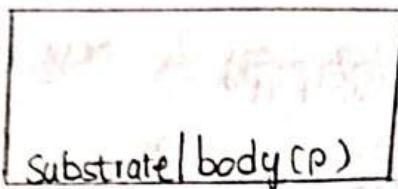
→ When $V_{AS} < 0V$.

When the gate is applied with negative voltage positive charges are induced in the n-channel and these induced positive charges makes the n-channel less conductive and the drain current decreased with increase in gate bias voltage.



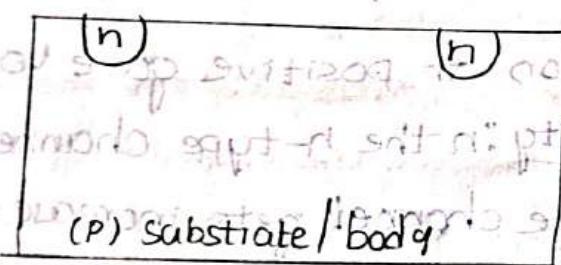
Construction of enhancement type N-channel MOSFET:

- In enhancement type MOSFET initially there is no channel between drain and source.
- N-channel MOSFET consists of source, drain, gate and p-type substrate.
- i) P-type substrate is formed by adding trivalent impurity to silicon wafer and the device will be fabricated on this substrate.

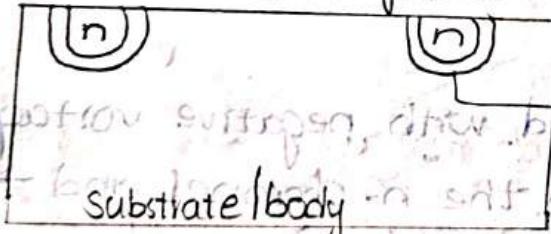


Formation of p-type substrate

- ii) After these two n-type wells are created there is junction b/w two n-type materials and p-type material and two depletion regions with same width will be formed.



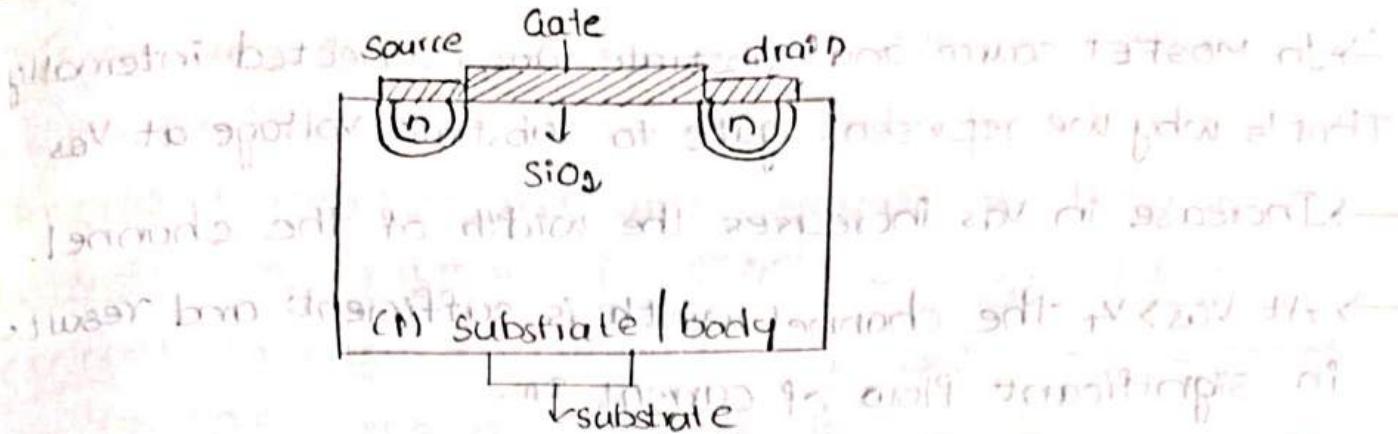
* Formation of n-type well



* Formation of depletion region

- One n well will act as source and other n well will act as drain. Source and drain will be taken out from the n-type wells with the help of metal contact.

- Gate terminals are not in direct contact with substrate. It is located over a thin layer of SiO_2 / silicon dioxide.



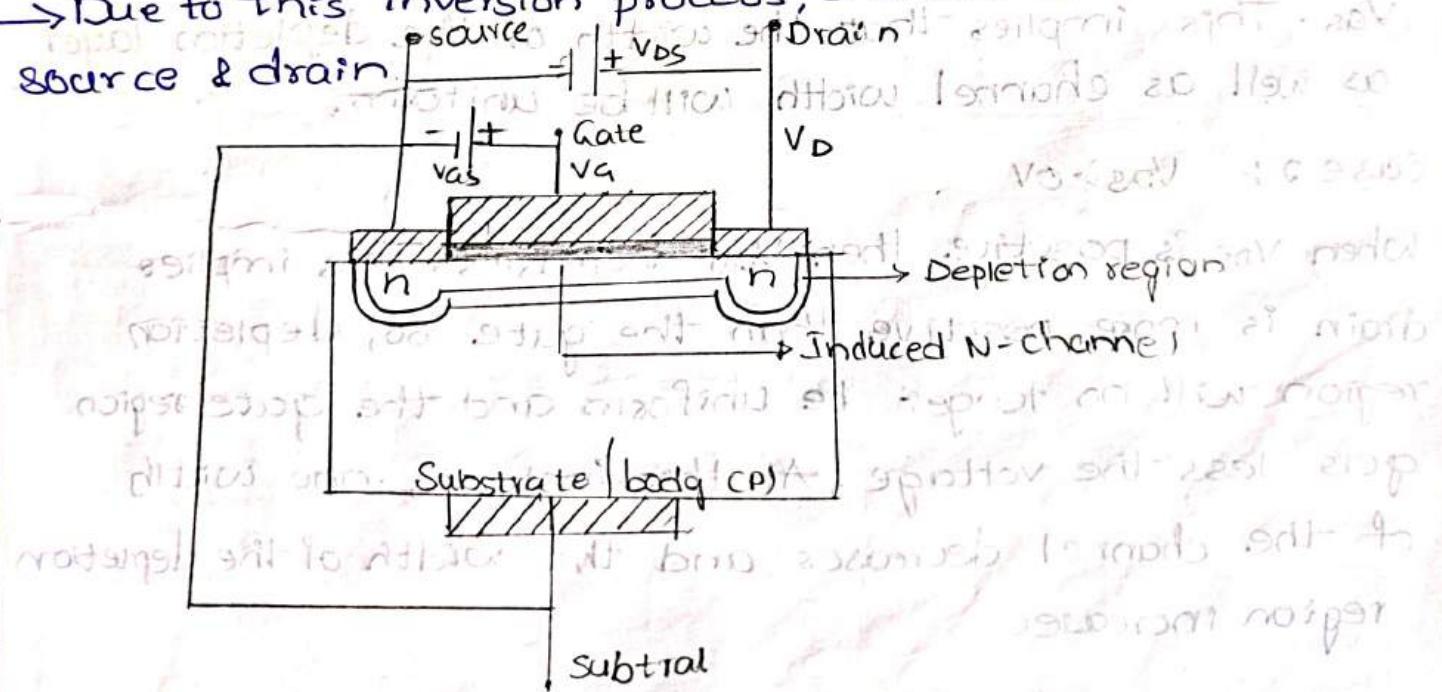
Formation of terminals

→ As SiO_2 is an insulator, a parallel plate capacitor is formed between Gate and p-type substrate with SiO_2 as dielectric medium.

→ If we apply normal V_{AS} (Substrate) between Gate and p-type substrate. Positive charge will accumulate over gate plate and less number of the charges will accumulate over substrate plate.

→ If we increase V_{AS} , more no. of +ve charges will accumulate over the substrate region & p-region near the surface will become n-region. This process is known as inversion.

→ Due to this inversion process, channel is created below



→ In MOSFET source and substrate are connected internally.
That's why we represent gate to substrate voltage at V_{GS}

→ Increase in V_{GS} increases the width of the channel

→ At $V_{GS} > V_t$ the channel width is sufficient and results in significant flow of current I_D .

→ The voltage that results in significant flow of current from source to drain is known as threshold voltage.

Applying KVL to the above circuit, we get

$$V_a - V_{GS} + V_{DS} - V_0 = 0 \quad (\text{consider potential difference between drain and source})$$

$$V_a - V_0 = V_{GS} - V_{DS} \quad (\text{between drain terminal})$$

$$V_{GD} = V_{GS} - V_{DS} \rightarrow 0 \quad (V_a - V_0 \text{ as } V_{GD})$$

Case 1 : $V_{DS} = 0V$

Sub $V_0 = 0$ in ①, we get

$$V_{GD} = V_{GS}$$

This means there is no potential difference b/w V_{GD} or V_{GS} . This implies that the width of the depletion layer as well as channel width will be uniform.

Case 2 : $V_{DS} > 0V$

When V_{DS} is positive then V_{GD} decreases. This implies drain is more positive than the gate so, depletion region will no longer be uniform and the gate region gets less the voltage. At this instant, one width of the channel decreases and the width of the depletion region increases.

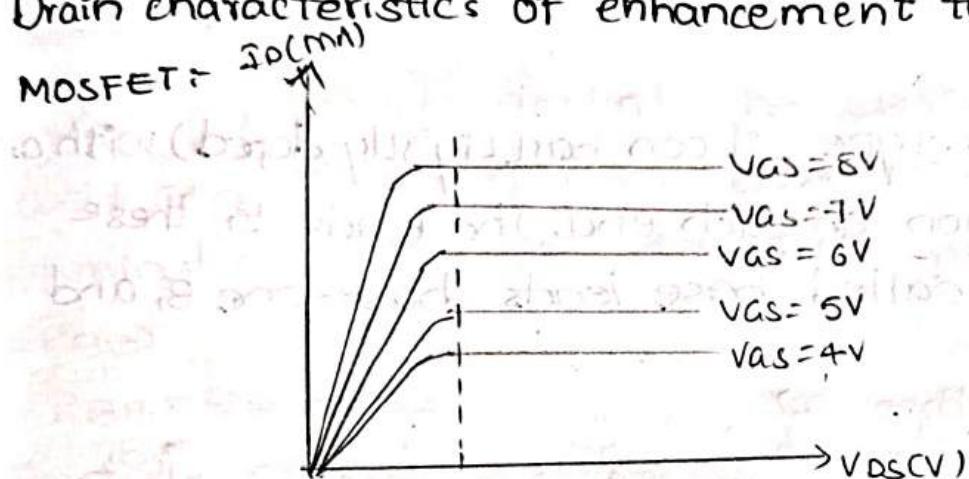
case 3: $V_{DS} = V_{GS} - V_T$

consider V_{DS} as V_T . In this case both V_{DS} & V_{GS} are in opposite direction and can't overcome V_T . The channel becomes very narrow. If we increase V_{DS} the drain current I_D becomes almost constant. This is known as V_{DS} Sat. V_{DS} Sat is equal to $V_{GS} - V_T$.

$$V_{DS \text{ Sat}} = V_{GS} - V_T$$

Drain characteristics of enhancement type N-channel

MOSFET: $I_D(MA)$



at ionization energy (begol) plasma is formed here due to ionization of electrons and nuclei in H2 at 10^-10. Ionized hydrogen anti-matter or anti-protons are produced. (3) second bottom of potential well is formed due to minimum cell potential difference. Inverse anti-matter

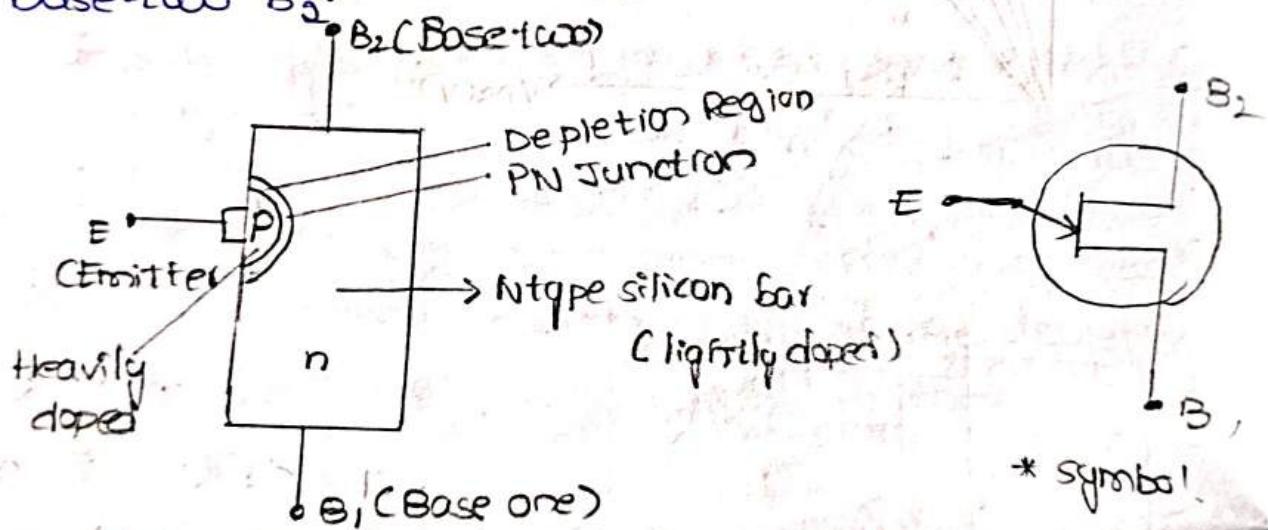
is formed due to ionization of H2 at 10^-10. The potential barrier is formed due to ionization of H2 at 10^-10.

UJT (Unijunction Transistor):-

- A Unijunction Transistor is a three terminal switching device.
- This device has a unique characteristic that when it is triggered, the emitter current increases regeneratively until it is limited by emitter power supply.
- It can be used in switching, pulse generator, saw tooth generators etc.

Construction:-

- It consists of n-type silicon bar (lightly doped) with electrical connection on each end. The leads to these connections are called base leads base-one B_1 and base-two B_2 .



- A small piece of heavily doped p-type material is alloyed to one side of n-type bar closer to B_2 for producing single PN-Junction. The terminal taken from p-type material is called Emitter (E).
- In the symbol arrow indicates the direction of the conventional current.

Equivalent circuit of OTI: After this as different parts

→ Equivalent circuit of OTI consists of a PN Junction Diode and two resistors R_{B1} and R_{B2} .

→ R_{B2} is the resistance of silicon bar between base B_2 and the emitter Junction.

→ R_{B1} is the resistance of bar between base B_1 and emitter Junction. This resistance is variable because its value depends upon the bias voltage across the PN-Junction.

i) When no voltage applied, the resistance between base 1 and base 2 of the silicon bar with emitter terminal open is called the interbase resistance (R_{BB}).

$$R_{BB} = R_{B1} + R_{B2}$$

The value of R_{BB} lies between $4k\Omega - 10k\Omega$.

ii) If a voltage V_{BB} is applied between the bases with emitter terminal open, the voltage will divide up across R_{B1} and R_{B2} .

voltage across R_{B1} , $V_1 = V_{BB} \cdot \frac{R_{B1}}{R_{B1} + R_{B2}}$

broadly among this condition

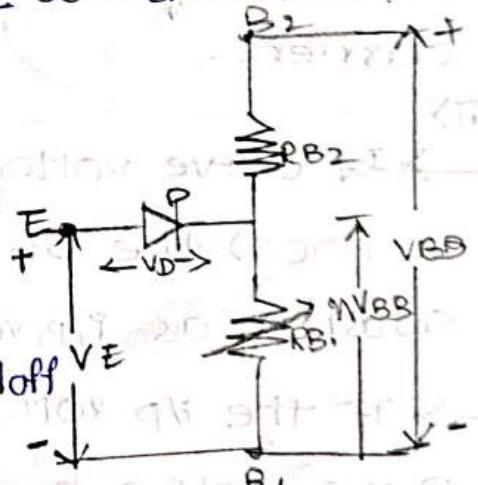
$$V_1 = \eta \cdot V_{BB}$$

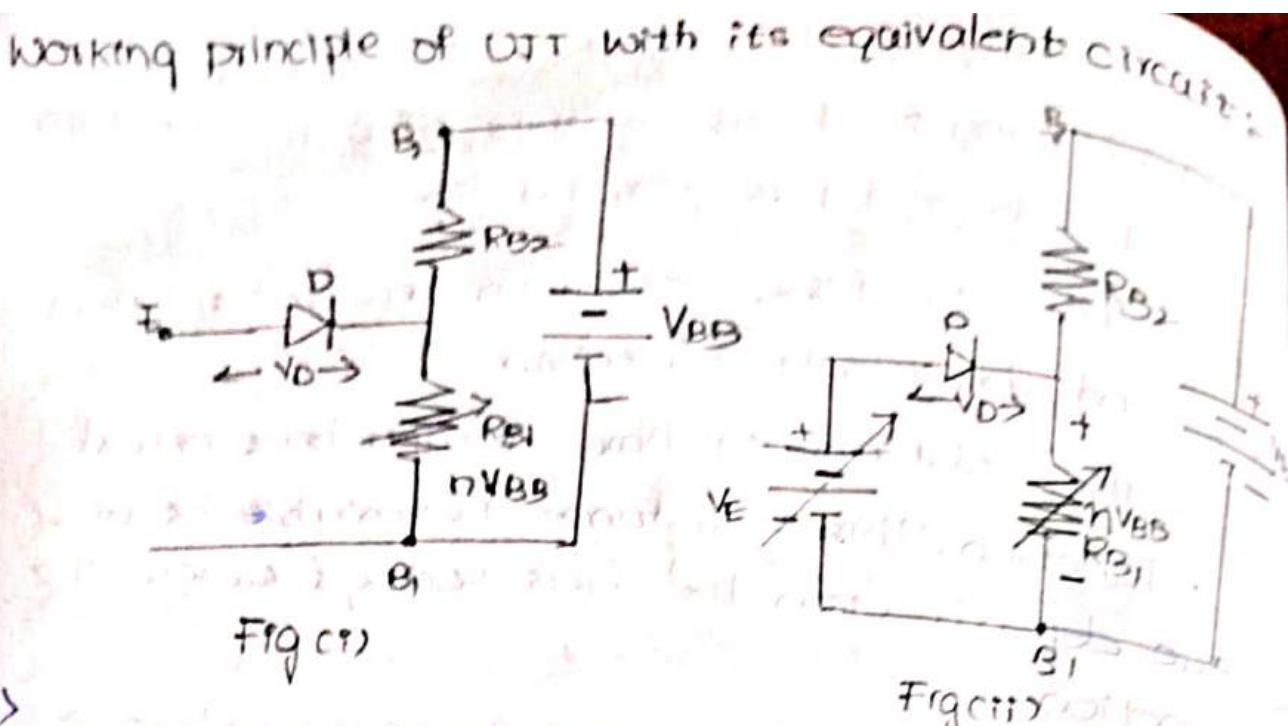
Where η is called the "intrinsic stand-off ratio".

$$\eta = \frac{R_{B1}}{R_{B1} + R_{B2}} = \frac{R_{B1}}{R_{BB}}$$

$$\eta = \frac{V_1}{V_{BB}}$$

The typical value of η ranges from 0.56 to 0.8.





- i) → When we apply V_{BB} between base 1 & base 2 with emitter open as shown in fig (i) the voltage gradient establishes along n-type bar.
- More than half of V_{BB} appears between emitter & B_2 , and the voltage ($V_1 = nV_{BB}$) between emitter & B_1 establishes a reverse bias on the P-n Junction and leakage current flows due to minority carriers.
- ii) → If a +ve voltage applied at the emitter as shown in fig (ii) the Pn junction will remain reverse biased so long as i/p voltage is less than V_1 .
- If the i/p voltage to the emitter exceeds V_1 , the P N Junction becomes forward biased. Under these conditions the holes are injected from p-type into n-type bar. These holes are repelled by +ve B_2 terminal & they are attracted towards B_1 terminal of the bar. This accumulation of holes in the

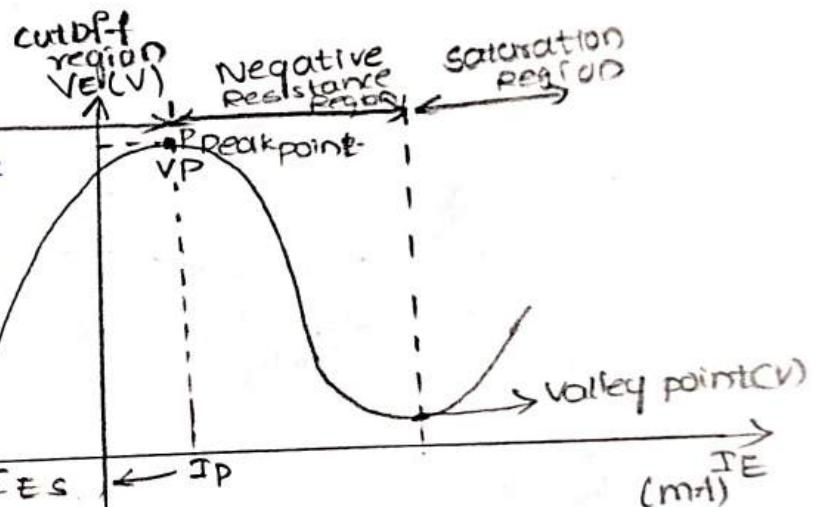
mitter to B_1 region results in the decreases of V_{BE} , in this section of bar. The internal voltage drop from mitter to B_1 is decreased and emitter current I_E increases.

> As more holes are injected, a condition of saturation will eventually be reached. At this point, the emitter current is constant. The device is then limited by emitter power supply only. The device is now in the ON state.

if a -ve pulse is applied to the emitter, the N junction is reverse biased and the emitter current is cutoff. The device is then said to be in the OFF state.

Characteristics of UJT:

→ upto the peak point P , the diode is reverse biased & hence, the region left to the peak point is called cut-off region. But a small leakage current I_{ES} flows from B_1 to emitter leakage current due to minority carriers.



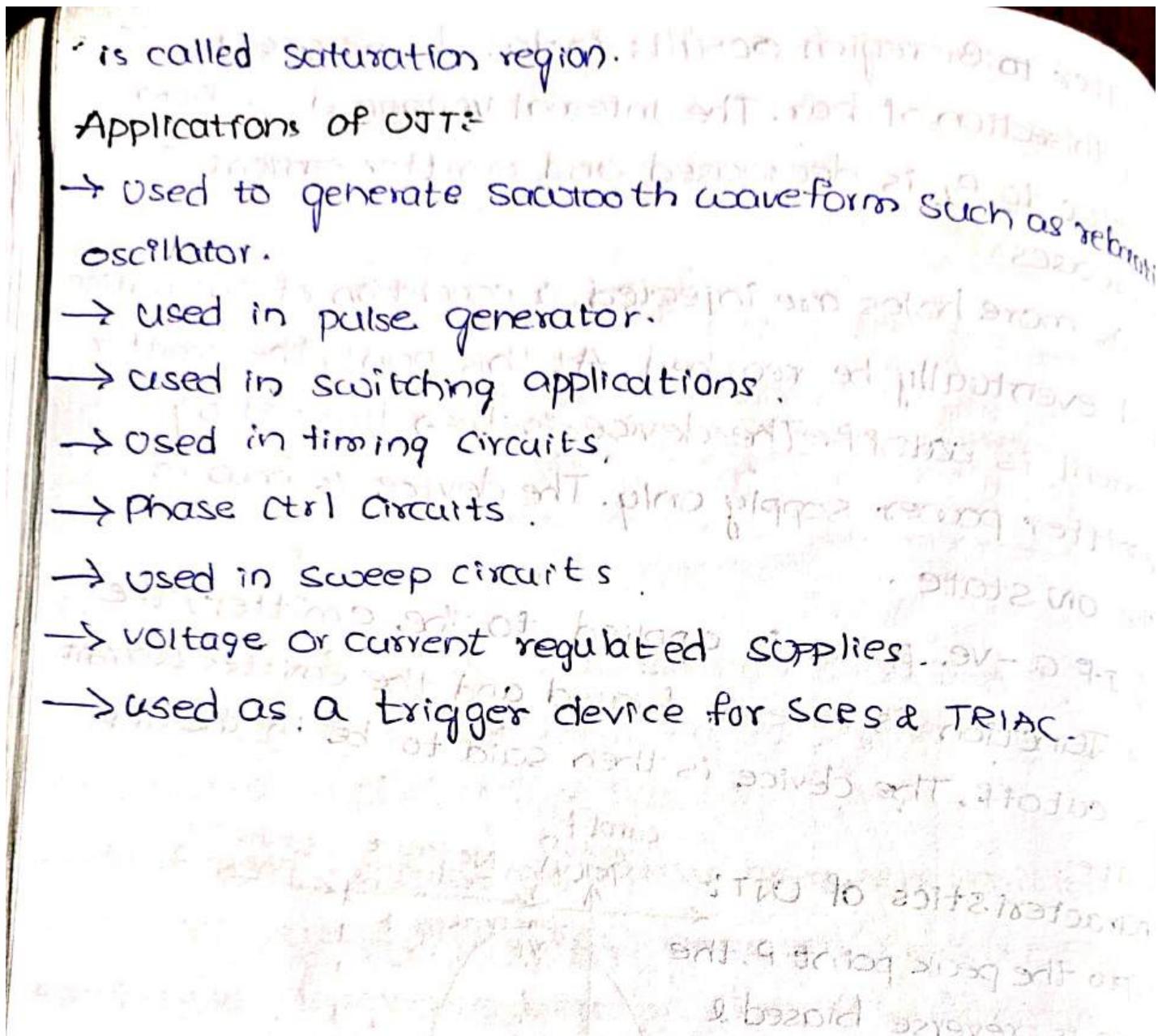
→ At the peak point P , the diode starts conducting & holes are injected into N -layer. Hence, the resistance decreases thereby decreasing V_E . For the increase I_E , so, there is a "negative resistance region" from peak point P to valley point (V) .

→ After the valley the device is driven into saturation & behaves like a conventional forward biased PN Junction diode. The region to the right of valley point

is called saturation region.

Applications of UJT:

- Used to generate smooth waveform such as oscillator.
- used in pulse generator.
- used in switching applications.
- used in timing circuits.
- Phase Ctrl Circuits.
- used in sweep circuits.
- voltage or current regulated supplies.
- used as a trigger device for SCRs & TRIAC.



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