BIPOLAR JUNCTION TRANSISTOR

Introduction:-

→ The transistor was developed by Dr. shockley along with Bell Laboratories team in 1951.

→ The transistor is a main building block of all modern electronic systems.

→ It is a three terminal device whose output current, voltage and power are controlled by its input current.

→ In communication systems it is the primary component in the amplifier.

→ An amplifier is a circuit that is used to increase the stength of an ac signal.

→ Basically there are two types of transistors

- Bipolar junction transistor.
- Field effect transistor.

→ the important property of the transistor is that it can raise the strength of a weak signal. This property is called amplification.

→ A transistor consists of two P-N junctions. The junction are formed by sandwitching either P-type or N-type semiconductor layers between a pair of opposite types which is shown beloco.

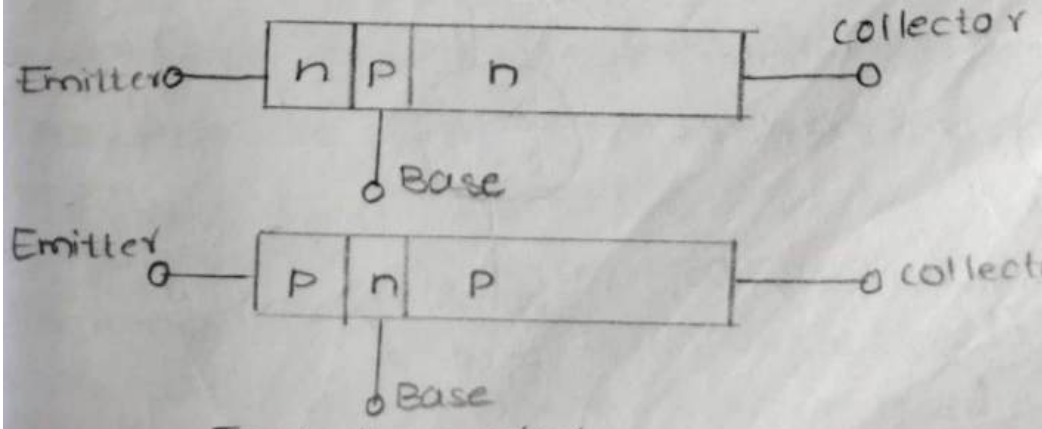


Fig: transistor

Transistor Construction:-

→ A transistor has three regions known as emitter, base and collector.

Emitter:- It is a region situated in one side of a transistor which supplies charge carriers (i.e electrons and holes) to the other two regions.

→ Emitter is heavily doped region.

Base:- It is the middle region that forms two P-N junction in the transistor.

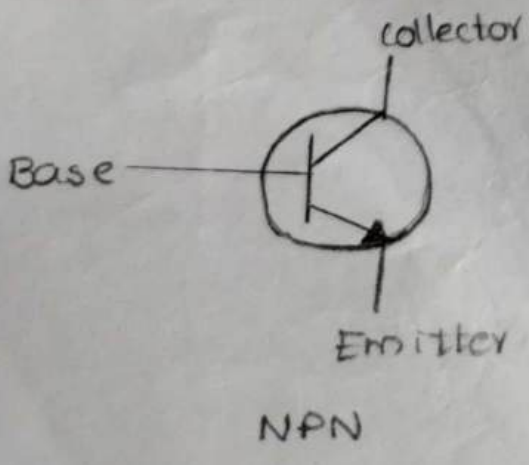
→ The base of the transistor is thin as compared to the emitter and is a lightly doped region.

Collector:- It is a region situated in the other side of a transistor (i.e opposite to the emitter) which collects the charge carriers.

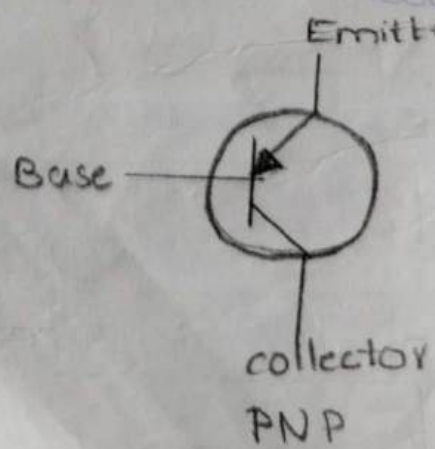
→ The collector of the transistor is always larger than the emitter and base of a transistor.

→ The doping level of the collector is intermediate between the heavy doping of emitter and the light doping of the base.

Transistor Symbols:-



NPN

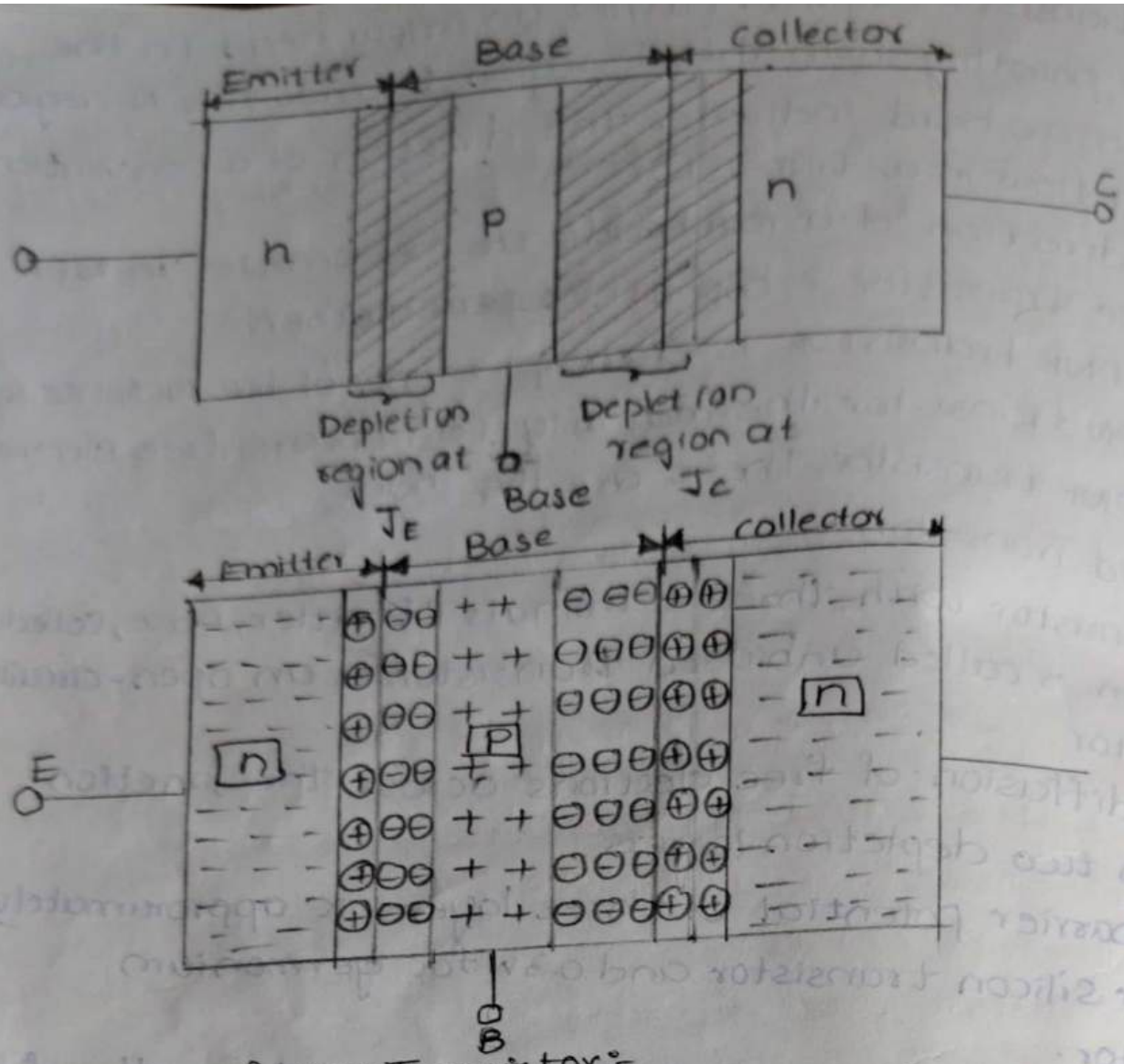


PNP

→ The transistor symbol carries an arrow head in the emitter pointing from the P-region towards the N-region.
→ The arrow head indicates the direction of a conventional current flow in a transistor.
→ The direction of arrow heads at the emitter in NPN and PNP transistor is opposite to each other.
→ The PNP transistor is a complement of the NPN transistor.
→ In NPN transistor the majority carriers are free electrons, while PNP transistor these are the holes.

Unbiased Transistors:-

→ A transistor with three terminals (Emitter, Base, Collector) left open is called unbiased transistor or an open-circuited transistor.
→ The diffusion of free electrons across the junction produces two depletion layers.
→ The barrier potential of three layers is approximately 0.7v for silicon transistor and 0.3v for germanium transistor.
→ Since the regions have different doping levels therefore the layers do not have the same width.
→ The emitter base depletion layer penetrates slightly into the emitter as it is a heavily doped region where as it penetrates deeply into the base as it is a lightly doped region.
→ Similarly the collector-base depletion layer penetrates more into the base region and less into the collector region.
→ The emitter-base depletion layer width is smaller than that of collector base depletion layer.
→ The unbiased transistor is never used in actual practice. Because of this we went for transistor biasing.



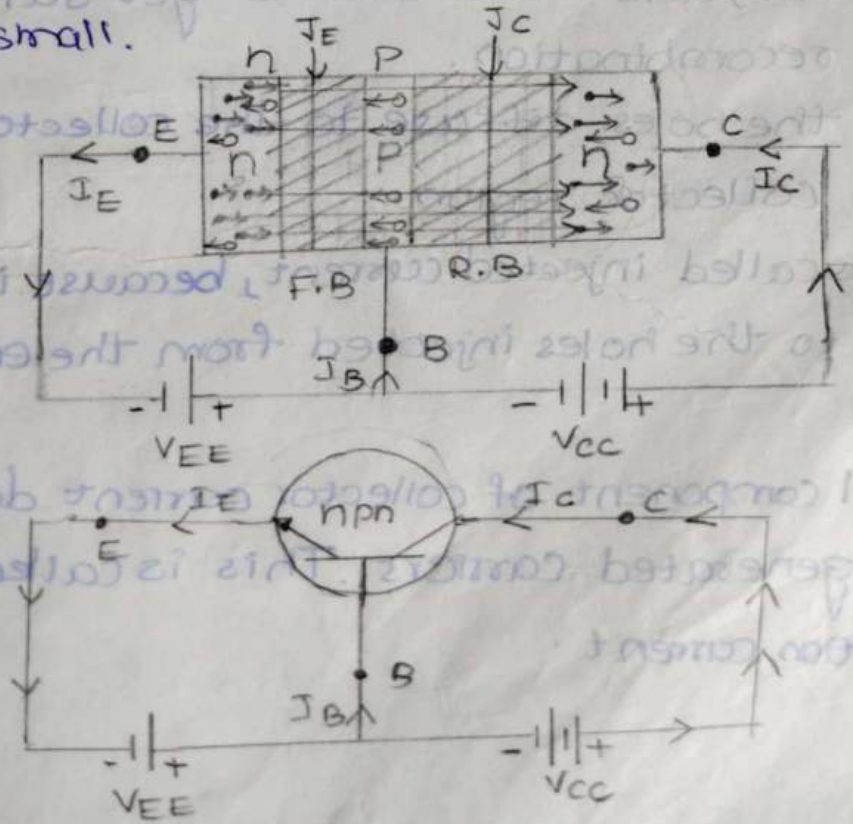
Operation of NPN Transistor:-

→ The NPN transistor is biased in forward active mode i.e, emitter-base of transistor is forward biased and collector base junction is reverse biased.

→ The emitter-base junction is forward biased only if V is greater than barrier potential which is 0.7 V for Silicon and 0.3V for germanium transistor.

→ The forward bias on the emitter-base junction causes the free electrons in the N-type emitter to flow towards the base region. This constitues the emitter current. Direction of conventional current is opposite to the flow of electrons.

> Electrons after reaching the base region tend to combine with the holes.
> If these free electrons combine with holes in the base, they constitue base current.
> Most of the free electrons do not combine with the holes in the base.
> This is because of the fact that the base and the width is made extremely small and electrons do not get sufficient holes for recombination.
> Thus most of the electrons will diffuse to the collector region and constitutes collector current. This collector current is also called injected current, because of this current is produced due to electrons injected from the emitter region.
> There is another component of collector current due to the thermal generated carriers.
> This is called reverse saturation current and is quite small.



Operation of PNP Transistor:-

→ operation of a PNP transistor is similar to npn transistor.

→ The current within the PNP transistor is due to the movement of holes where as in an NPN transistor it is due to the movement of free electrons

→ In PNP transistor, its emitter-base junction is forward biased and collector base junction is reverse biased.

→ The forward bias on the emitter-base junction causes the holes in the emitter region to flow towards the base region. This constitues the emitter current.

→ The holes after reaching the base region, combine with the electrons in the base and constitue base current.

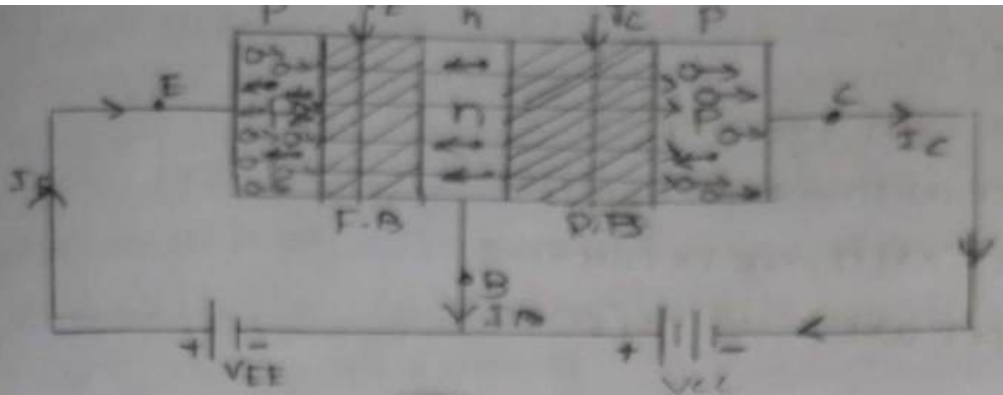
→ Most of the holes do not combine with the electron in the base region.

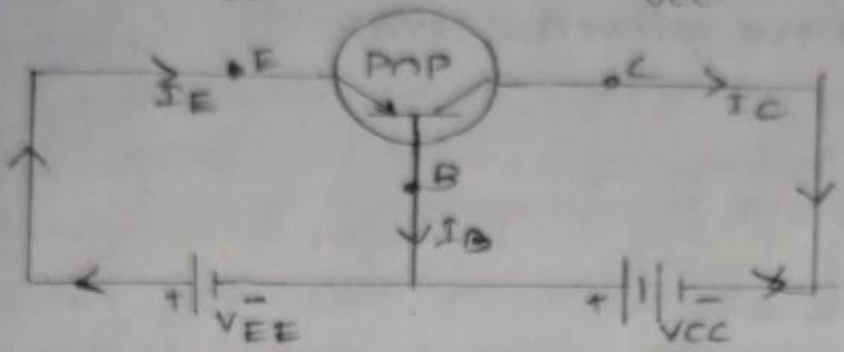
→ This is due to the fact that base width is made extremely small, and holes does not get sufficient electrons for recombination.

→ Thus most of the holes diffuse to the collector regi and constitues collector region.

→ This current is called injected current, because it is produced due to the holes injected from the emitter region.

→ There is small component of collector current due to the thermally generated carriers. This is called reverse Saturation current.





Transistor Currents:-

→ We know that direction of conventional current is always opposite to the electron current in any electronic device

→ However, the direction of a conventional current is same as that of a hole current in a PNP transistor

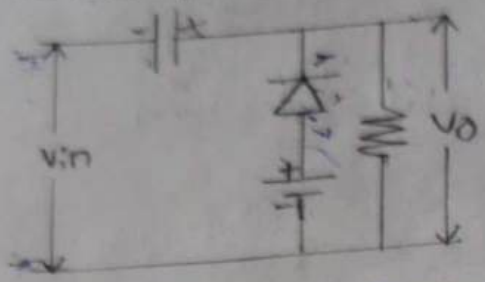
- Emitter current
- Base current
- Collector current

→ Since the base current is very small.

Biased clampers:-

1. +ve clamper with +ve reference
2. +ve clamper with -ve reference
3. -ve clamper with +ve reference
4. -ve clamper with -ve refence.

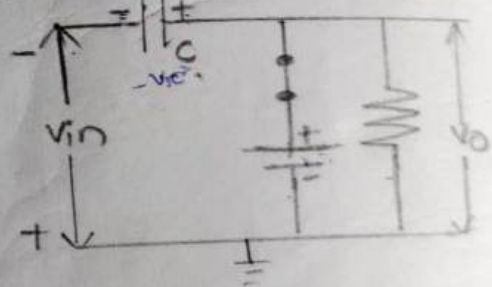
① +ve clamper with +ve reference (+Vr):-



Negative half cycle:- During the negative half cycle of input signal, terminal A becomes negative and terminal B becomes positive. In this case, both input and battery voltages make the diode forward biased.

→ When the diode is in the forward biased condition, the diode will act as closed switch, then the capacitor starts charging and its value is equal to the sum of the input voltage and the bias voltage.

→ This means that the voltage across the capacitor is -Vm+Vr. Moreover in this case, no signal appears at the output, as shown in fig.



Applying KVL

$V_{in} = V_c + V_r$

$V_c = V_{in} - V_r$

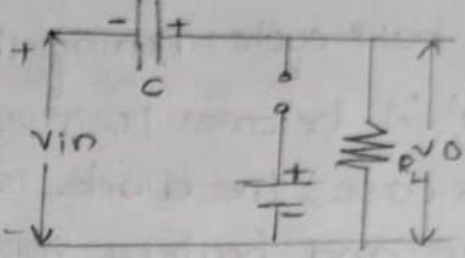
$\boxed{V_c = -V_m - V_r}$

Positive half cycle:- During the positive half cycle of the input signal, terminal 'A' becomes positive and terminal 'B' becomes negative. In this case, the input signal makes the diode reverse biased.

→ At the same time, the battery provides forward bias to the diode.

→ During +ve half cycle, if $V_m < V_r$, then the diode will act as closed switch because of the forward biased condition of the diode. In this condition, the diode will not allow the input signal to appear across the output. Because of the closed switch action and forward bias condition, the capacitor starts charging.

→ when $V_{in} > V_r$ the the diode becomes reverse biased, and it will act as an open switch. For this case, the input signal will appear across the output along with the charge present on the capacitor. So, we will get an additional DC shift in the input signal.



Apply KVL:

$V_{in} = V_C + V_O$

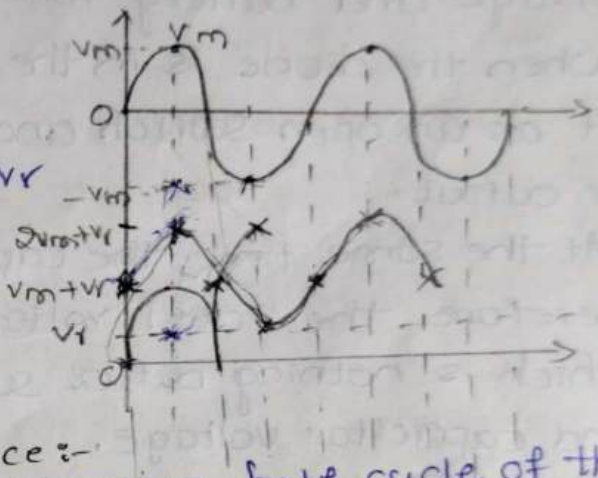
$V_{in} = -V_m - V_r + V_O$

$\boxed{V_O = V_{in} + V_m + V_r}$

case1: If $V_{in} = 0$, $V_O = V_m + V_r$

case2: If $V_{in} = V_m$ then $V_O = 2V_m + V_r$

case3: If $V_{in} = -V_m$ then $V_O = V_r$

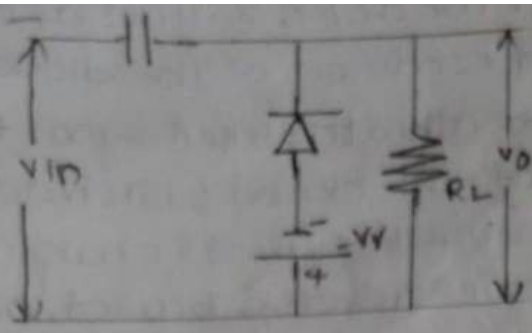


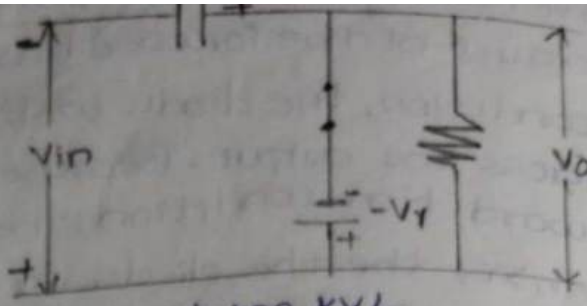
② +ve clamper with −ve reference:-

Negative halfcycle: During the negative half cycle of the input signal, terminal A becomes negative and terminal B becomes positive. In this case, the diode is forward biased by the input signal and reverse biased by the battery voltage.

→ when the diode is in forward biased condition, the diode will act as a closed switch, then the capacitor starts charging, and its value is equal to difference b/w the peak input voltage and the bias voltage. this means that the voltage across the capacitor is '$-V_m + V_r$'.

→ Moreover, in this case, no signal appears at the output as shown in fig





By applying KVL

During -ve half cycle $V_{in} = V_C + V_\gamma$

$V_C = V_{in} + V_\gamma$

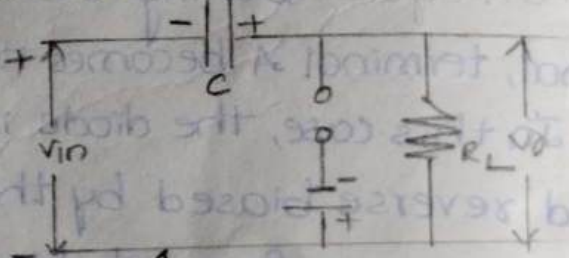
$V_c = -V_m + V_\gamma$

Positive half cycle: During the +ve half cycle of the input signal terminal "A" becomes positive and terminal "B" becomes negative. For this case, the diode is reverse biased by both the input voltage and battery voltage.

→ When the diode is in the reverse biased condition, it will act as an open switch and allow the input to appear across the output.

→ At the same time, the capacitor starts discharging, therefore the total voltage appears across the output, which is nothing but a summation of the input voltage and capacitor voltage.

→ Thus, the total voltage V_o becomes the sum of the input and capacitive voltages.



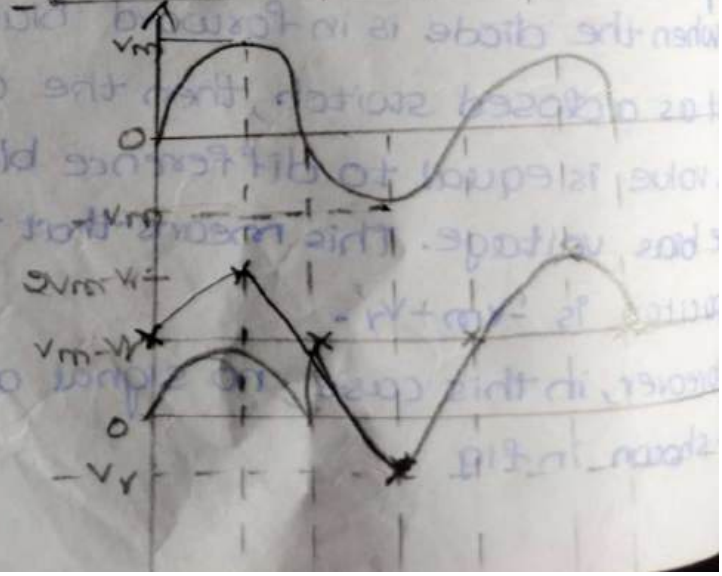
By applying KVL

During +ve half cycle

$V_{in} = V_C + V_o$

$V_{in} = -V_m + V_\gamma + V_o$

$\boxed{V_o = V_{in} + V_m - V_\gamma}$



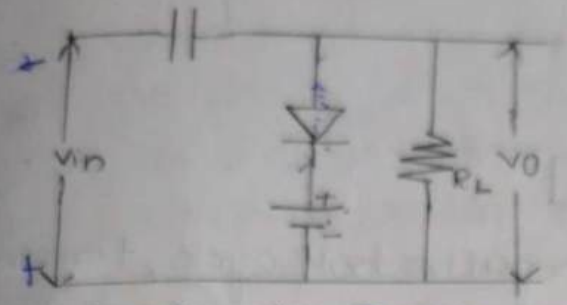
Case (i):

$V_{in} = 0, \quad V_o = V_m - V_\gamma$

$V_{in} = V_m, \quad V_o = 2V_m - V_\gamma$

$V_{in} = -V_m$, $V_o = -V_r$

③ ve clamper with reference (+Vr):



positive halfcycle:- During positive halfcycle of the input signal, terminal "A" becomes positive and terminal "B" becomes negative. For this case, the input signal makes the diode as forward biased. At the same time, the battery provides reverse bias to the diode.

→ Because of the reverse biased condition of the diode, if $V_{in} < V_r$ during the +ve half cycle, the diode will act as an open switch.

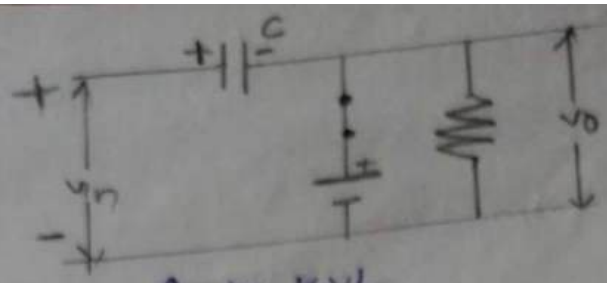
→ For this condition, the diode will not allow the input signal to appear across the output because the diode is connected in parallel.

→ Because of the open switch action and reverse bias condition, the capacitor will not charge.

→ When $V_{in} > V_r$, the diode becomes forward biased, acting as a closed switch and preventing the input signal from appearing across the output.

→ During this condition, the capacitor starts charging and charges up to the peak value of the input signal. For this case, the voltage across the capacitor will be equivalent to difference b/w V_m and V_r.

→ This means that the voltage across the capacitor is equivalent to "$V_m - V_r$".



Apply KVL

$V_{in} = V_C + V_r$

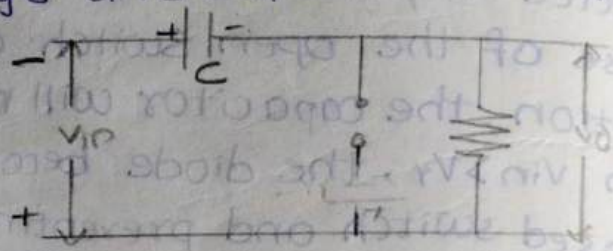
$V_C = V_{in} - V_r$

$\boxed{V_o = V_m - V_r}$

Negative half cycle: During the negative half cycle, terminal A becomes negative and terminal B becomes positive. For this case, the diode will be reverse biased by both the input signal and bias voltage.

→ When the diode is in the reverse biased condition, it will act as an open switch, and the capacitor will start discharging.

→ As a result, whatever the voltage is across the capacitor, it will appear across the output. Moreover, the total voltage across the output is equivalent to the summation of input voltage and capacitor voltage.

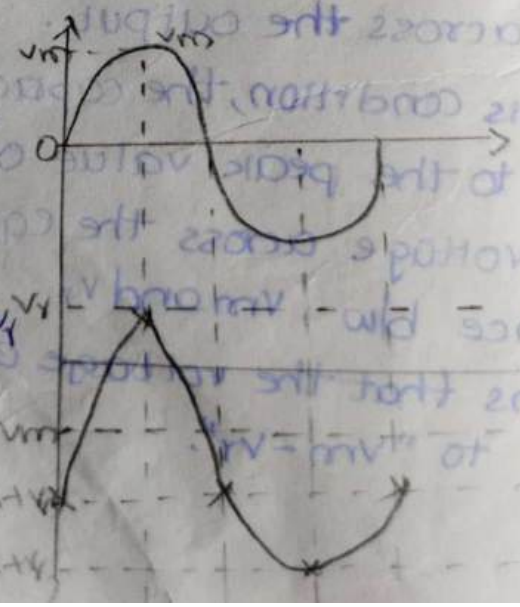


Apply KVL:

$V_{in} = V_C + V_o$

$V_{in} = V_m - V_r + V_o$

$\boxed{V_o = V_{in} - V_m + V_r}$



case i: $V_{in} = 0$ $V_o = -V_m + V_r$

case ii: $V_{in} = V_m$ $V_o = V_r$

case iii: $V_{in} = -V_m$ $V_o = -2V_m + V_r$

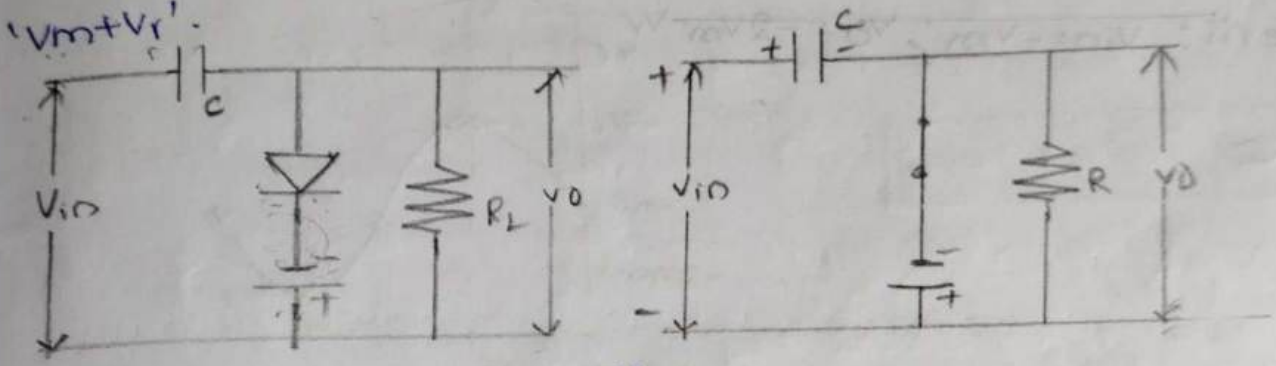
(4) -ve clamper with $-V_r$:-

positive half cycle:- During +ve half cycle of the input signal, terminal A becomes positive and terminal B becomes negative.

→ In this case, both the input signal and the bias voltage will forward bias the diode.

→ When the diode is in the forward biased condition, it will act as a closed switch, and the capacitor starts charging with its value equal to the sum of the input voltage and the bias voltage.

→ This means that, the voltage across the capacitor is 'V_m+V_r'.



Applying KVL $V_{in} = V_c - V_r$

$V_c = V_{in} + V_r$

$\boxed{V_c = V_m + V_r}$ [$\because V_{in} = V_m$]

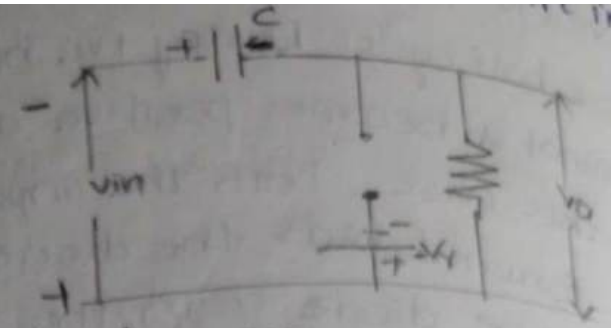
Negative half cycle:- During the negative half cycle of the input signal, terminal "A" becomes -ve and "B" becomes +ve. For this case, the input signal makes the diode as reverse biased.

→ At the same time, the battery provides forward bias to the diode. During -ve half cycle, if $V_{in} < V_r$, the diode will act as closed switch because of the forward biased condition of the diode.

→ For this condition, the diode will not allow the input signal to appear across the output. Because of the closed switch action and forward bias condition, the capacitor starts charging.

→ When $V_{in} > V_r$, then the diode becomes reverse biased, and it will act as an open switch. For this case, the input signal will appear across the output along with the charge present

on the capacitor. So,
the input signal.



By applying KVL:

$V_{in} = V_C + V_O$

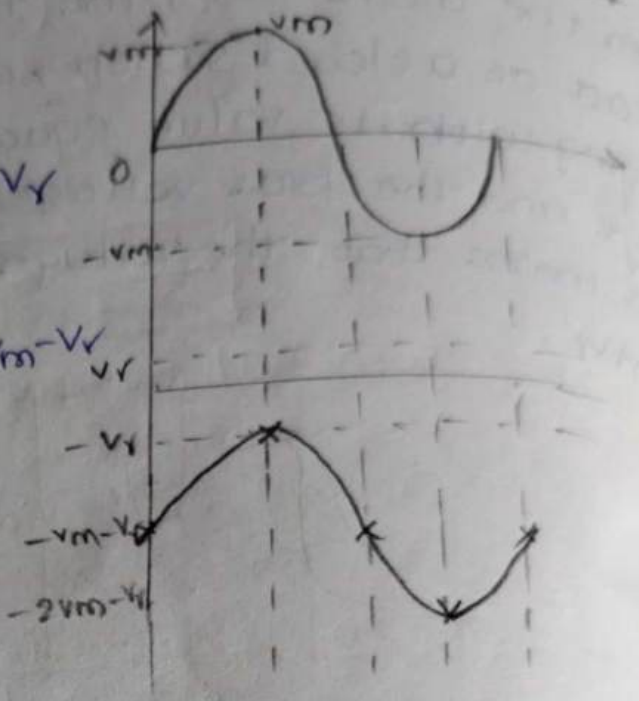
$V_{in} = V_m + V_\gamma + V_O$

$\boxed{V_O = V_{in} - V_m - V_\gamma}$

case i: $v_{in} = 0$; $V_O = -V_m - V_\gamma$

case ii: $v_{in} = V_m$; $V_O = -V_\gamma$

case iii: $V_{in} = -V_m$; $V_O = -2V_m - V_\gamma$



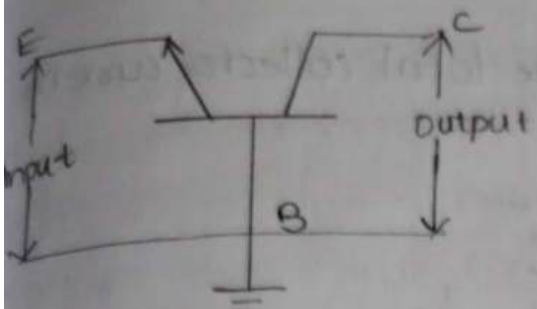
Transistor configurations:

→ Transistor is a three-terminal device, but we require four terminals two for the input and two for the output for connecting it in a circuit.

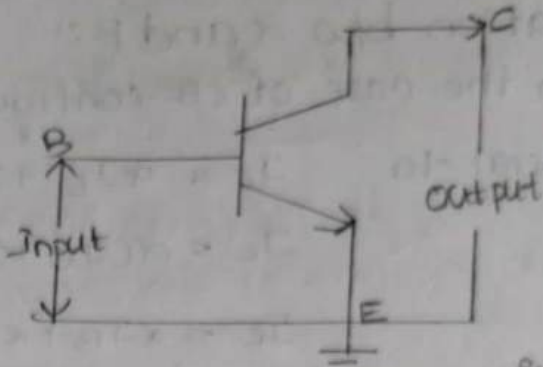
→ Hence, one of the terminals of the transistor is made common to the input and output circuits. Thus there are three types of configurations for operation of a transistor.

→ The three transistor configurations are

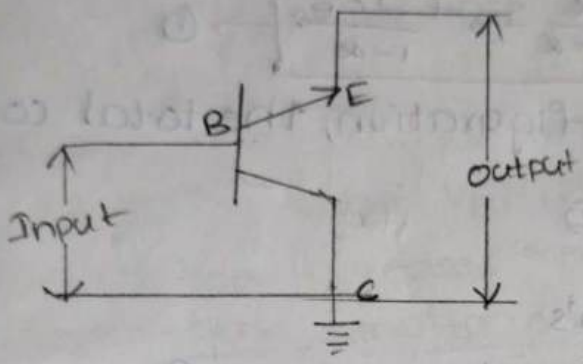
1) common base configuration
2) common emitter configuration
3) common collector configuration



common base configuration

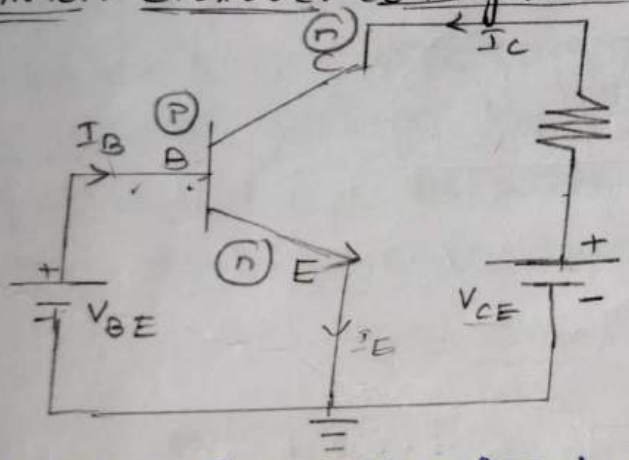


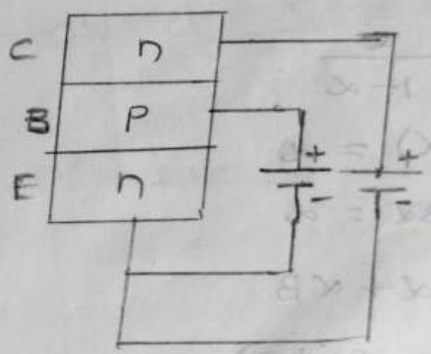
common emitter configuration



common collector configuration

Common Emitter configuration:-





B C E
I_B V_{BE} V_{EC}

⇒ In CE configuration input is connected between base and emitter and output is taken across collector and emitter. In this configuration the base current I_B flows in the input circuit and the collector current I_C flows in the output circuit.

Current amplification factor(β):-

It is defined as the ratio of change in output current to the change in input current.

$$\beta = \frac{\text{change in output current}}{\text{change in input current}}$$

$$\beta = \frac{\Delta I_C}{\Delta I_B}$$

→ Relation b/w α and β :-

As in the case of CB configuration, the total collector current I_C equal to

$$I_C = \alpha I_E + I_{CBO}$$

$$I_C = \alpha(I_B + I_C) + I_{CBO}$$

$$I_C = \alpha I_B + \alpha I_C + I_{CBO}$$

$$I_C(1-\alpha) = \alpha I_B + I_{CBO}$$

$$\boxed{I_C = \frac{\alpha}{1-\alpha} I_B + \frac{I_{CBO}}{1-\alpha}} \rightarrow (1)$$

As in the case of CE configuration, the total collector cur

$$\boxed{I_C = \beta I_B + I_{CEO}} \rightarrow (2)$$

comparing (1) and (2) eqn's

$$\beta = \frac{\alpha}{1-\alpha}, \quad I_{CEO} = \frac{1}{1-\alpha} I_{CBO} \rightarrow (3)$$

$$\beta = \frac{\alpha}{1-\alpha}$$

$$\beta(1-\alpha) = \alpha$$

$$\beta - \beta\alpha = \alpha$$

$$\beta = \alpha + \alpha\beta$$

$$\beta = \alpha(1+\beta)$$

$$\boxed{\alpha = \frac{\beta}{1+\beta}} \rightarrow (4)$$

Substitue (4) in eqn (3)

$$I_{CEO} = \frac{1}{1 - \frac{\beta}{1+\beta}} \cdot I_{CBO}$$

$$= \frac{1+\beta}{1+\beta-\beta} I_{CBO}$$

$$\boxed{I_{CEO} = (1+\beta) I_{CBO}} \rightarrow (5)$$

substitue eqn ⑤ in ③

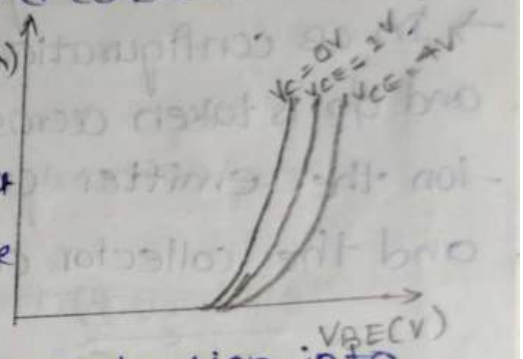
$$I_{CE} = \beta I_B + (1+\beta) I_{CB_0}$$

I/p and o/p characteristics of CE configaration :-

Input characteristics :-

→ The curve drawn between base current I_B and emitter-base voltage V_{BE} for a constant voltage V_{CE} is known as Input characteristics.

→ For a given value of V_{CE} the emitter-base junction is forward biased and acts like P-N junction and conducts current after knee voltage (cut-in voltage)



→ With the increase in V_{CE} causes the i/p current I_B to be lower V_{BE}, because high value of V_{CE} increases reverse bias for collector-base junction and causes greater depletion region and penetration into base which causes the reduction of base space.

→ Inorder to get base current, we have to provide highest base emitter voltage V_{BE}.

→ Input resistance (Ri) :- The ratio of change in inpult voltage ΔV_{BE} to change in input current ΔI_B.

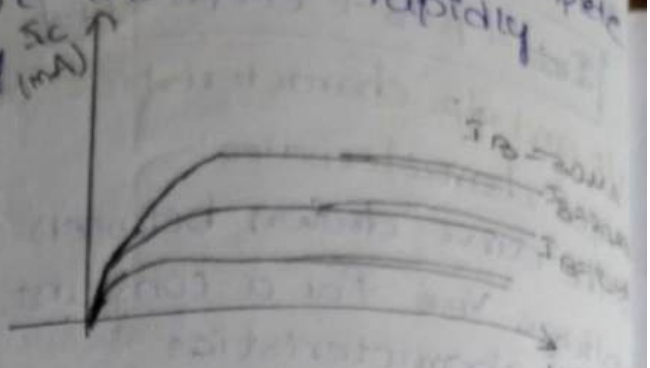
$$R_I = \frac{\Delta V_{BE}}{\Delta I_B}$$

output characteristics :-

→ The curve drawn b/w output voltage V_{CE} and output current I_C at constant input current I_B is known as output characteristics.

→ With the low values of I_B that is 0uA only leak current flows thraugh the collector region. with the low values of V_{CE} base current I_B doesnot cause a corresponding change in collector current I_C.

→ with much values of V_{CE} breakdown and collector current increases rapidly

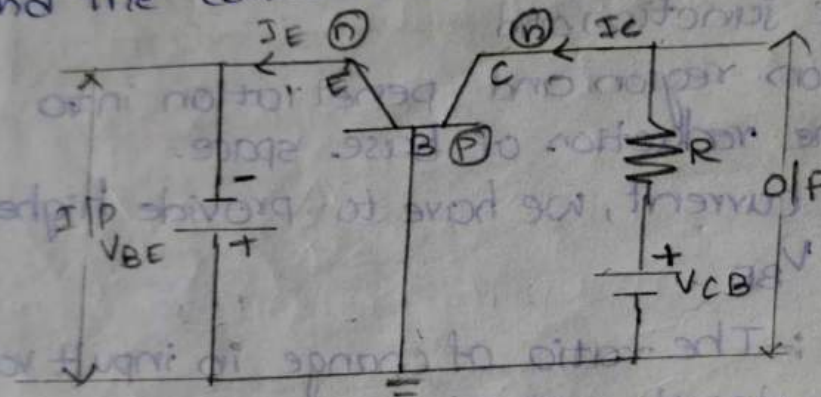


Output resistance (r_o): The ratio of change in o/p voltage ΔV_{CE} to change in o/p current ΔI_C.

$$r_o = \frac{\Delta V_{CE}}{\Delta I_C}$$

Common-base configuration:-

→ In CB configuration i/p is connected b/w emitter and base and o/p is taken across collector and base. In this configuration the emitter current I_E flows in the input circuit and the collector current I_C flows in the o/p circuit.



→ A change in emitter current produces a similar change in collector current.

Current amplification factor (α):-

The ratio of change in o/p current to change in i/p is called current amplification factor (α).

$$\alpha = \frac{\Delta I_C}{\Delta I_E}$$

Expression for collector current (I_C):-

→ The collector current consists of two parts

1) The current produced due to normal transistor act which is produced by majority carriers (αI_E).

ii) The leakage current due to movement of minority across collector-base junction or account of reverse bias.

$$I_C = \alpha I_E + I_{CB_0} \rightarrow (1)$$

We know, $I_E = I_B + I_C \rightarrow (2)$

sub (2) in (1)

$$I_C = \alpha(I_B + I_C) + I_{CB_0}$$

$$I_C = \alpha I_B + \alpha I_C + I_{CB_0}$$

$$I_C - \alpha I_C = \alpha I_B + I_{CB_0}$$

$$I_C(1-\alpha) = \alpha I_B + I_{CB_0}$$

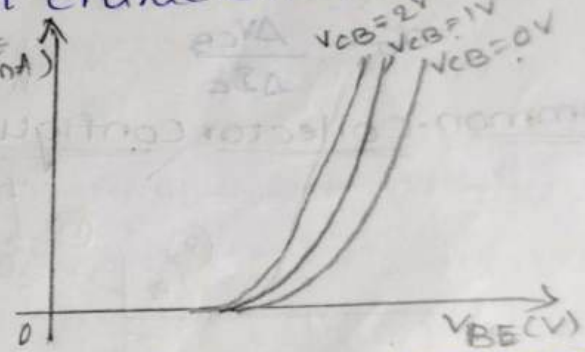
$$\boxed{I_C = \frac{\alpha}{1-\alpha} I_B + \frac{1}{1-\alpha} \cdot I_{CB_0}}$$

I/P and O/P characteristics of CB configuration:-

Input characteristics:-

→ The curve drawn between emitter current I_E and emitter base voltage V_{BE} for a given value of collector base voltage V_{BC} is known as input characteristics.

→ For a given value of V_{BC} the emitter-base junction is forward bias and acts like a P-N junction and so the curve is just like P-N junction.



With the increase in V_{CB} the collector base junction experiences a reverse bias and causes the depletion region at collector base junction to penetrate into base of the transistor and reduces the distance blw emitter-base regions and hence current conduct.

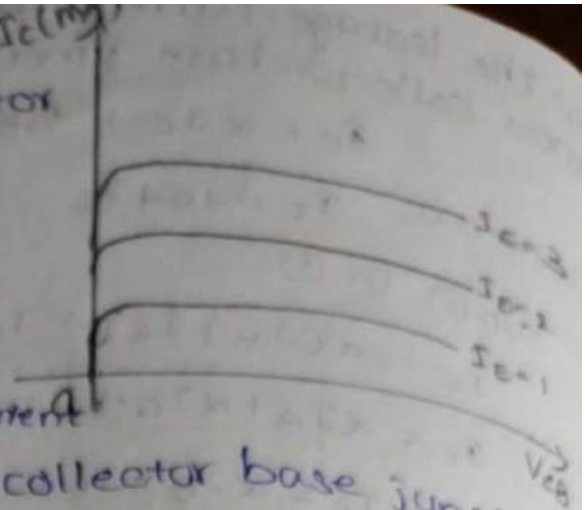
Input resistance (r_i):-

The ratio of change in input voltage ΔV_{BE} to change in input current ΔI_E.

$$r_i = \frac{\Delta V_{BE}}{\Delta I_E}$$

Output characteristics:-

→ The curve drawn between collector current (I_C) and collector base voltage V_{BC} for a given value of emitter current I_E is known as output characteristics



→ When I_E = 0mA only leakage current flows in the output region as collector base junction is reverse biased.

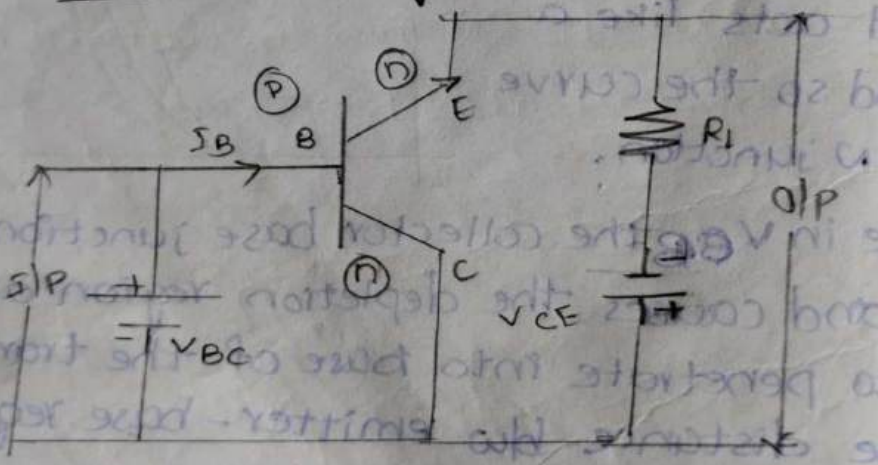
→ With the increase in I_E the collector current I_C is almost equal to I_E and appears to remain constant when V_{CB} is increased.

Output resistance:-

It is defined as the the ratio of change in o/p voltage ΔV_{CB} to change in o/p current ΔI_C

$$r_o = \frac{\Delta V_{CB}}{\Delta I_C}$$

Common-collector configuration:-



→ In cc configuration input is connected between ba and collector output is taken across emitter an collector.

→ In this configuration base current I_B flows in the input circuit and emitter current I_E flows in the output circuit.

current amplification factor (γ):-

It is defined as the ratio of change in output current to change in input current.

$$\gamma = \frac{\Delta I_E}{\Delta I_B}$$

Relation between α, β and γ:-

$$\alpha = \frac{\Delta I_C}{\Delta I_E} \quad \text{—} (1)$$

$$\beta = \frac{\Delta I_C}{\Delta I_B} \quad \text{—} (2)$$

$$\gamma = \frac{\Delta I_E}{\Delta I_B} \rightarrow (3)$$

We know that $I_E = I_B + I_C \rightarrow (4)$

Sub (4) in (3)

$$\gamma = \frac{\Delta (I_B + I_C)}{\Delta I_B}$$

$$\gamma = 1 + \frac{\Delta I_C}{\Delta I_B}$$

$$\boxed{\gamma = 1 + \beta}$$

$$\boxed{\beta = \gamma - 1}$$

$$\beta = \frac{\alpha}{1-\alpha}$$

$$\gamma = 1 + \frac{\alpha}{1-\alpha}$$

$$\gamma = \frac{1-\alpha+\alpha}{1-\alpha}$$

$$\boxed{\gamma = \frac{1}{1-\alpha}}$$

$$\gamma(1-\alpha) = 1$$

$$\gamma - \gamma\alpha = 1$$

$$\gamma - 1 = \gamma\alpha$$

$$\boxed{\alpha = \frac{\gamma - 1}{\gamma}}$$

Expression for output current (I_E):

$I_E = I_B + I_C \rightarrow (1)$

From CB configuration,

$I_C = \alpha I_E + I_{CBO} \rightarrow (2)$

Sub (2) in (1)

$I_E = I_B + \alpha I_E + I_{CBO}$

$I_E - \alpha I_E = I_B + I_{CBO}$

$I_E(1-\alpha) = I_B + I_{CBO}$

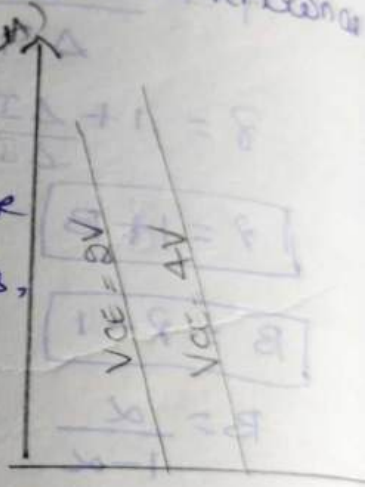
$I_E = \frac{1}{1-\alpha} \cdot I_B + \frac{1}{1-\alpha} I_{CBO}$

$$\boxed{I_E = \gamma I_B + \gamma I_{CBO}}$$

Input characteristics:-

→ The curve drawn between collector base voltage and base current by keeping V_{CE} as constant is known as input characteristics

→ With the low value of V_{BC} the base current is more and with the increase in V_{BC} the base current I_B is decreases, because increased V_{BC} will reduce the space of base region



Input resistance (r_i):-

The ratio of change in input voltage ΔV_{BC} to change in input current ΔI_B is known as input resistance

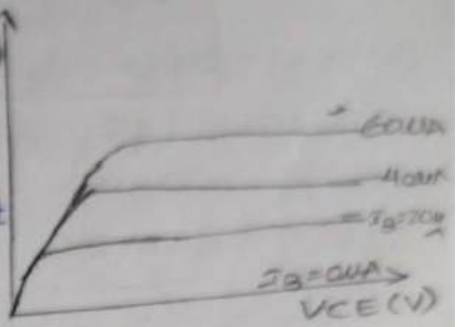
$$\boxed{r_i = \frac{\Delta V_{BC}}{\Delta I_B}}$$

Output characteristics of CC configuration:

→ The curve drawn between collector emitter voltage V_{CE} and emitter current I_E at a constant base current I_B is known as output characteristics.

→ At $I_B = 0\mu A$ only small current flows in the output region which is known as reverse leakage current.

→ From the expression of emitter current ($I_E = \gamma I_B + (\gamma+1) I_{CBO}$) we can say that increased base current will increase the emitter current by 'γ' times of I_B.



Output resistance (r_o):-

It is defined as the ratio of change in output voltage V_{CE} to change in output current I_E is known as output resistance.

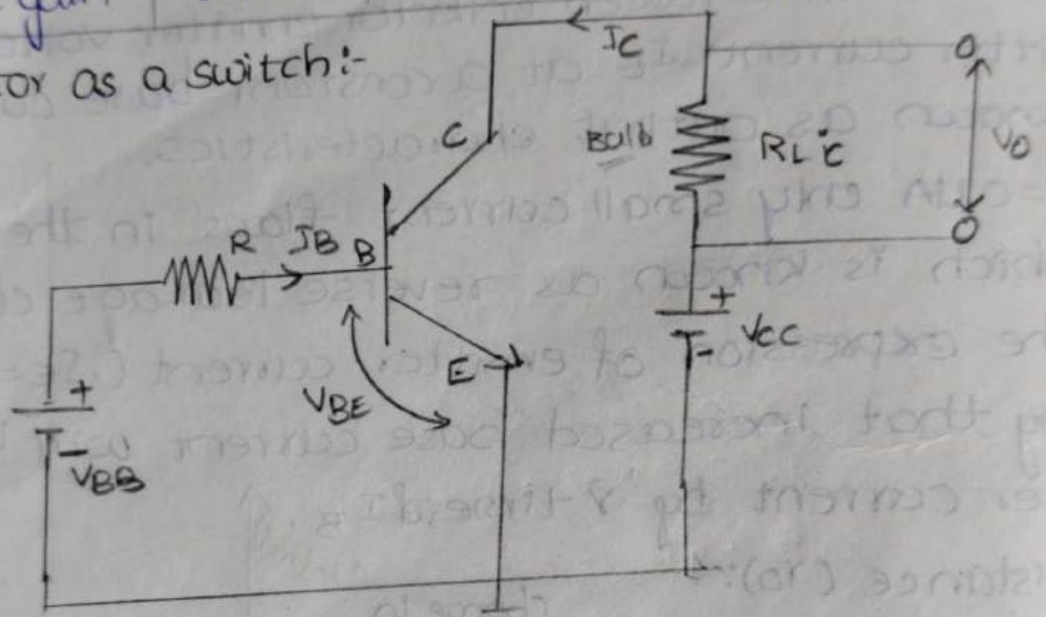
$$r_o = \frac{\Delta V_{CE}}{\Delta I_E}$$

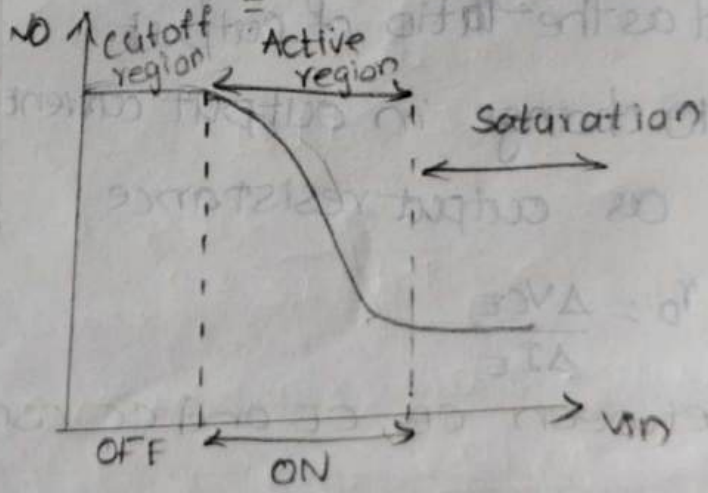
Comparison between CB, CE and CC configurations :-

Parameter	CB configuration (E B C)	CE configuration (B E C)	CC configuration (B C E)
common terminal	Base	Emitter	collector
Input terminal	Emitter	Base	Base
output terminal	collector	collector	Emitter
Input resistance	$r_i = \frac{\Delta V_{BE}}{\Delta I_E}$ low	$r_i = \frac{\Delta V_{BE}}{\Delta I_B}$ medium	$r_i = \frac{\Delta V_{BC}}{\Delta I_B}$ very high
output resistance	$r_o = \frac{\Delta V_{CB}}{\Delta I_C}$ Very high	$r_o = \frac{\Delta V_{CE}}{\Delta I_C}$ high	$r_o = \frac{\Delta V_{CE}}{\Delta I_E}$ low
Current gain	$\alpha = \frac{\Delta I_C}{\Delta I_E}$ less than unity	$\beta = \frac{\Delta I_C}{\Delta I_B}$ high	$\gamma = \frac{\Delta I_E}{\Delta I_B}$ Very high
Application	High frequency	audio signal amplifier	For impedance matching

voltage gain	low	high	very low

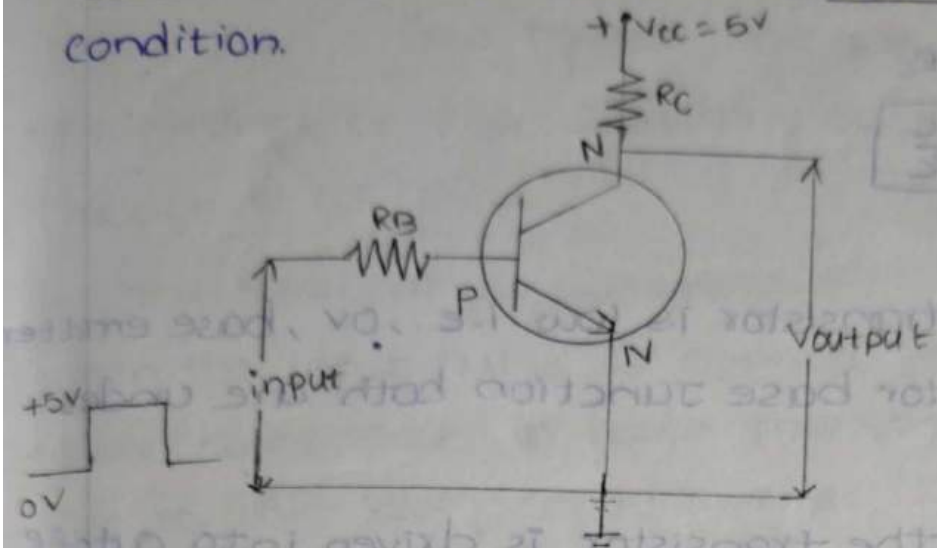
Transistor as a switch:-





Transistor as a switch :-

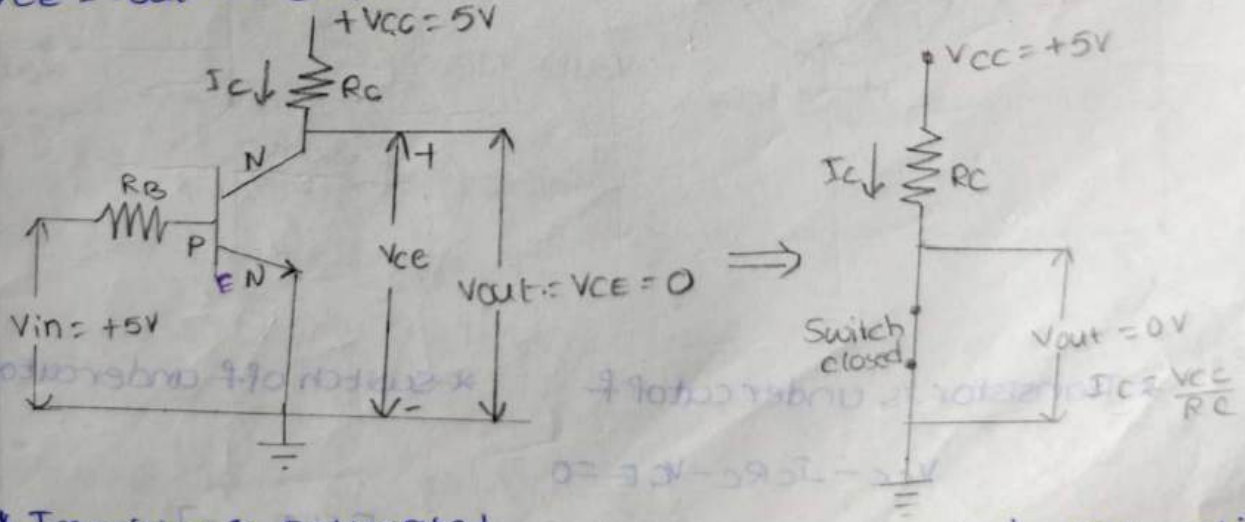
→ In switching circuits, a transistor is operated at cutoff for off condition and at saturation for the ON condition.



Transistor as a switch

i) **Saturation Region:-** When the input to transistor is high i.e., +5V; the base emitter Junction is forward biased as the transistor is NPN.

At this condition the transistor is driven into saturation and said to be ON & acts as a closed switch. Now, the voltage between collector and emitter is zero (VCE = Vout = 0) and the current is maximum.



* Transistor is saturated

* Switch ON under saturation

→ Apply KVL to the output loop

$V_{cc} - I_c R_c - V_{CE} = 0$

$V_{cc} = I_c R_c + V_{CE}$ [$\because V_o = V_{CE} = 0$]

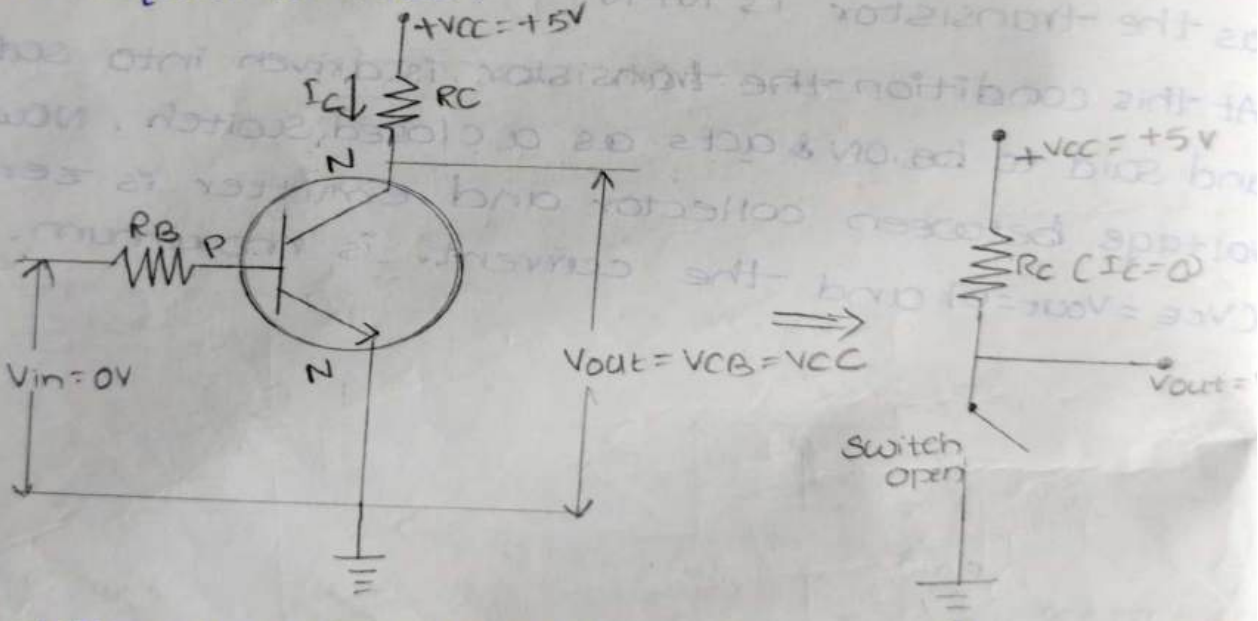
$V_{cc} = I_c R_c$

$$I_c = \frac{V_{cc}}{R_c}$$

ii) cutoff Region:-

→ When the input to transistor is low i.e., 0V, base em Junction and collector base junction both are unde reverse biased.

→ At this condition, the transistor is driven into cut and said to be off & acts as a open switch. Now a small current i.e., Negligible current flows through the transistor [$I_c = 0$] and the output voltage V_{out} will be equal to $+V_{cc}$.



* Transistor is under cutoff

* Switch off under cutoff

$V_{cc} - I_c R_c - V_{CE} = 0$

$V_{cc} = V_{CE} + I_c R_c$ [$\because I_c = 0$]

$V_{CE} = V_{cc}$

$V_{CE} = +5V$

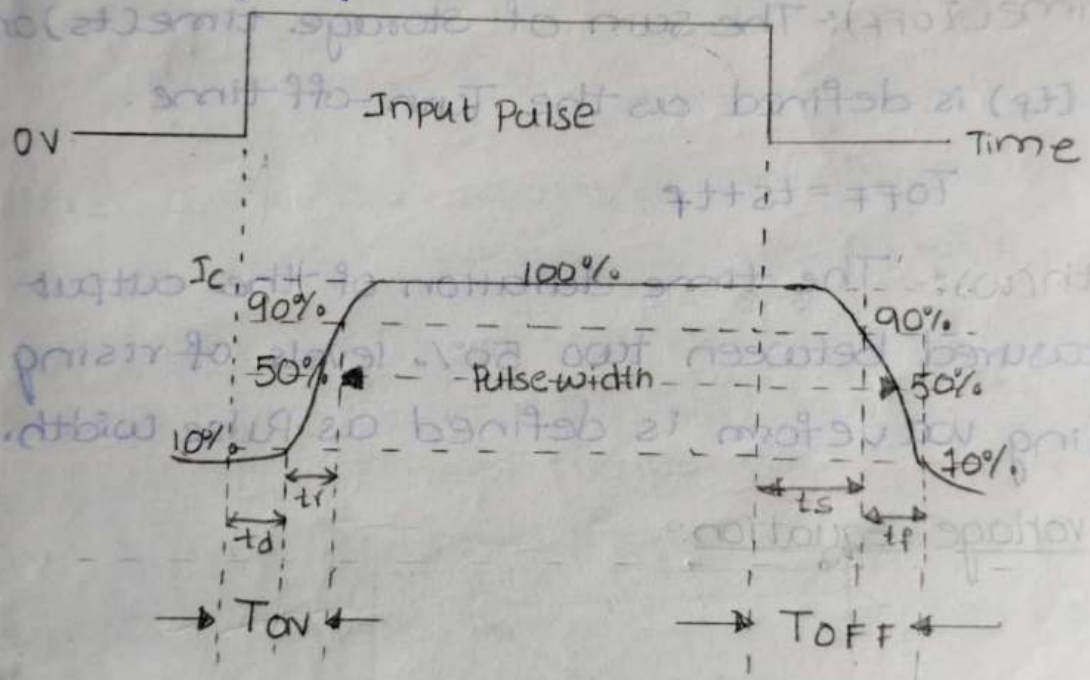
Switching Times:-

The switching transistor has a pulse as an input and a pulse with few variations will be the output. There are a few terms that you should know regarding the timings of the switching output pulse. Let us go through it as below

Let the input pulse duration = T

when the input pulse is applied the collector current takes some time to reach the steady state value, due to the stray capacitances.

The following figure explains this concept.



Output Pulse

From the figure above,

Time delay (td):- The time taken by the collector current to reach from its initial value to 10% of its final value is called as the Time Delay.

Rise time (tr):- The time taken for the collector current to reach from 10% of its initial value to 90% of its final value is called as Rise Time.

Turn-on time (T_{ON}):- The sum of time delay (t_d) and rise time (t_r) is called as Turn-on time.

$$T_{ON} = t_d + t_r$$

Storage time (t_s):- The time interval between the trailing edge of the input pulse to the 90% of the maximum value of the output, is called as the storage time.

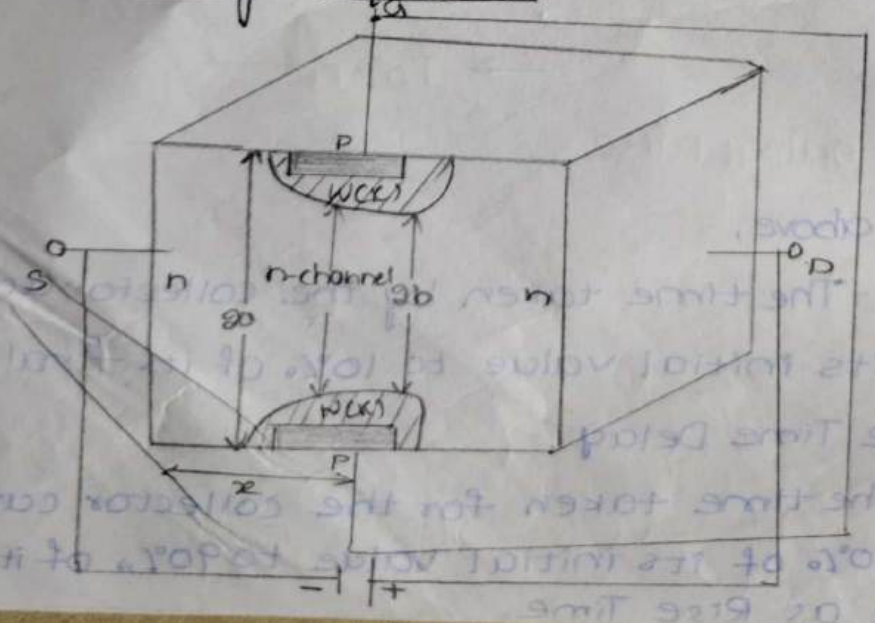
Fall time (t_f):- The time taken for the collector current to reach from 90% of its maximum value to 10% of its initial value is called as the fall Time.

Turn-off time (T_{OFF}):- The sum of storage time (t_s) and fall time (t_f) is defined as the Turn-off time.

$$T_{OFF} = t_s + t_f$$

Pulse width (w):- The time duration of the output pulse measured between two 50% levels of rising and falling waveform is defined as Pulse width.

Pinch off voltage equation:-



$N_A >> N_D$

where N_a is the acceptor ion impurity(holes)

N_D is the Donar ion impurity (electrons)

$W(x) = W_n(x) + W_p(x)$

where $W(x)$ is the p-n junction total depletion region width.

→ Here depletion region pentration is the corrbinatio of n-type channel and p-type gate.

So, $W(x) = W_n(x) + W_p(x)$

$W_p << W_n$

where W_p is very small width compare to W_n so we neglect $W_p(x)$.

$$\boxed{W(x) = W_n(x)}$$

→ $W(x) = a - b(x)$

Here a is the width of the channel and b is width of the channel at drain side.

W is the width of the depletion layer.

b(x) is the parameter defined at the channel width at different value of x.

x is the distance from the source

→ We have already know that junction potential incase of p-n junction diode is

$$V_j = \frac{q N_D W^2}{2\varepsilon}$$

where q is the charge of the electron ($q = 1.6021 \times 10^{-19} C$)

ε = dielectric constant of the channel material

$$W^2 = \frac{2\varepsilon}{q N_D} \cdot V_j$$

$$W = \left[\frac{2\varepsilon}{qN_D} \cdot V_j\right]^{\frac{1}{2}} \longrightarrow (1)$$

But we also know that $V_j = V_o - V_d \longrightarrow (2)$

where V_j is the junction potential

V_o is the contact potential

V_d is the applied voltage (gate channel)

Sub (2) in (1)

$$W = \left[\frac{2\varepsilon}{qN_D}(V_o - V_d)\right]^{\frac{1}{2}}$$

$$W(x) = a - b(x) = \left[\frac{2\varepsilon}{qN_D}(V_o - V_d)\right]^{\frac{1}{2}} \longrightarrow (3)$$

$a - b(x)$ = pentration $W(x)$ of the depletion region in the channel at distance x from the source

Now assume that pinch off has occured then

$b(x) = b = 0$ and $V_d = V_P$

$$W(x) = a - 0 = \left[\frac{2\varepsilon}{qN_D}(V_o - V_P)\right]^{\frac{1}{2}}$$

$$a^2 = \frac{2\varepsilon}{qN_D}(V_o - V_P)$$

$$V_o - V_P = \frac{qN_D}{2\varepsilon} \cdot a^2$$

Here V_o is in microvolts so we can neglect

$$-V_P = \frac{qN_D}{2\varepsilon} \cdot a^2$$

$$|V_P| = \frac{qN_D}{2\varepsilon} a^2 \longrightarrow (4)$$

Relation between V_{GS} and V_P

Put $V_o - V_d = V_{GS}$ in eqn (3)

$$a - b(x) = \left[\frac{2\varepsilon}{qN_D} V_{GS}\right]^{\frac{1}{2}}$$

$$(a-b)^2 = \frac{2\varepsilon}{qN_D} V_{GS}$$

$$V_{GS} = \frac{qN_D}{2\varepsilon}(a-b)^2$$

$$V_{GS} = \frac{qN_D}{2\varepsilon} \cdot \frac{a^2(a-b)^2}{a^2}$$

$$V_{GS} = V_P \cdot \left(\frac{a-b}{a}\right)^2 \quad [\because \text{eqn } \textcircled{4}]$$

$$\boxed{V_{GS} = V_P\left(1-\frac{b}{a}\right)^2}$$

Problems:-

1. For an n-channel FET with $a = 3\times10^{-4}$ cm, $N_D = 10^{15}$ electron /cubic cm. Find

i) Pinch off voltage

ii) The channel half width for $V_{GS} = \frac{1}{2}V_P$ and $I_D = 0$, $\varepsilon_r = 12\varepsilon_0$

Sol:- Given that,

$\varepsilon_r = 12\varepsilon_0$

$a = 3\times10^{-4}$ cm

$N_D = 10^5$ electrons/cubic cm

$V_{GS} = \frac{1}{2}V_P$

where $\varepsilon_0 = 8.854\times10^{-12}$ F/m $\quad q = 1.605\times10^{-19}$

$$V_P = \frac{qN_D \cdot a^2}{2\varepsilon_r}$$

$$= \frac{1.605\times10^{-19}\times10^5}{2\times12\times8.854\times10^{-12}} \times (3\times10^{-4})^2$$

$$= 0.067$$

$$V_{GS} = V_P\left(1-\frac{b}{a}\right)^2$$

$$\frac{V_{GS}}{V_P} = \left(1-\frac{b}{a}\right)^2$$

$$\sqrt{\frac{V_{GS}}{V_P}} = 1-\frac{b}{a}$$