Nanoscale Device Engineering (EC 502)

Syllabus

Unit – I

L =3, T = 0, P = 0, C = 3

- Introduction to Nanoscience and Nanotechnologies

Unit – 2

- Fabrication Technology & SPICE Device Models

  (VLSI Processes: Introduction, Twin-Well CMOS Process, Integrated Devices, MOSFETs, Resistors, Capacitors, pn Junction Diodes, BiCMOS Process, Lateral pnp Transistor, p-Base and Pinched-Base, Resistors, SiGe BiCMOS Process, VLSI Layout, Beyond 20nm Technology Implications of Technology Scaling: Issues in Deep-Submicron Design: Silicon Area, Scaling Implications, Velocity Saturation, Subthreshold Conduction, PVT Variations, Wiring: The Interconnect, SPICE Device Models: The Diode Model, The Zener Diode Model, MOSFET Models, The BJT Model)

Unit – 3

- Applications of Nanoscience and Nanotechnologies

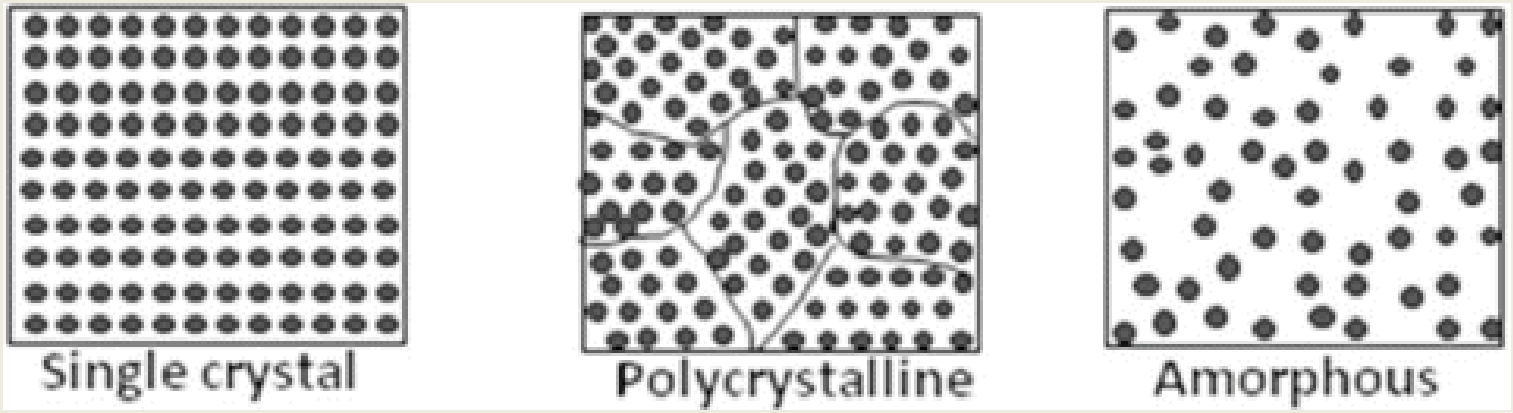
  (Information and Communication Technologies: Integrated Circuits, Data Storage, Photonics, Displays, Information storage devices, Wireless sensing and communication)

VLSI Fabrication Process

Crystal Growth and Wafer Preparation

- Polycrystalline Silicon (Si) is used as the starting material for the growth of device quality Single Crystal Si.
- There are following 3 types of Si:

1. Amorphous Silicon – No crystal order, More defects
2. Polycrystalline Silicon – Multiple crystal order, Less defects
3. Single Crystal Silicon – Uniform crystal order, Negligible defects



VLSI Fabrication Process

Crystal Growth and Wafer Preparation

Electronic Grade Silicon (EGS)

- EGS is a polycrystalline material of high purity.
- It is a raw material for the preparation of Single Crystal Si.
- It is 99.9% pure.
- EGS is obtained from quartzite (relatively pure form of sand SiO_2).

Quartzite

↓

(Metallurgical Grade Si) MGS

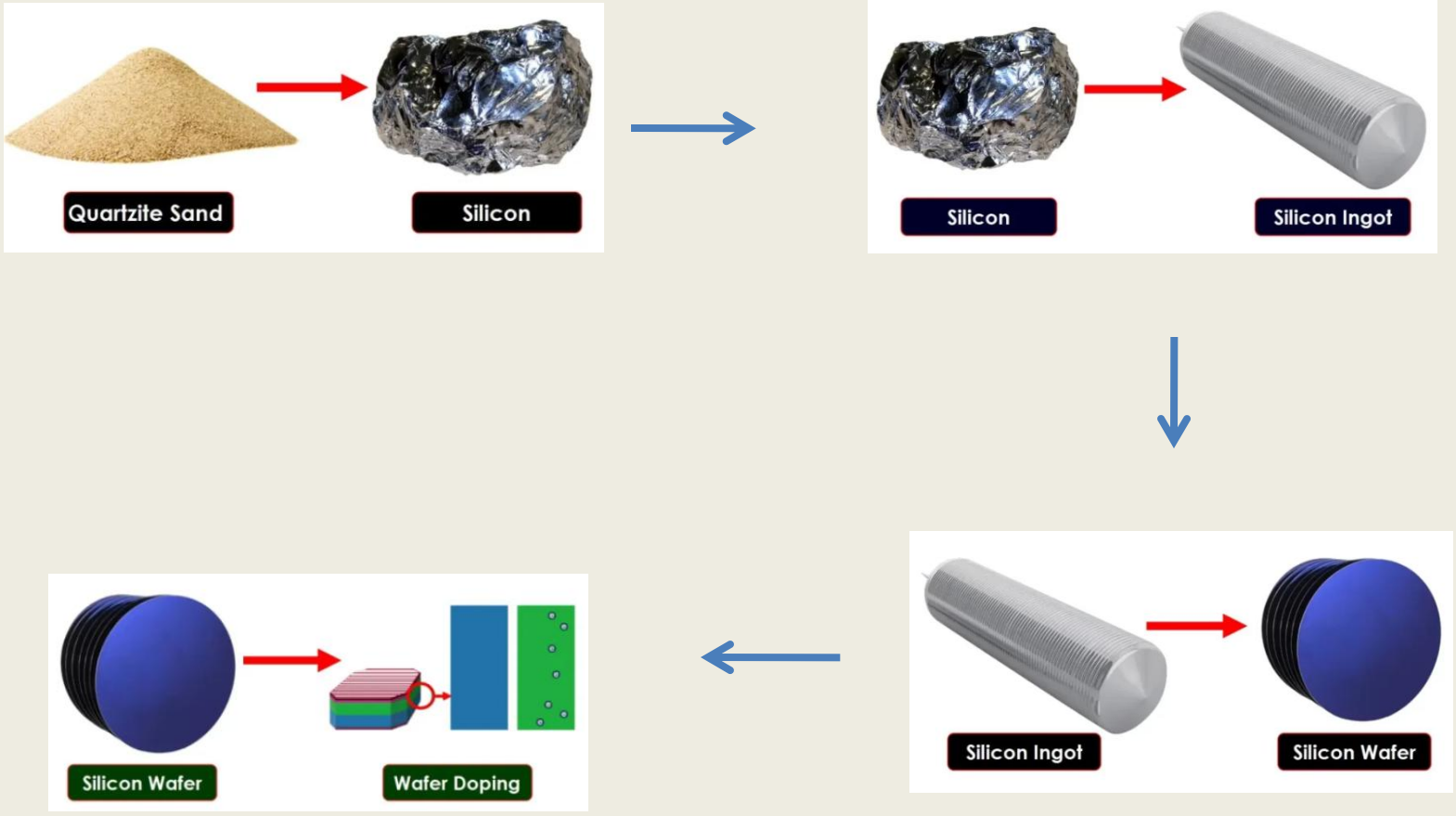
↓

EGS

VLSI Fabrication Process

Crystal Growth and Wafer Preparation

Electronic Grade Silicon (EGS)



VLSI Fabrication Process

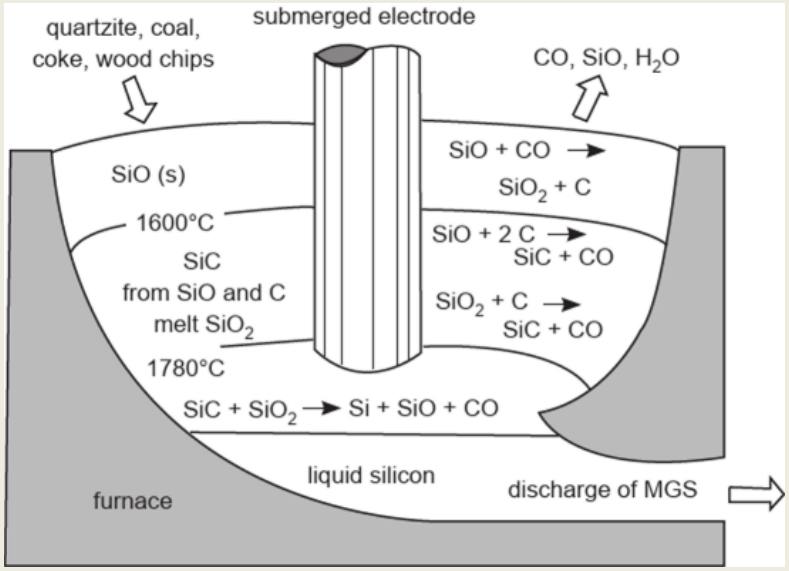
Crystal Growth and Wafer Preparation

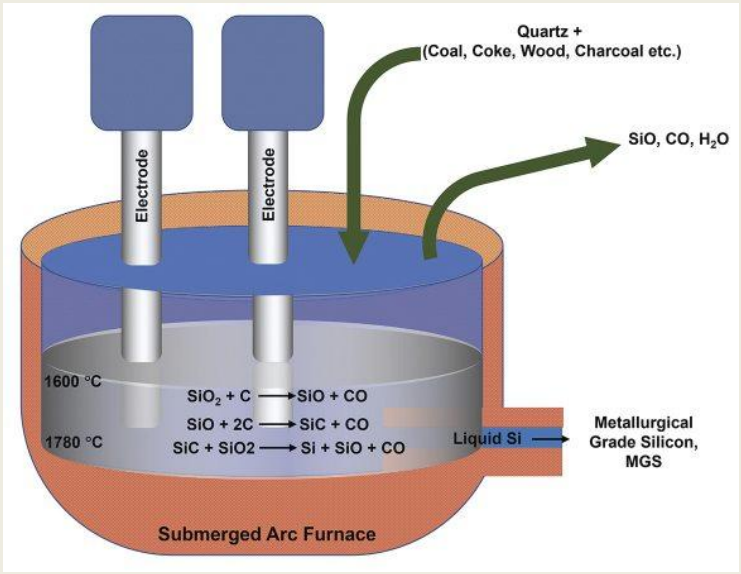
Obtaining EGS from Ore (Quartzite) – It is done in following steps:

1. **Quartzite to MGS**

- It is performed in submerged electrode arc furnace filled with quartzite, coal, coke and wood chips.

  $3C\ (solid) + 2\ SiO_2\ (solid) = Si\ (liquid) + SiO\ (gas) + CO\ (gas)$





VLSI Fabrication Process

Crystal Growth and Wafer Preparation

$SiO_2 + C = SiO + CO$

$SiO + 2C = SiC + CO$

$SiC + SiO_2 = Si\ (MGS) + SiO\ (gas) + CO\ (gas)$

- MGS has a purity of 98%.

2. In next step, MGS is treated with anhydrous HCL to form trichlorosilane ($SiHCl_3$).

$Si\ (solid) + 3HCl\ (gas) = SiHCl_3 + H_2\ (gas)$

- $SiHCl_3$ is liquid at room temperature (B.P. 32^0C).

3. EGS is prepared from $SiHCl_3$ in a chemical vapor deposition process.

$2SiHCl_3\ (gas) + 2H_2 = 2\ Si\ (solid\ EGS) + 6\ HCl\ (gas)$

- EGS is 99.99% pure and it is used as the starting material for the manufacturing of Single Crystal Silicon.

VLSI Fabrication Process

Crystal Growth and Wafer Preparation

Single Crystal Silicon:

- Single crystal silicon, also known as mono-crystalline silicon, is a form of silicon where the entire solid has a continuous, unbroken crystal lattice structure with no grain boundaries.
- It is a highly pure and crystalline material.
- Its uniform structure and properties make it ideal for fabrication of high - efficiency solar cells and semiconductor devices.

EGS to Single Crystal Silicon is prepared using following three techniques:

1. **Czochralski Method (CZ)** - Most Used; and used for both Si and GaAs
2. **Float Zone Method (FZ)** - very pure but high cost
3. **Bridgeman technique** - for compound semiconductors

VLSI Fabrication Process

Crystal Growth and Wafer Preparation

Single Crystal Silicon:

EGS to Single Crystal Silicon is prepared using following three techniques:

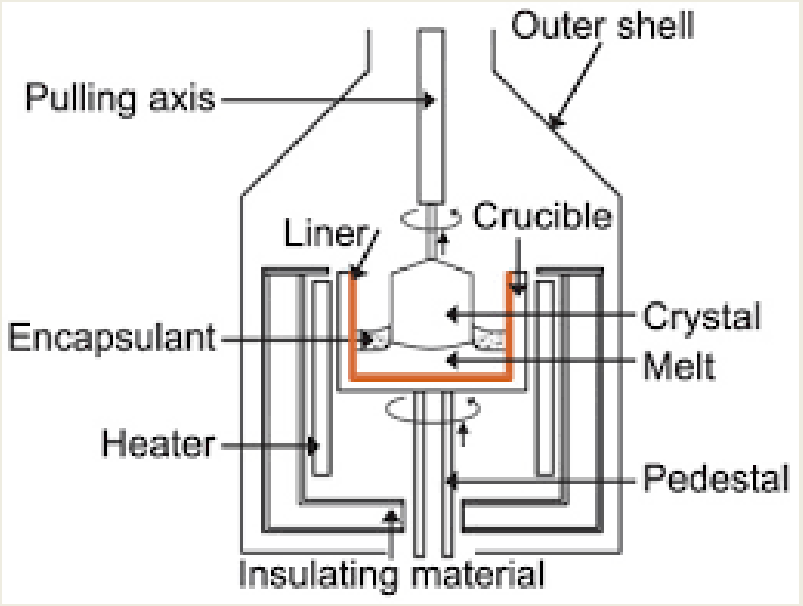
1. Czochralski Method (CZ) - Most Used; and used for both Si and GaAs
2. Float Zone Method (FZ) - very pure but high cost
3. Bridgeman technique - for compound semiconductors

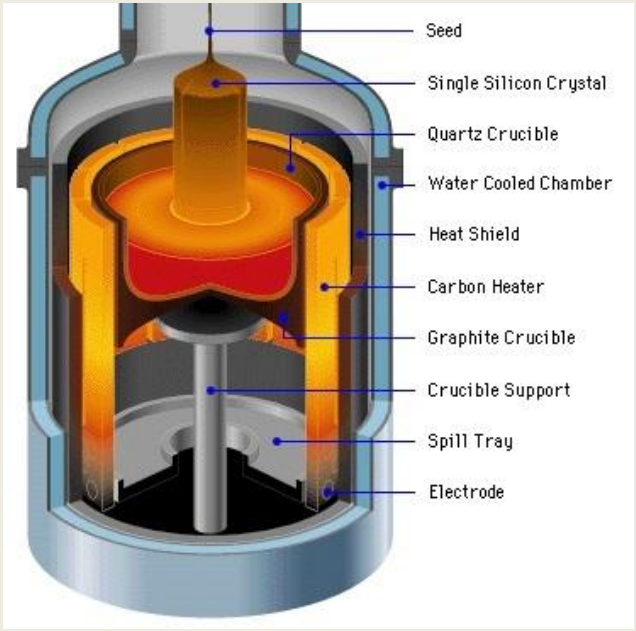
VLSI Fabrication Process

Crystal Growth and Wafer Preparation

1. Czochralski Method (CZ)

- Single crystal Si is produced by melting polycrystalline Si and then resolidifying it.
- Electronic grade silicon is loaded into quartz crucible and heated to ~ 1500 ^{o}C in presence of Argon (Ar) inert gas.

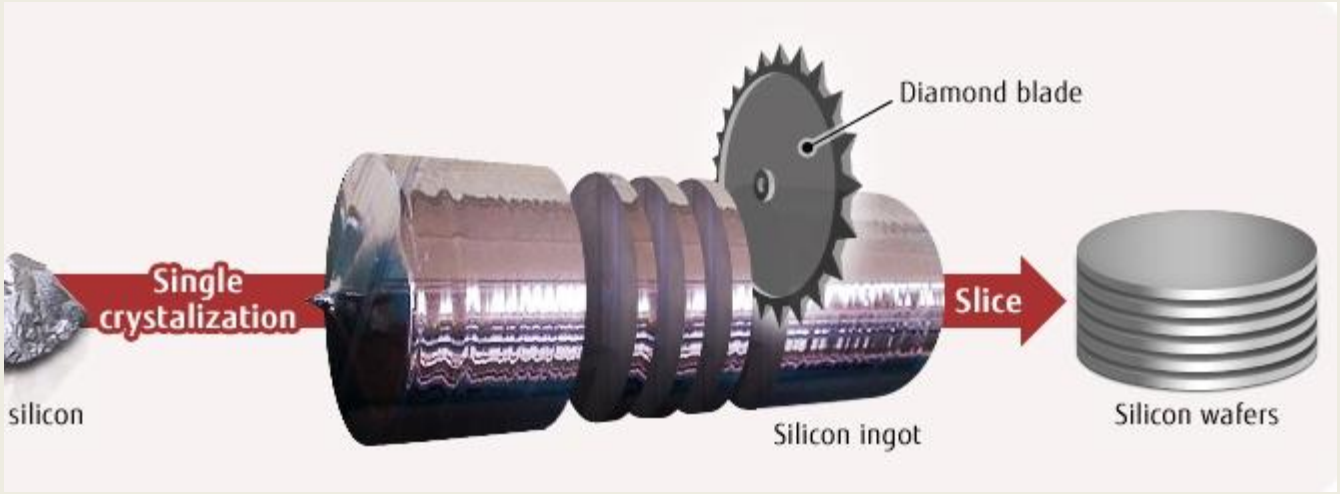




VLSI Fabrication Process

Crystal Growth and Wafer Preparation

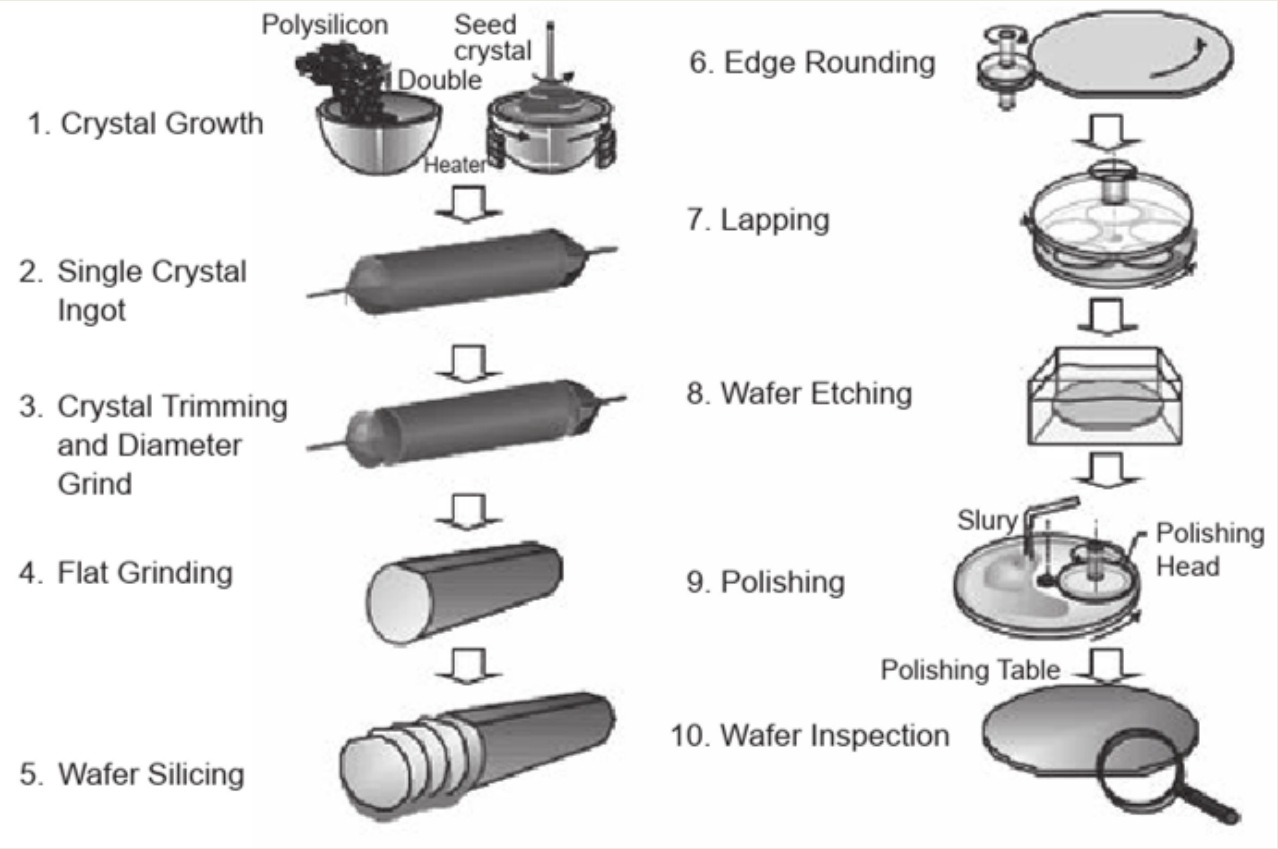
- A seed crystal with the desired orientation is lowered into the melt and rotated counter clockwise slowly while crucible is rotated clockwise.
- The quartz crucible is normally discarded after the process is terminated.



VLSI Fabrication Process

Wafer Preparation

- A **wafer** is a thin slice of Single crystal Silicon used for the fabrication of integrated circuits.



VLSI Fabrication Process

Diode fabricatrion:

There are following steps in the fabrication of diode:

1. Wafer Preparation
2. Oxidation
3. Masking
4. Lithography
5. Etching
6. Diffusion or Ion implantation
7. Metallization
8. Packaging

CMOS Fabrication Process

- The CMOS can be fabricated using different processes such as:

1. N-well process
2. P-well process
3. Twin tub process

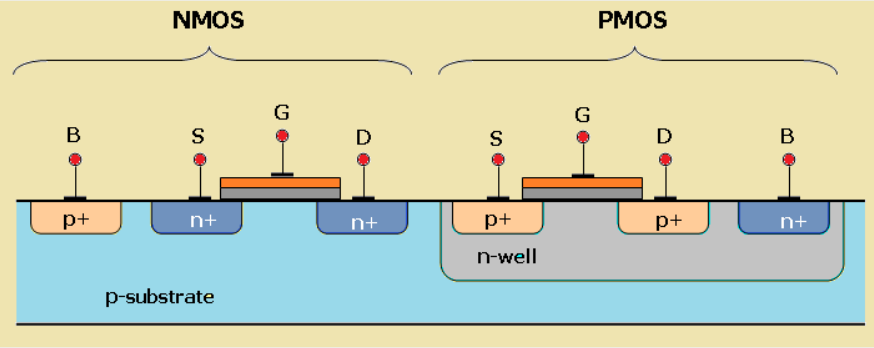


Fig. 1 N–well process

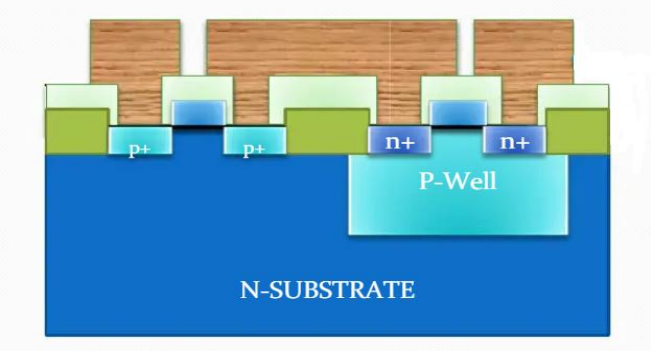


Fig. 2 P-well process

CMOS Fabrication Process

- **Twin-tub CMOS Process**

➢ The twin-well CMOS fabrication process, also known as the twin-tub process, is a method for creating both n-channel (nMOS) and p-channel (pMOS) transistors on the same silicon substrate.

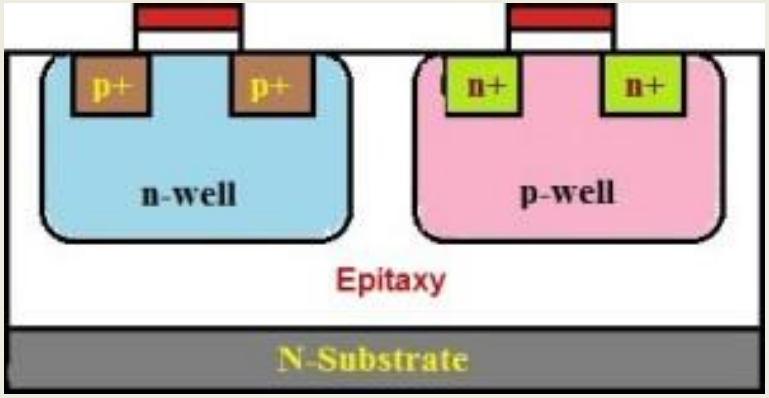
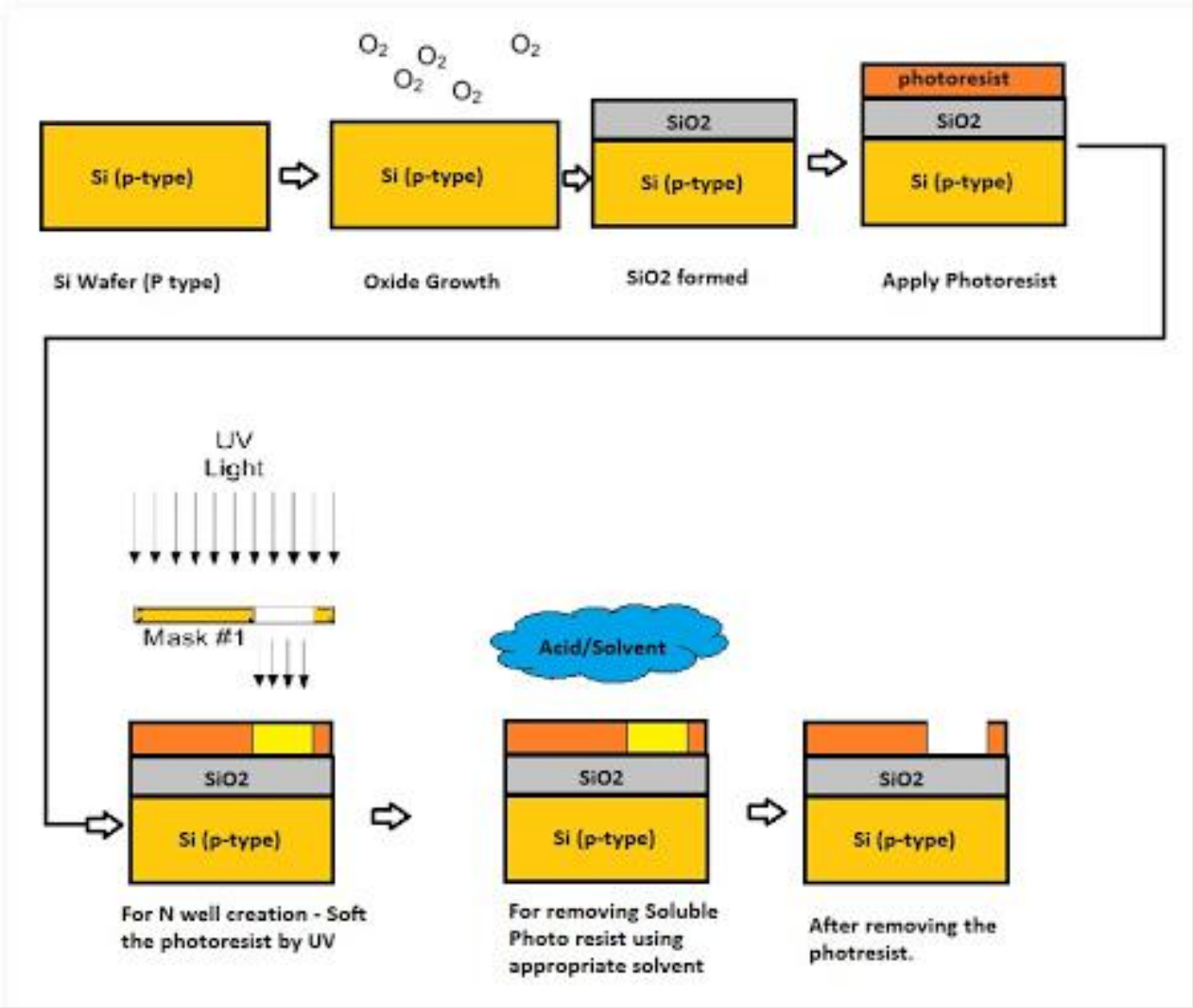


Fig. 3 Twin Tub process

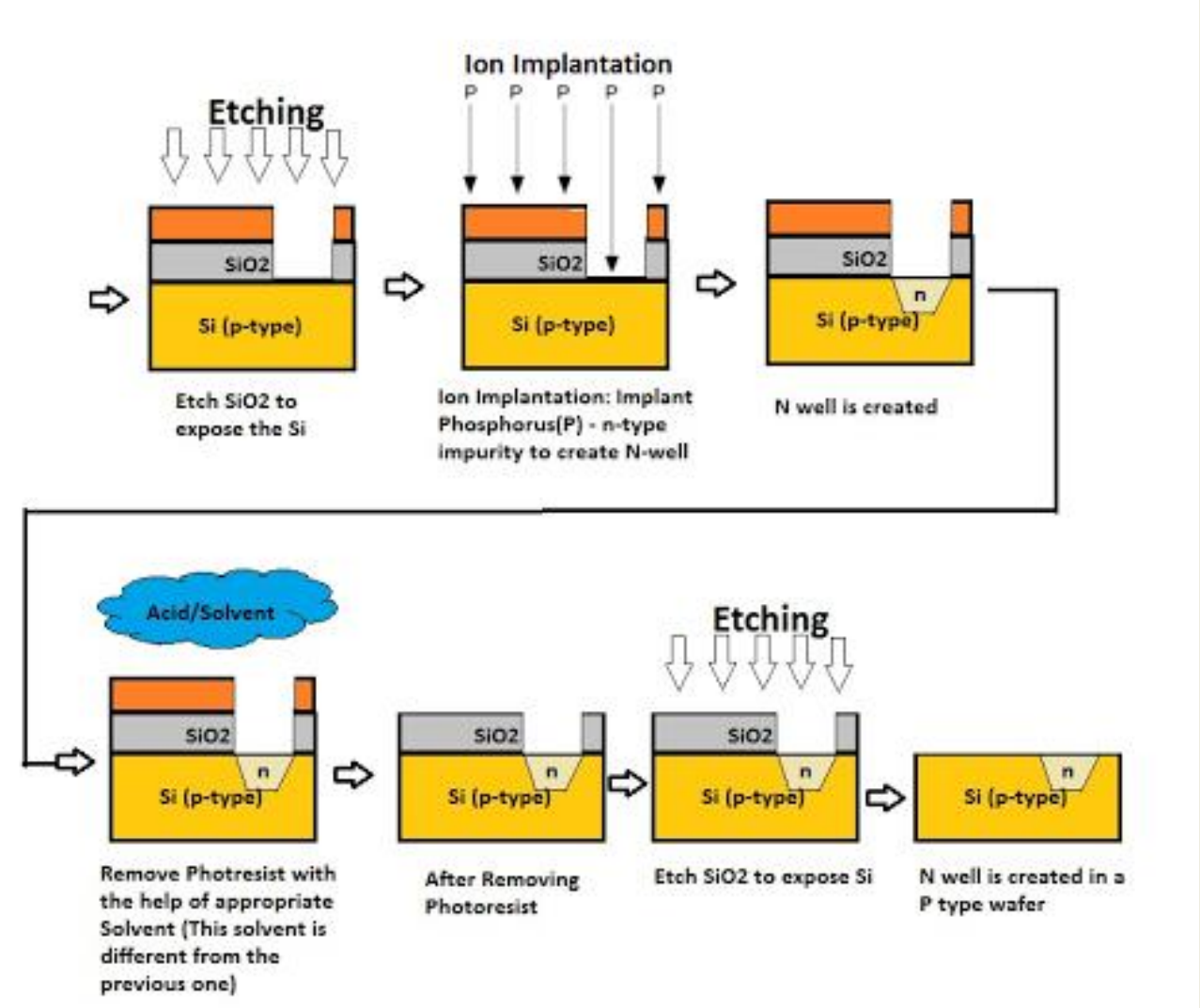
CMOS Fabrication Process

- **N-well fabrication steps**



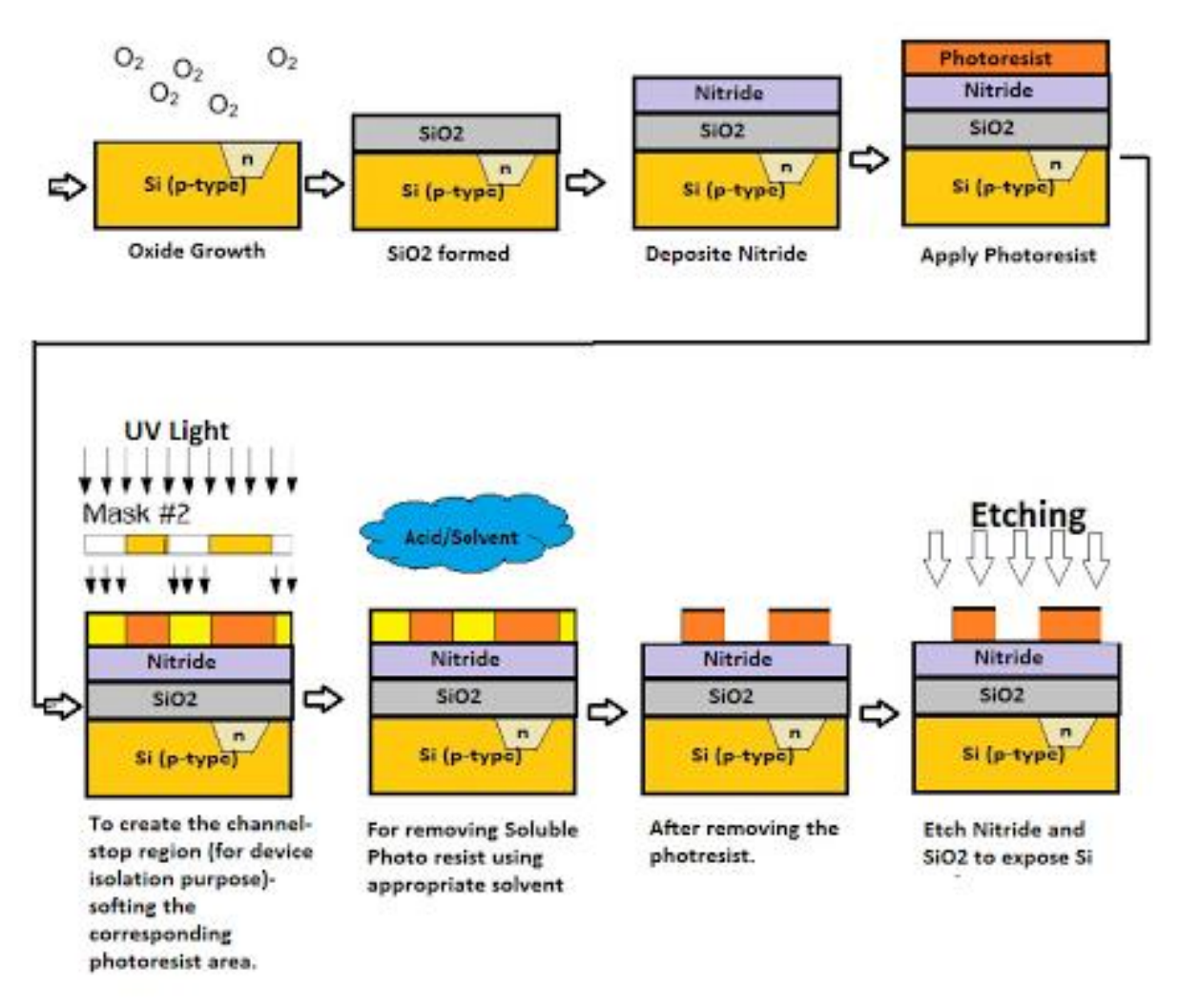
CMOS Fabrication Process

- **N-well fabrication steps**



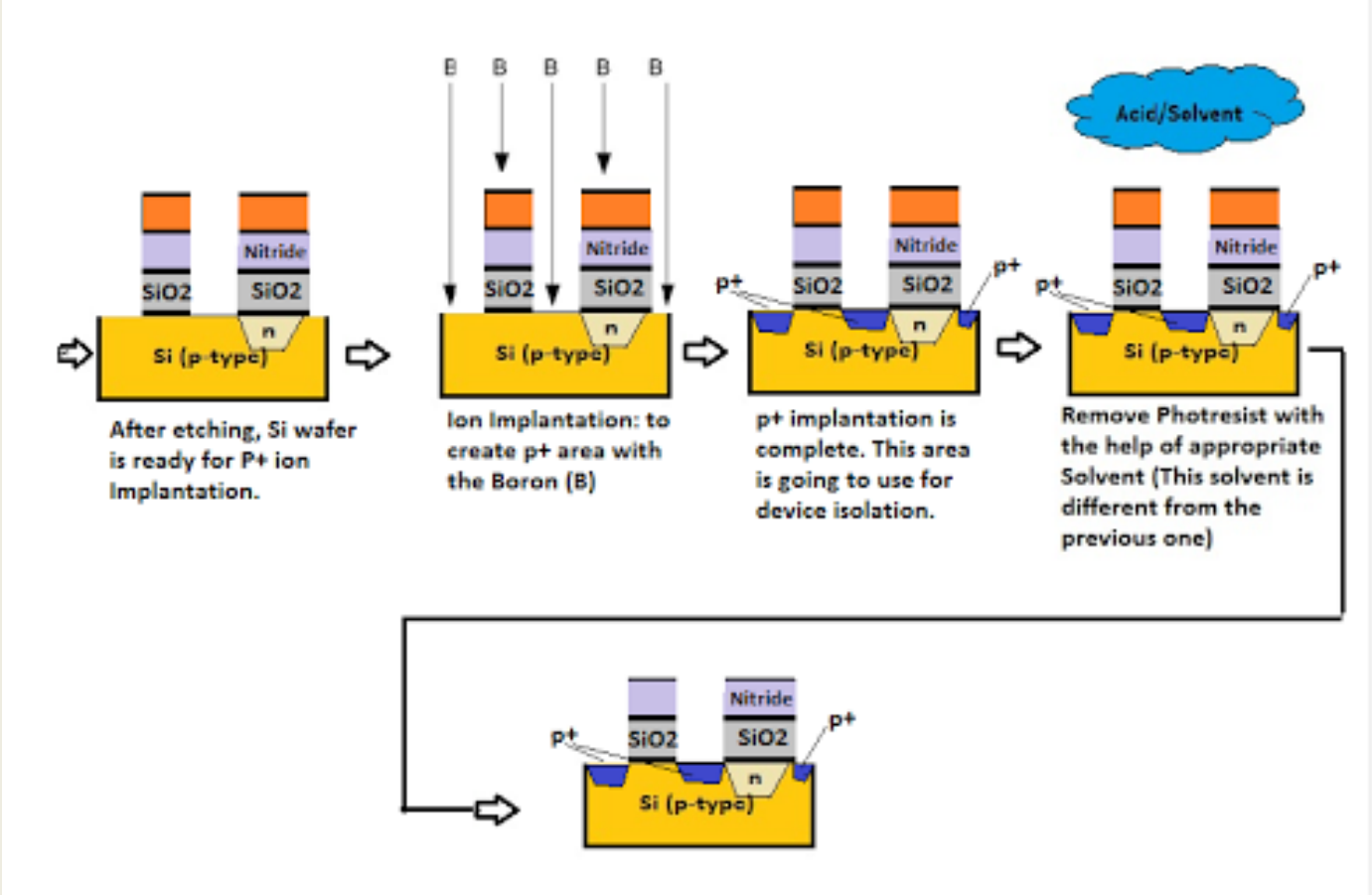
CMOS Fabrication Process

- **N-well fabrication steps**



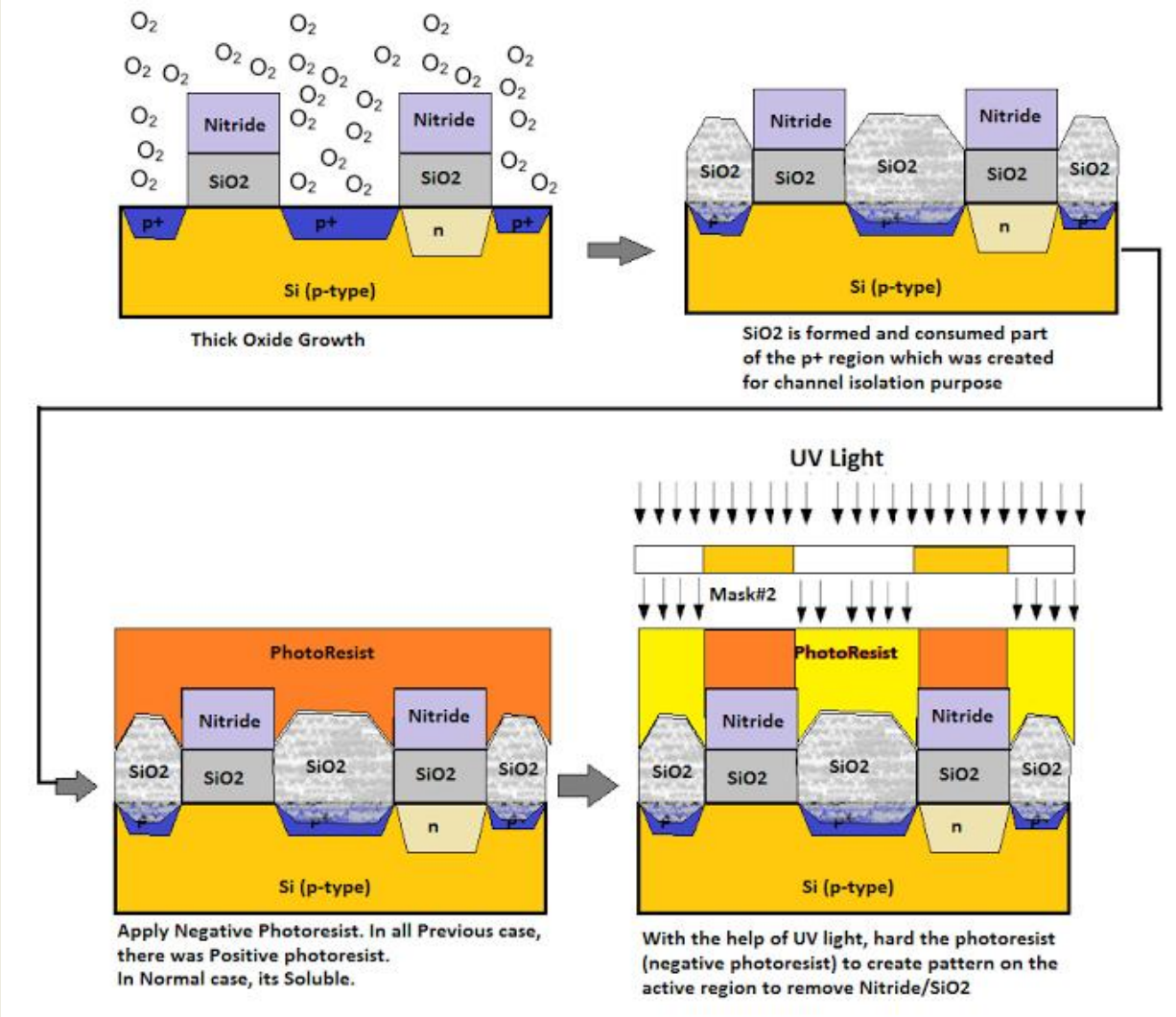
CMOS Fabrication Process

- **N-well fabrication steps**



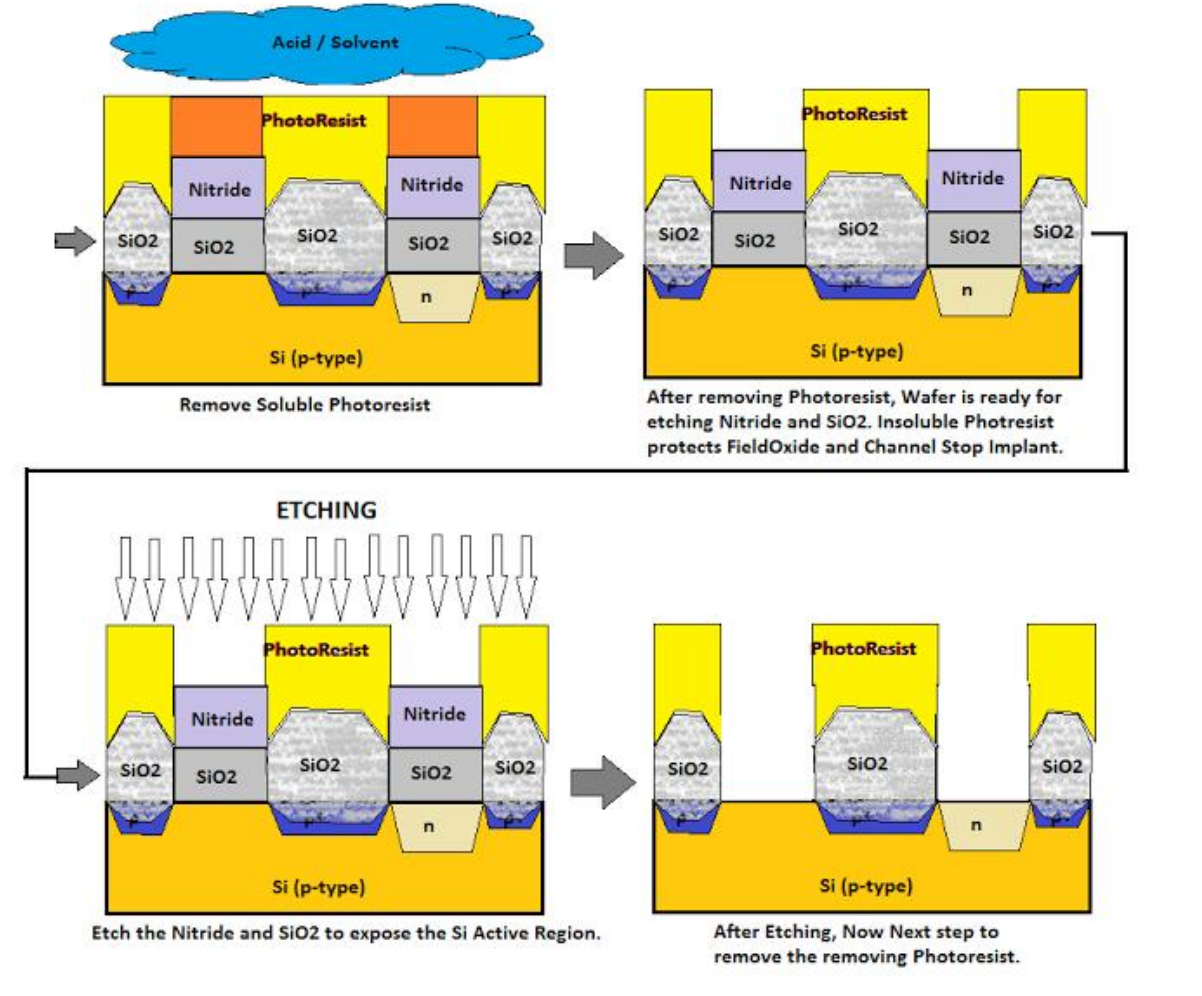
CMOS Fabrication Process

- **N-well fabrication steps**



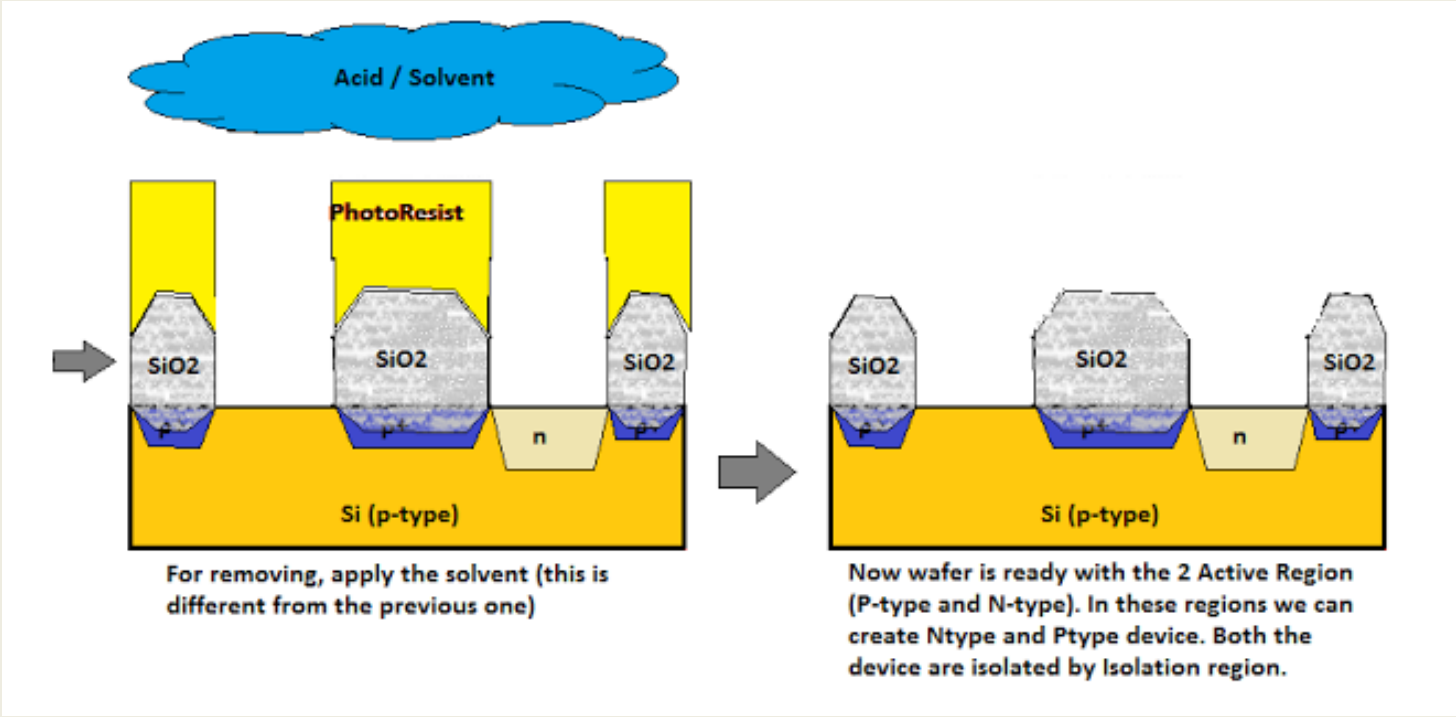
CMOS Fabrication Process

- **N-well fabrication steps**



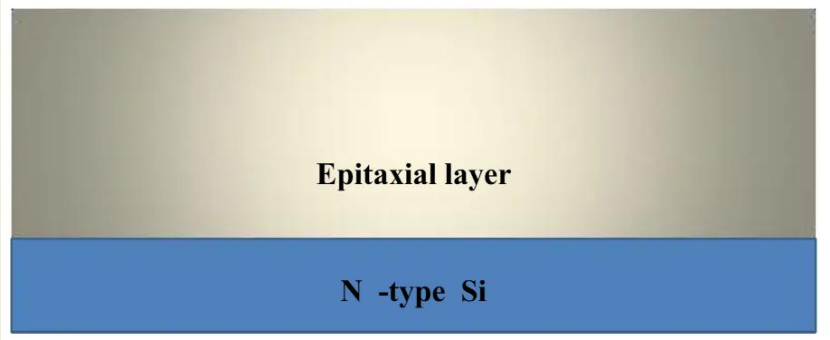
CMOS Fabrication Process

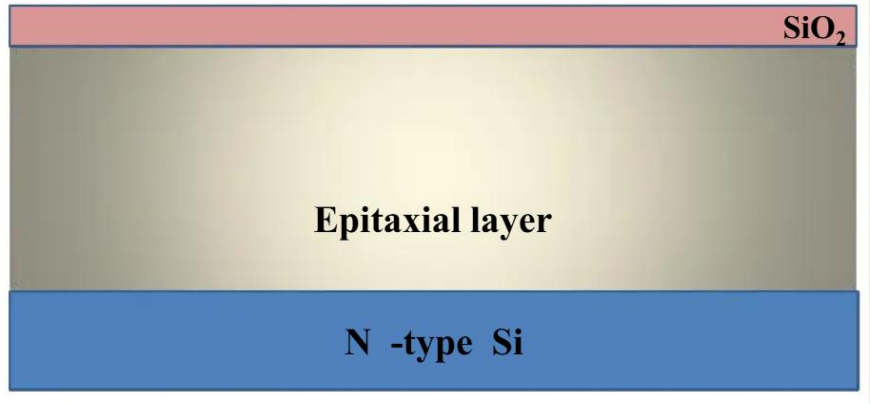
- **N-well fabrication steps**

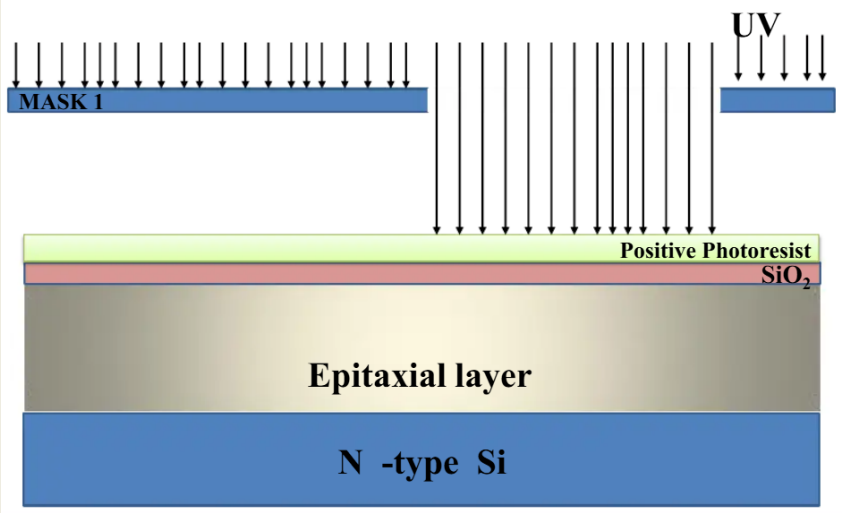


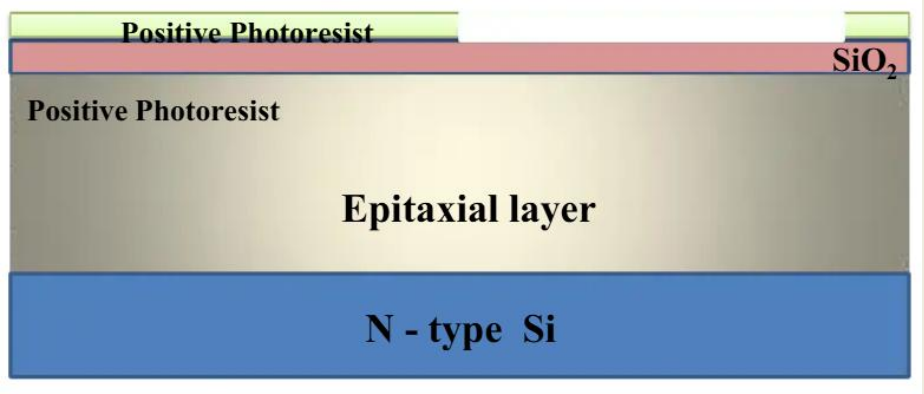
CMOS Fabrication Process

- **Twin-tub fabrication steps**



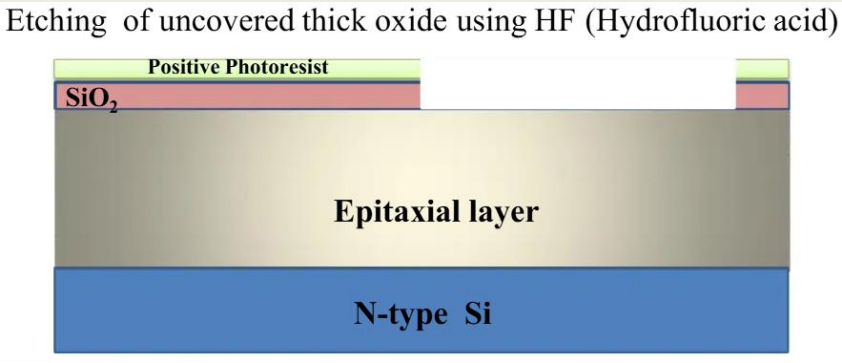


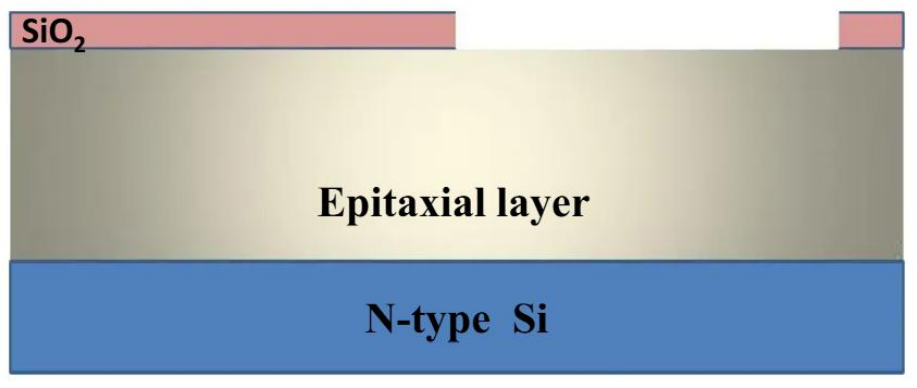


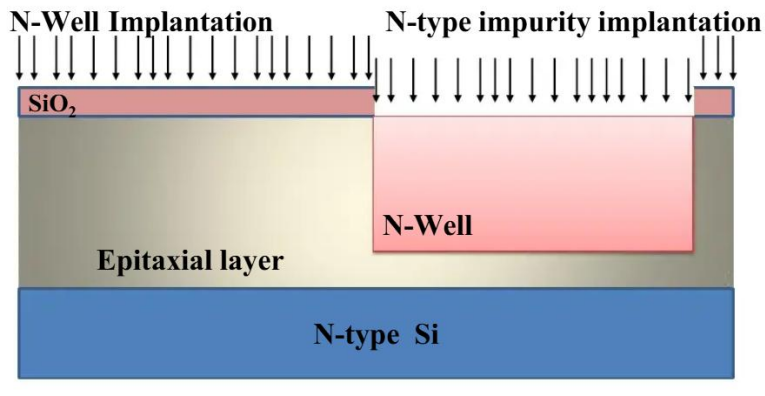


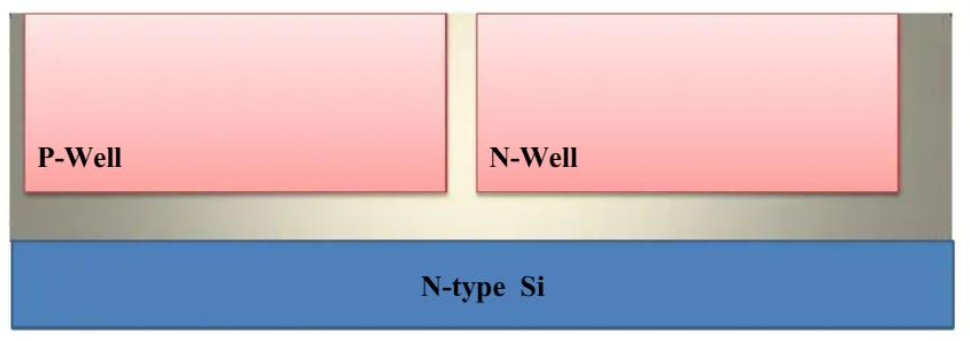
CMOS Fabrication Process

- **Twin-tub fabrication steps**



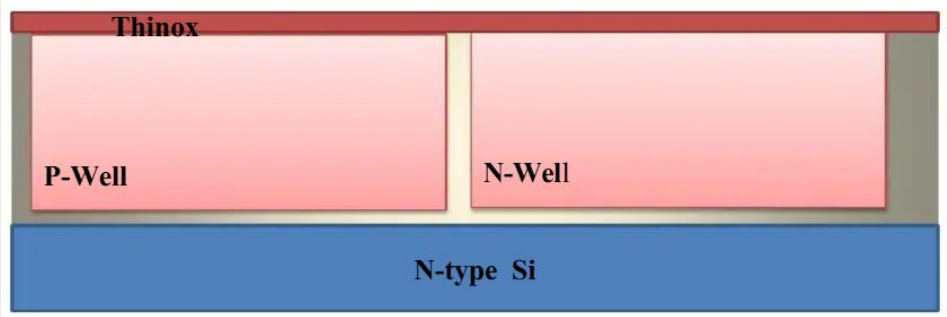


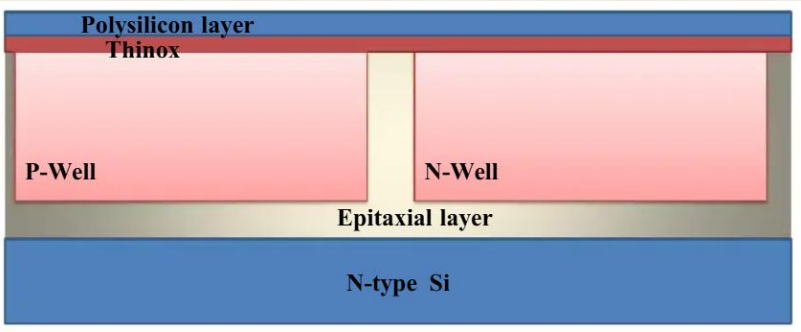


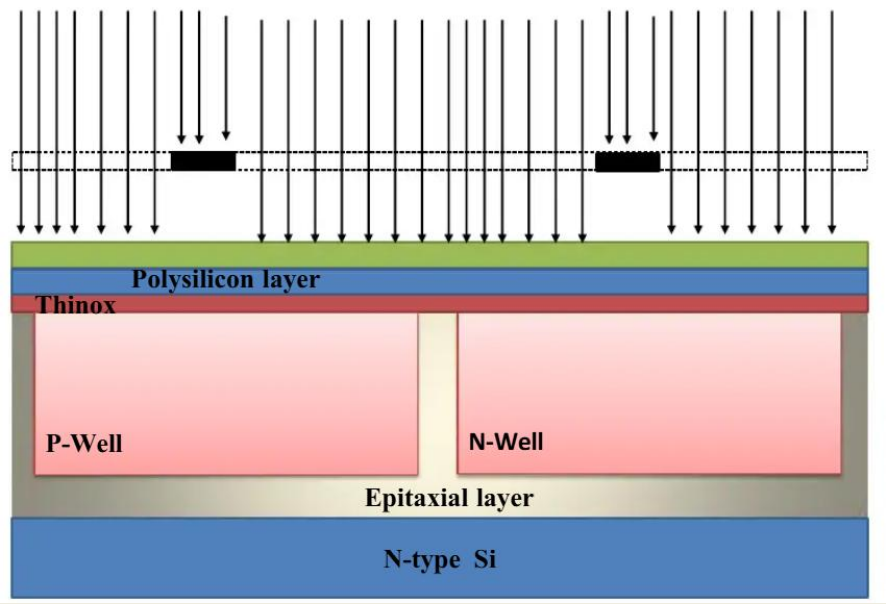


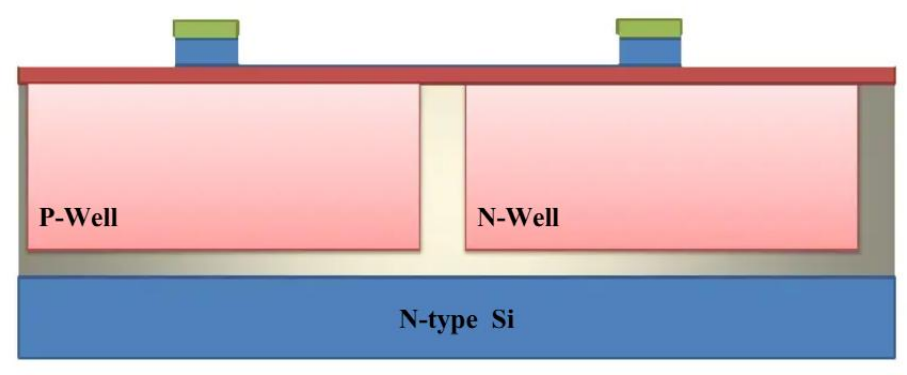
CMOS Fabrication Process

- **Twin-tub fabrication steps**



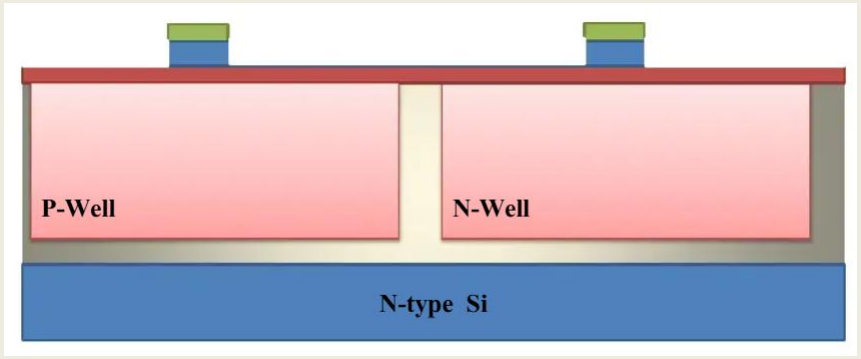


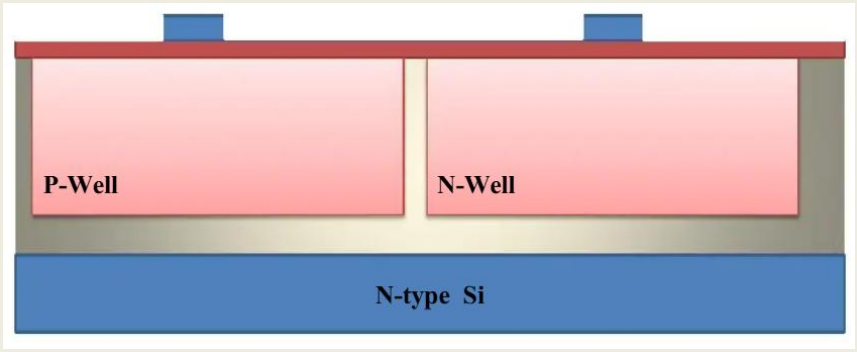


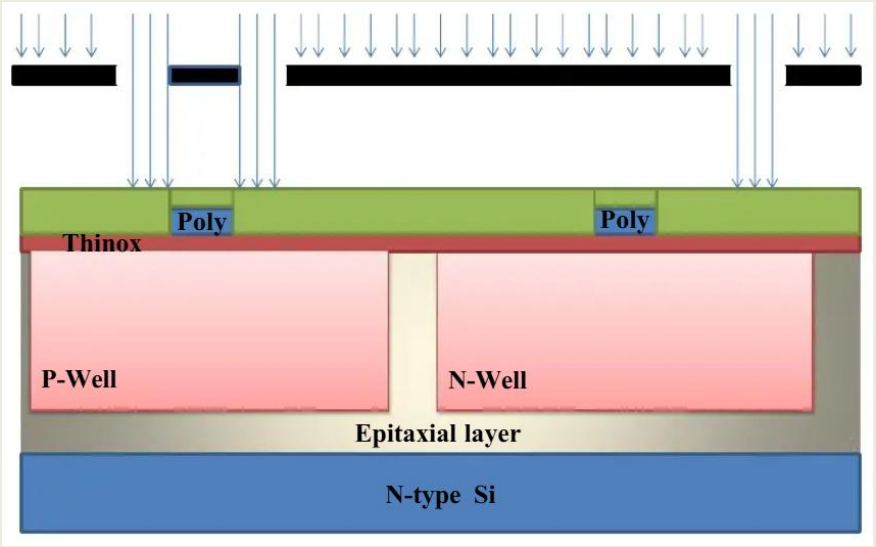


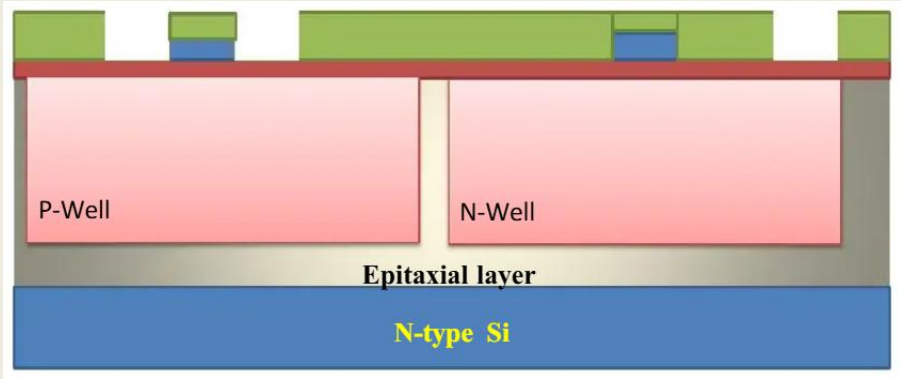
CMOS Fabrication Process

- **Twin-tub fabrication steps**



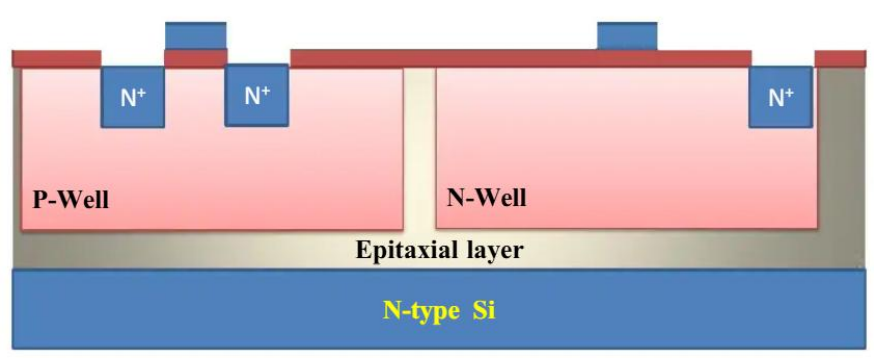


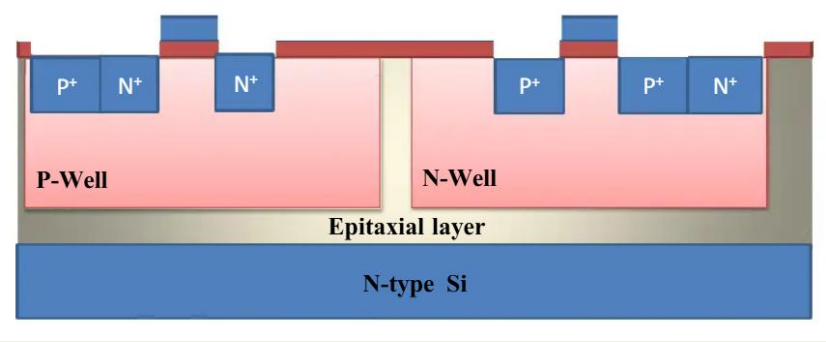


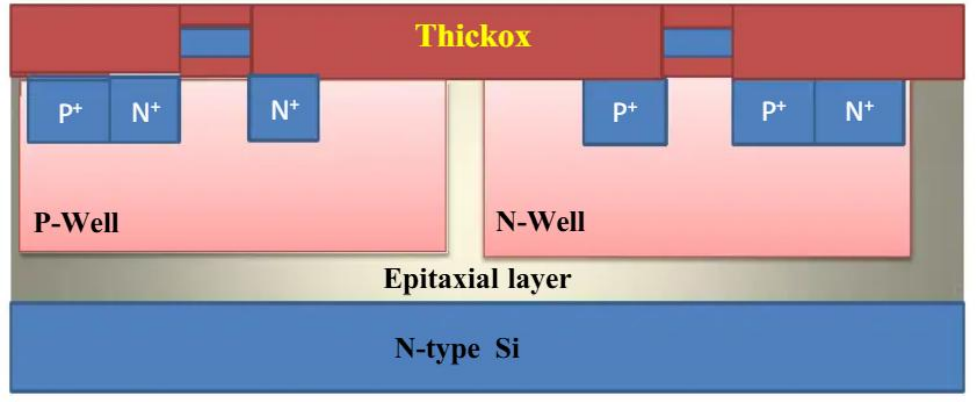


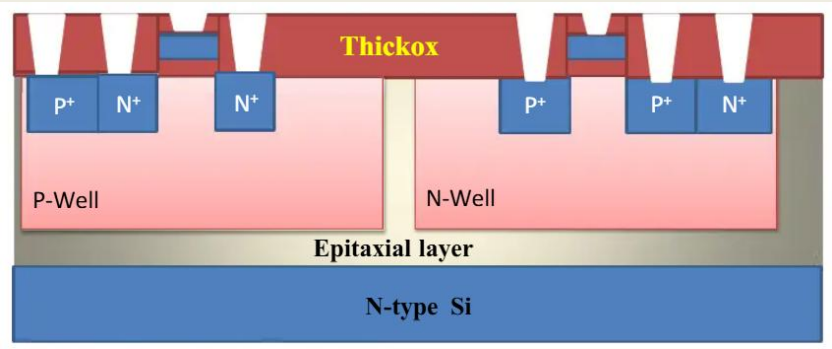
CMOS Fabrication Process

- **Twin-tub fabrication steps**



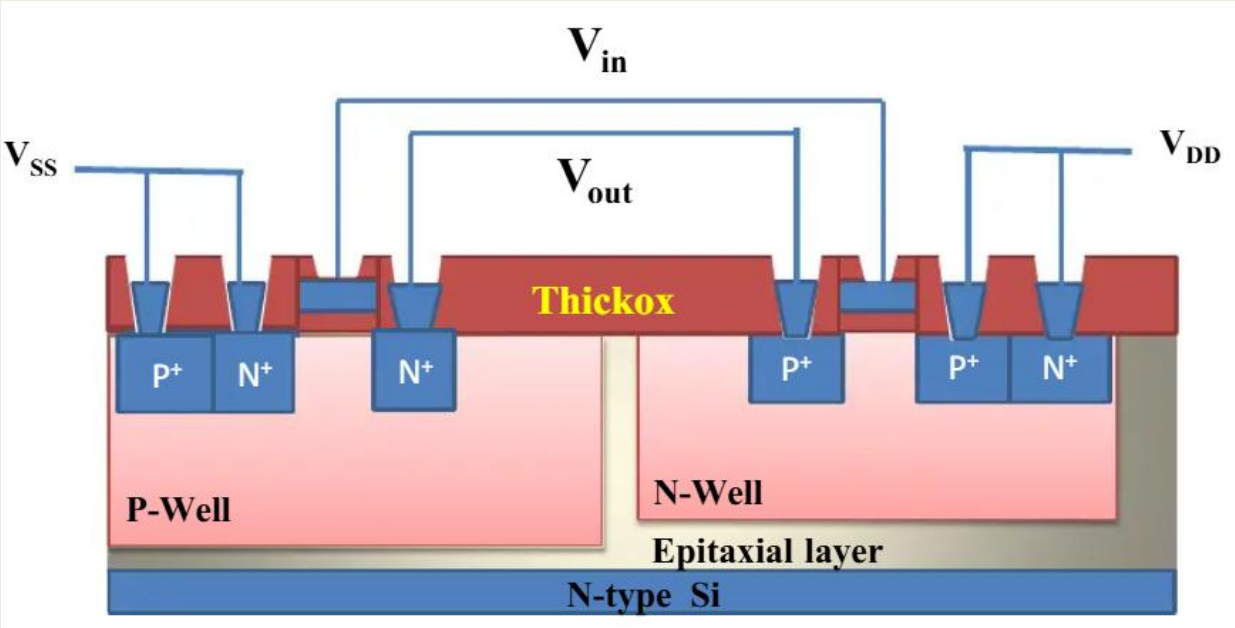


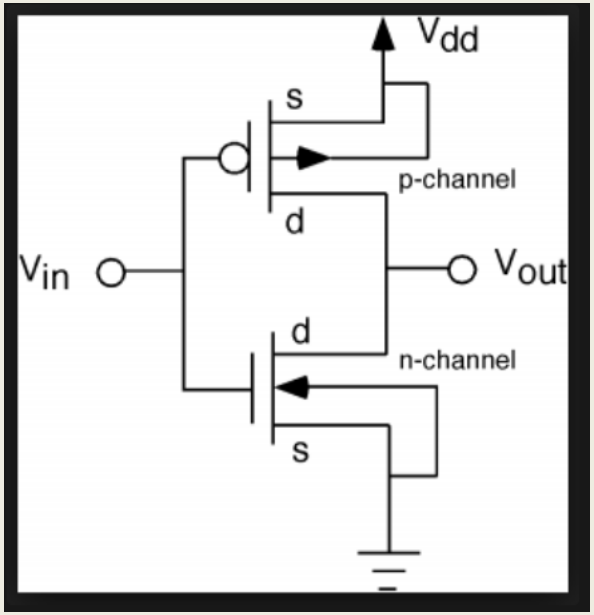




CMOS Fabrication Process

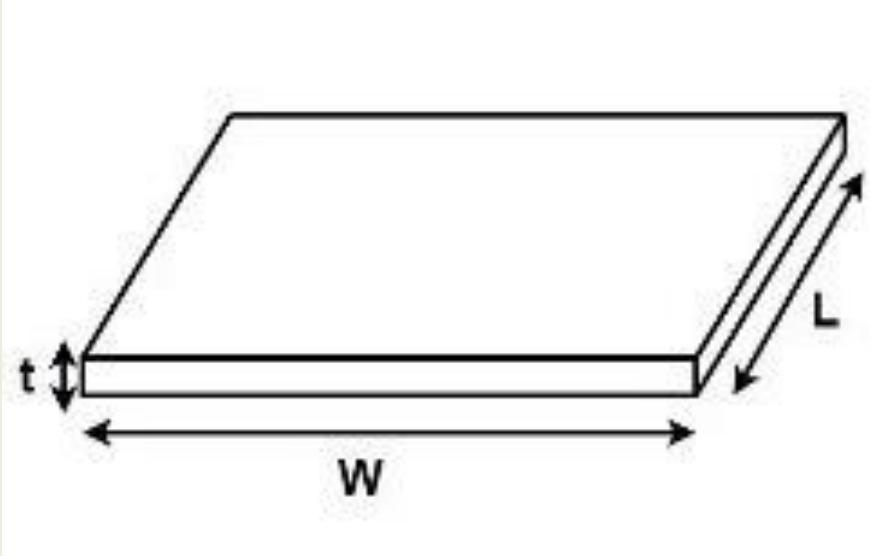
- **Twin-tub fabrication steps**





Resistor Fabrication Process

- The resistor is obtained in integrated circuit by utilizing the bulk resistance of a defined volume of semiconductor.



$$R_S = \frac{\rho L}{L.t} = \frac{\rho}{t} \text{ (ohms per square)}$$

Resistor Fabrication Process

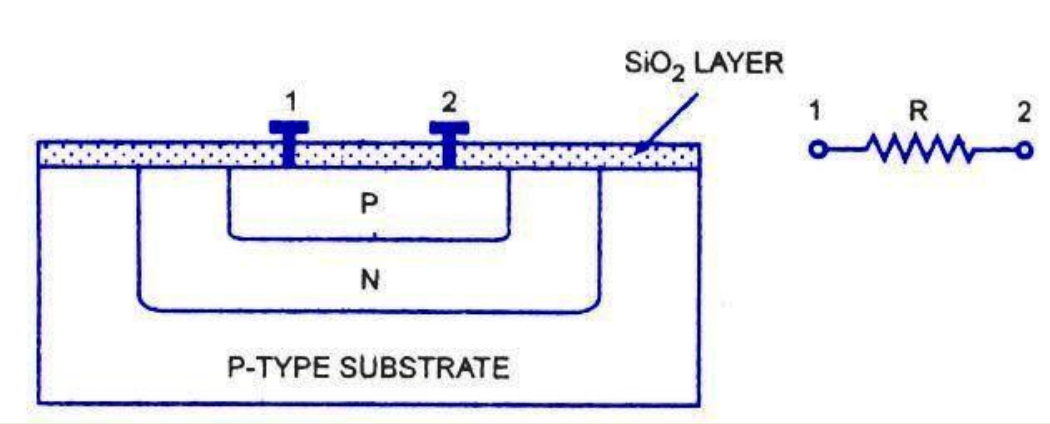
- Resistors are fabricated using different techniques for different applications. Most common types are

1. Diffused Resistors

➢ This type of resistor is fabricated by diffusion of p-type impurity in and n-type substrate.

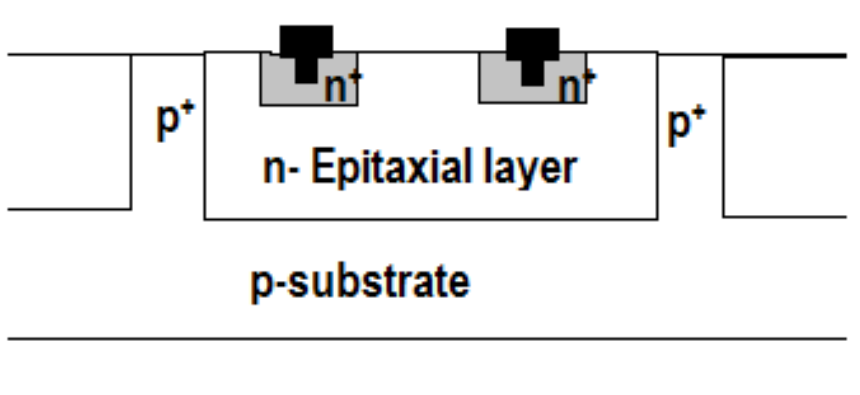
➢ The sheet resistance of diffusion resistor is 100-200 Ω/square.

➢ The sheet resistance is monitored during the diffusion process and can be designed to a tolerance of 5%.



Resistor Fabrication Process

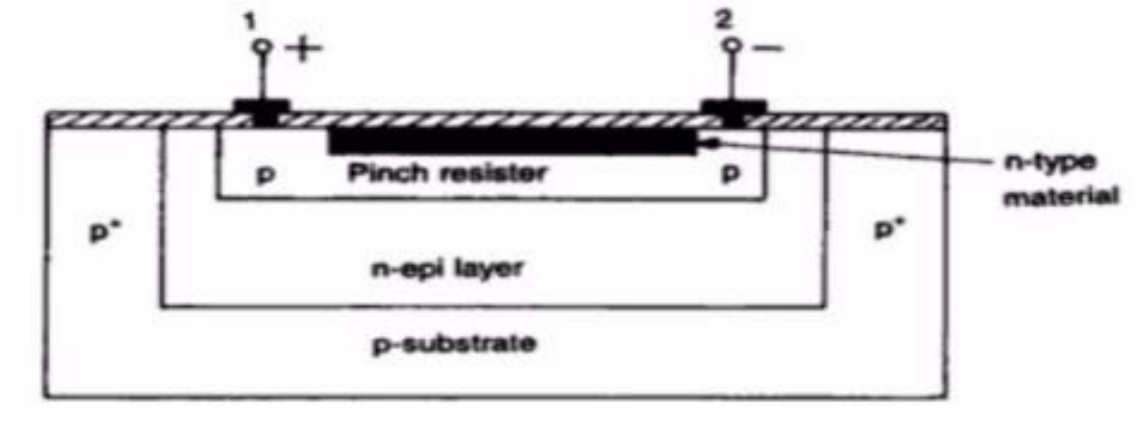
- **Epitaxial Resistor**



- Epitaxial layer is a thin layer of semiconductor material grown epitaxially over the substrate.
- Epitaxial resistor is used to achieve large value of resistance.
- Sheet resistance of epitaxial layer is 1-10 kΩ/sq.

Resistor Fabrication Process

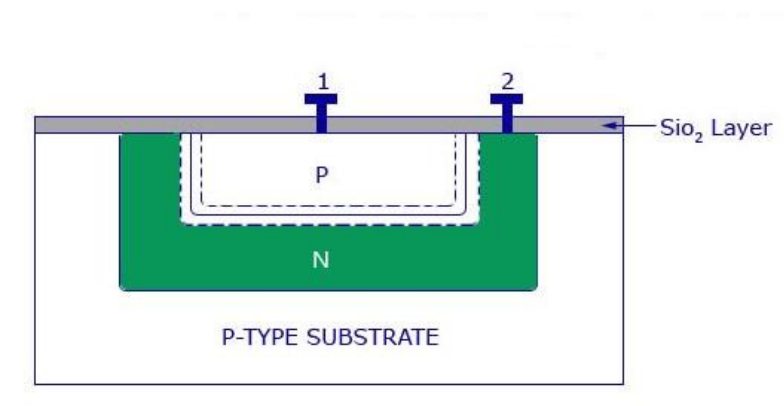
- **Pinched Resistor**

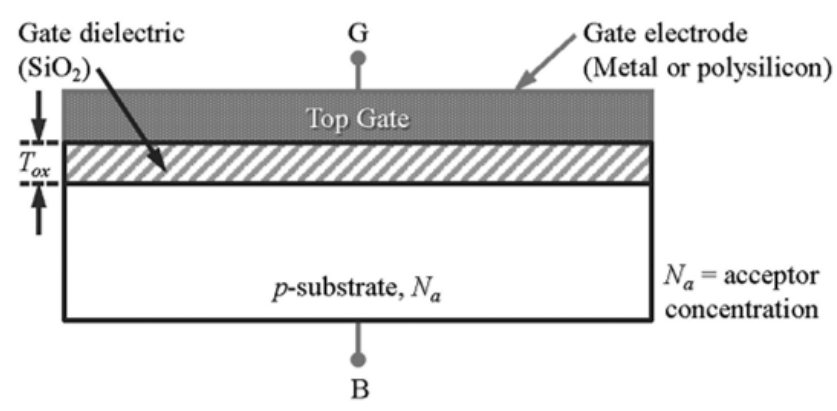


- It creates high sheet resistance by narrowing the cross-sectional area of a diffusion region.
- The sheet resistance of semiconductor is increased by reducing its effective cross sectional area (10-50kΩ/square).
- No current flow through the n-type material due to diode at terminal 2 in reverse direction.

Capacitor Fabrication Process

Capacitor fabrication





- There are different techniques to fabricate different types of capacitors. Most common types are

1. Diffused Junction capacitor
2. MOS capacitor

Capacitor Fabrication Process

Capacitor fabrication

1. Diffused Junction capacitor

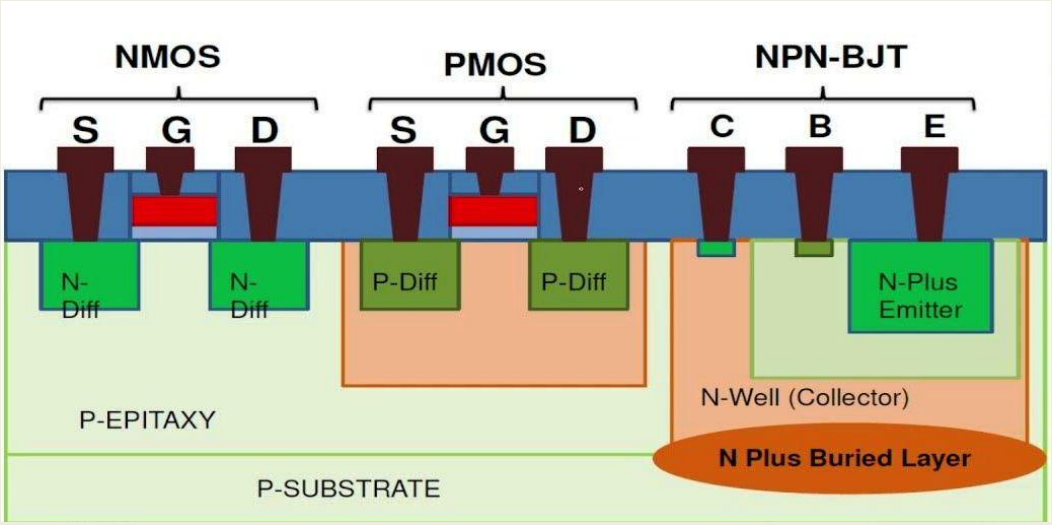
- A reverse-biased diffused p-n junction is used as capacitor.
- These capacitors are non linear.

2. MOS Capacitor

- MOS capacitor or oxide insulated capacitors are fabricated by using the emitter region as one plate, metallization as the second plate and intermediate oxide layer as dielectric.
- To obtain a higher capacitance per unit area, oxide thickness is kept between 500-1000 A^0.

BiCMOS Fabrication Process

- BiCMOS is a technique to combine the features of BJT and CMOS together.
- CMOS has advantage of small size, low power consumption and high noise immunity. However, its speed is limited due to its inability to drive high capacitive loads.
- On the other hand, BJT can operate faster than CMOS and have greater current drive capability.



BiCMOS Fabrication Process

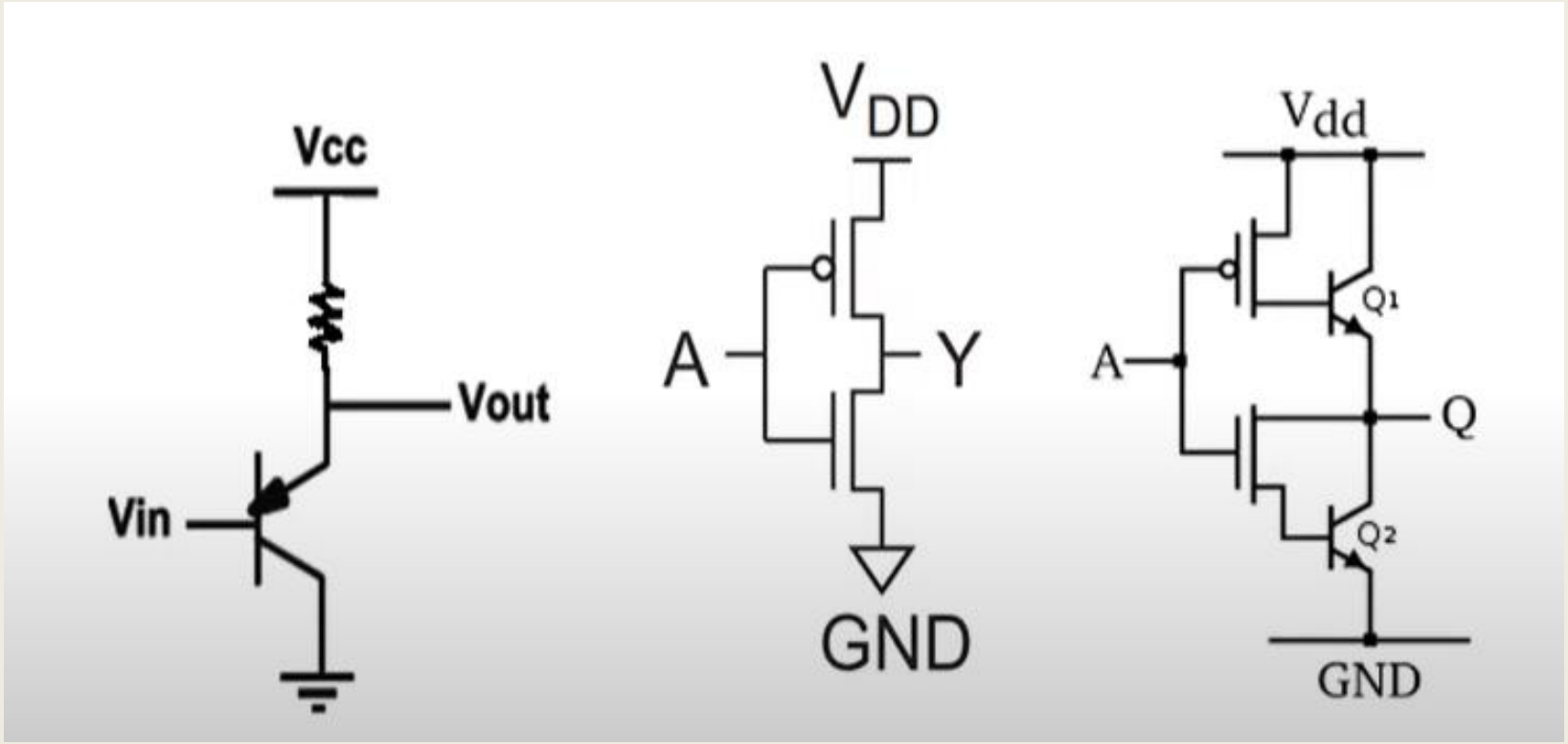
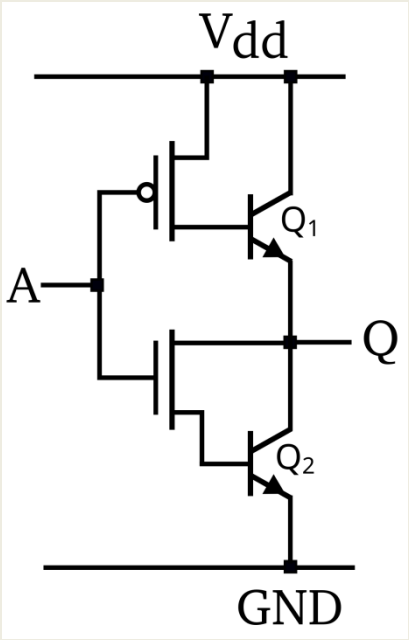


Fig. Inverter using BJT, CMOS and BiCMOS

BiCMOS Fabrication Process

- BiCMOS has the charging and discharging currents are $(\beta+1)I_D$, whereas it is I_D in CMOS inverter.
- The time required to charge and discharge will be less resulting into higher speed.

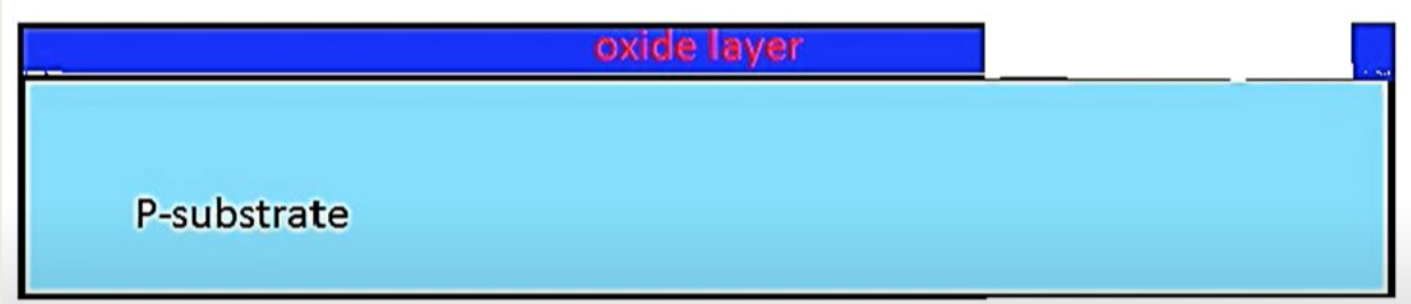


BiCMOS Fabrication Process

- BiCMOS fabrication has following steps:
- Step 1

- Step 2

- Step 3

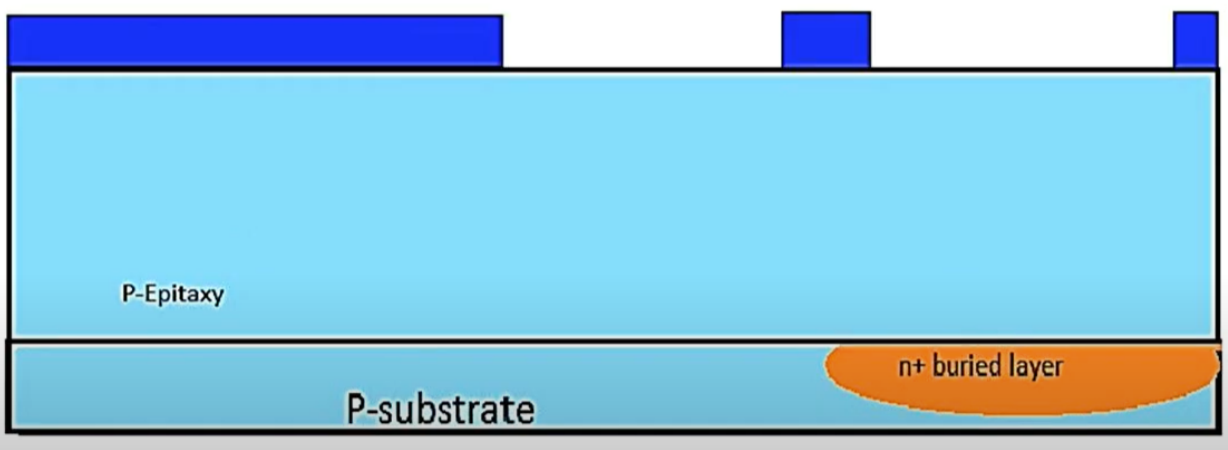


BiCMOS Fabrication Process

- Step 4

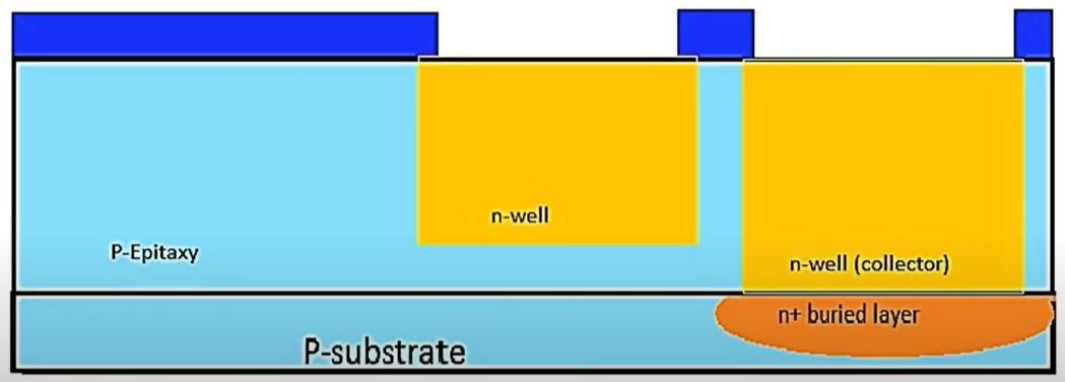
- Step 5

- Step 6

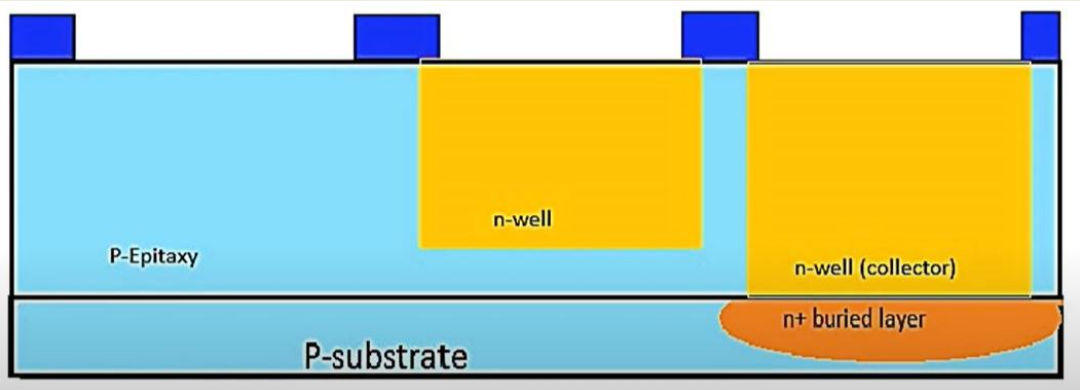


BiCMOS Fabrication Process

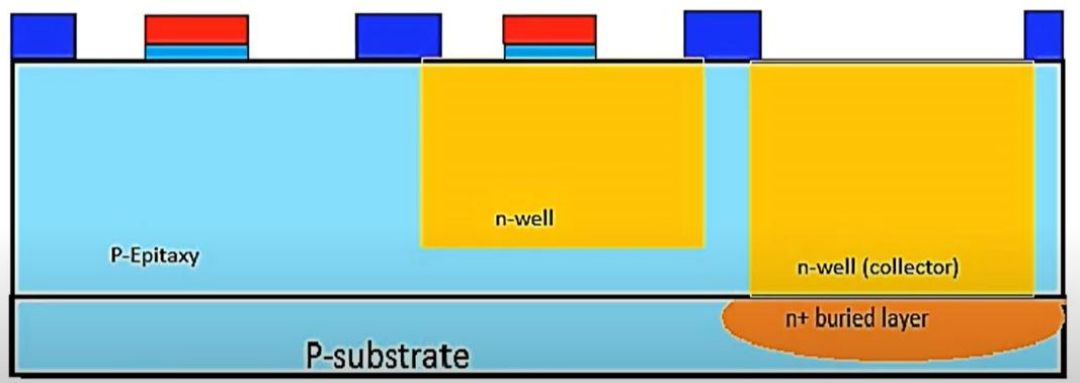
- Step 7



- Step 8

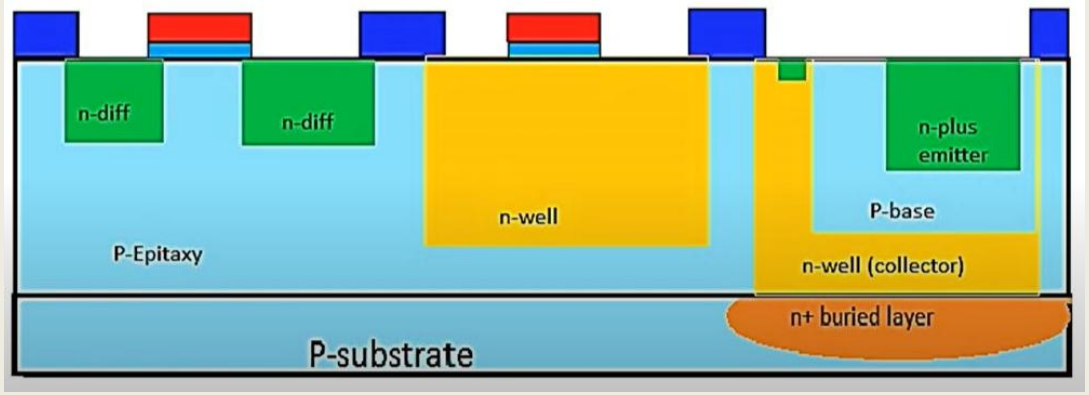


- Step 9

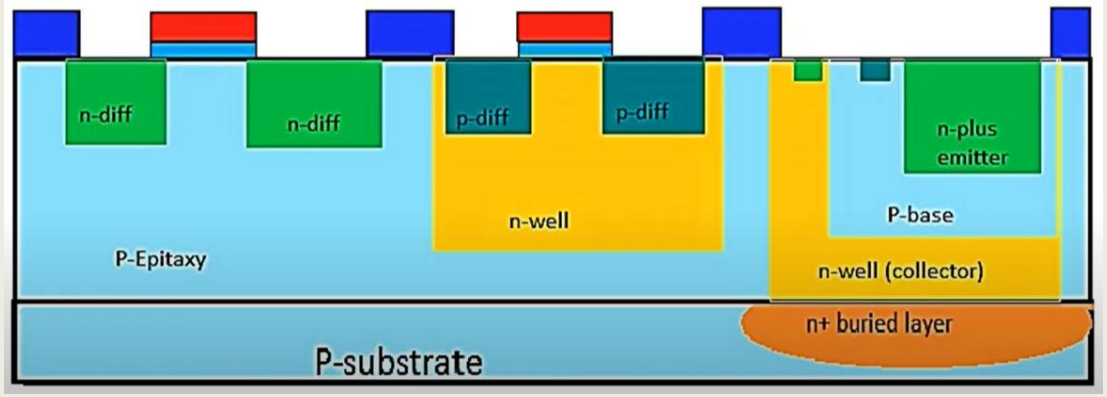


BiCMOS Fabrication Process

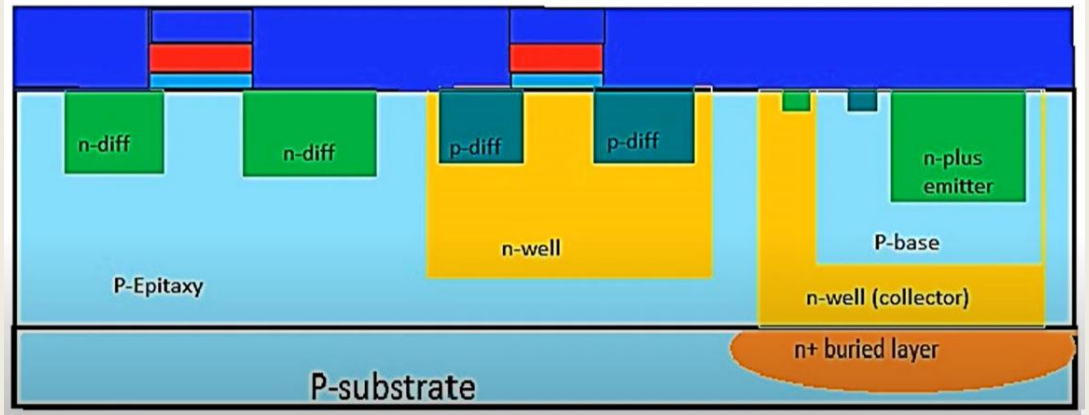
- Step 10



- Step 11

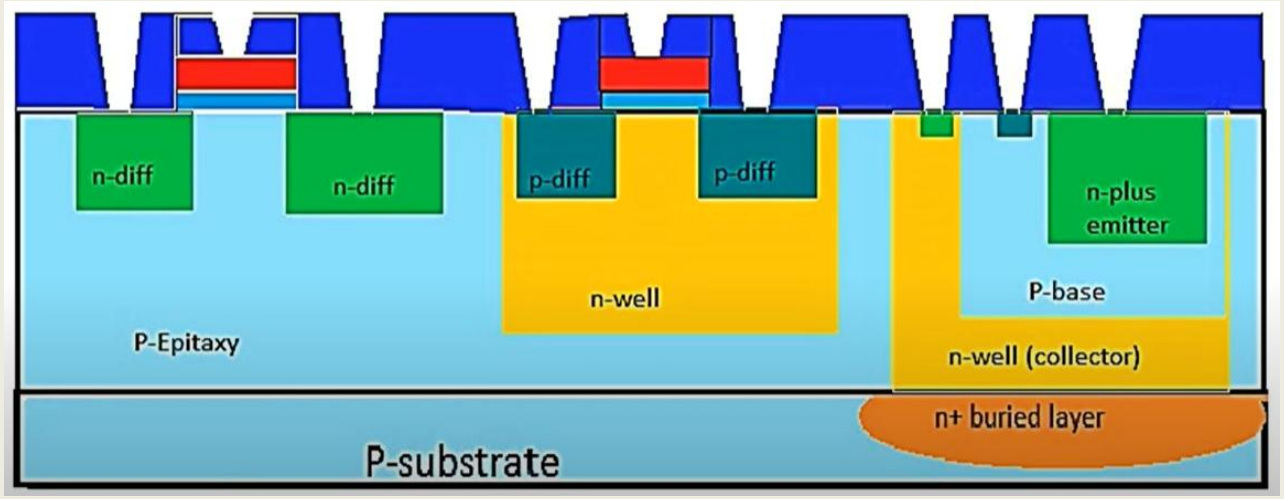


- Step 12

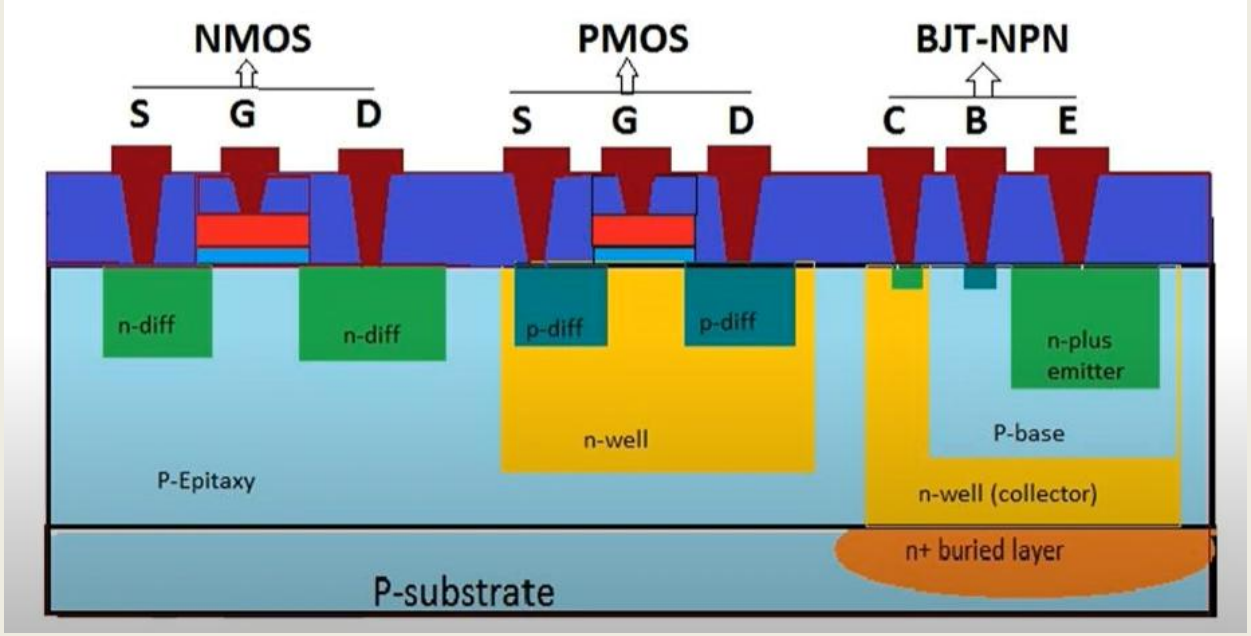


BiCMOS Fabrication Process

- Step 13



- Step 14




Thank You