General purpose band-gap reference with N-well resistors at VDD=3.3v, Vbgp=1.2v:Status

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***Abstract*— In this work update on the implementation of general purpose band-gap reference is provided. Author have implemented the band-gap reference circuit using SkyWater PDK. Different ways of implementations are depicted in the prior art. In this work an, all MOS transistor band-gap reference circuit is considered for implementation. Different analysis are done onto the circuit. Further work is to optimize the circuit to achieve the desired spces.**

***Keywords*— band-gap reference, PTAT, CTAT, start up circuit, trimming circuit**

I. INTRODUCTION

The BGR architecture without BJT and OP-AMP, proposed by Antonio as depicted in figure-1 is considered as base circuit. The sais circuit is reported on 180nm. Author is implementing the same circuit at 130nm Skywater PDK at 3.3V. In the circuit transistors M1, M2 M3 forms current mirror topology and M4-M8 maintains equality in node voltages. R1,R2 makes circuit invariant to temperature changes. Following equations governs the circuit operation

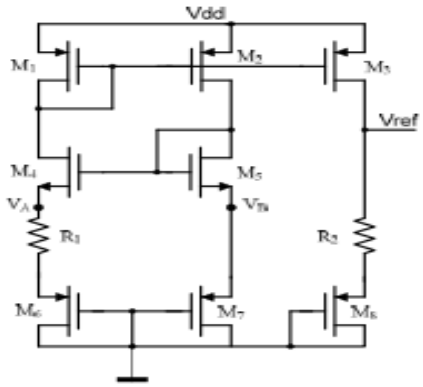

Fig. 1. BGR MOS based implementation[1]

$$V_{DD} = V_{DS_{M1}} + V_{SD_{M4}} + V_{R1} + V_{DS_{M6}}$$
$$V_{DD} = V_{DS_{M2}} + V_{DS_{M5}} + V_{DS_{M7}}$$
$$V_{DD} = V_{DS_{M3}} + V_{R2} + V_{DS_{M8}} \qquad V_{REF} = V_{GS_{M5}} + R_2 \cdot I \approx \frac{R_2}{R_1}$$
$$V_A = V_B \Leftrightarrow V_{R1} + V_{DS_{M6}} = V_{DS_{M7}}$$

III. IMPLEMENTATION RESULTS

The said circuit is simulated using NGSPICE with SkyWater sky130_fd_pr__pfet_g5v0d10v5 and sky130_fd_pr__res_generic_ndl tech node-cell[2-4]. The circuit is made to work on appx. 1.2V and different analysis like transient analysis, VDD sweep, TEMP sweep, VC variation, PPM variation are simulated [5-6]. The waveform of these are depicted from figure-2 to figure-5 as follows.

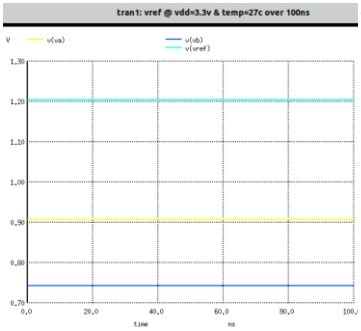

Fig. 2. Transient analysis of BGR

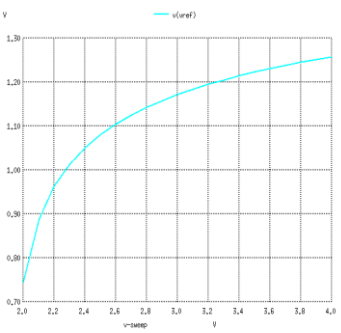

Fig. 3. Vdd sweep of BGR

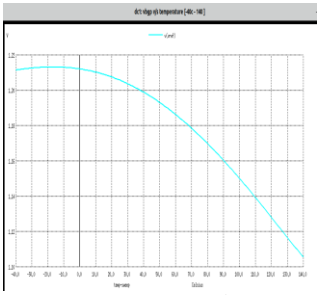

Fig. 4 Temp sweep of BGR

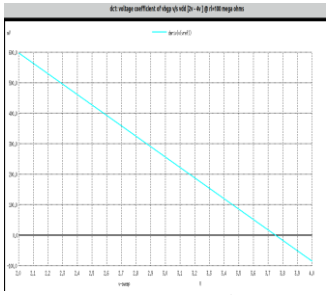

Fig. 5 VC variation of BGR

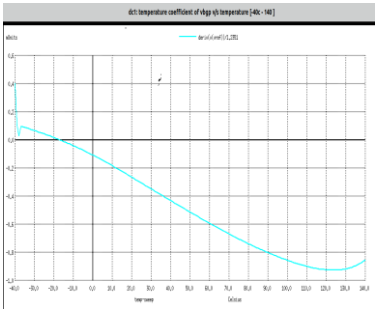

Fig. 4 PPM variation of BGR

IV. CONCLUSION AND FUTURE WORK

Author have simulated the said BGR circuit using Skywater PDK, sky130_fd_pr__pfet_g5v0d10v5 and sky130_fd_pr__res_generic_ndl tech node-cell using ngspice. Now author has to optimize the circuit performance to achieve the specs with the said tech-node.

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[6] https://github.com/ankursah5/avsdbgp_3v3