General purpose band-gap reference with N-well resistors at VDD=3.3v, Vbgp=1.2v

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***Abstract*— In this work an overview of theory pertaining to general purpose band-gap reference is provided. Different ways of implementations are depicted in the write-up. Further author propose to implement the band-gap reference circuit using SkyWater PDK. Author aims to propose a novel circuit implementation for the purpose with comprehensive analysis on impact of process, power supply, load, temperature variation on ac and dc accuracy. If resources permits author also plan to cover the package stress analyses as well. Author aims to design a circuit with high dc accuracy, with no or limited trimming tradeoffs primarily based on standard CMOS process.**

Keywords*— band-gap reference, PTAT, CTAT, start up circuit, trimming circuit

I. Introduction

Since 1960s band gap circuits are very critical component in almost all integrated circuits like DRAM's, flash memories, DACs and analog devices. The aim is to generate a stable voltage/current invariant of temperature, process variations. Companies like Analog Devices, Texas Instruments, Linear Technology, National Semiconductor, Maxim, STMicroelectronics, Faraday manufacture voltage references ICs.

We do not have any direct mechanism or quantity which does not vary with temperature and other obvious variations. For ease of understanding considering only temperature the variations are nullified by combining the effects on two opposite temperature coefficient. With the work of Hilbiber (1964) and Widlar (1965) of Fairchild proved the effectiveness of CTAT and PTAT phenomena which led to first band-gap circuit in 1971. One can understand a typical band-gap reference circuit principal with diagram shown in figure-1. As depicted in the figure-1 the V_{REF} is being generated in combination of V_{CTAT} and V_{PTAT}.

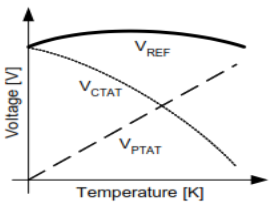

Fig. 1. V_{REF} generation with help of CTAT and PTAT

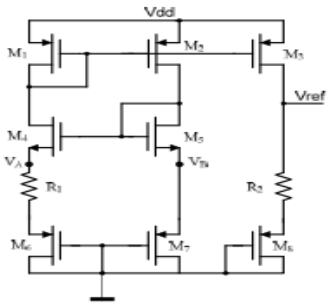

Fig. 2. BGR MOS based implementation

II. III. Different implementation approaches

The property of Zener diode to break at a known voltage when reverse bias can be exploited to implement a voltage reference circuits. These circuit can also be implemented by making use of V_{TH} of MOS, threshold voltage between enhancement transistor and depletion transistor also, along with the above discussed mechanism using CTAT and PTAT. Concept of sample-and-hold scheme with duty cycling is also proposed to implement BGRs in prior art. CMOS based BGR makes use of voltage referencing wrt well transistors. Pallavi et al proposed a curvature elimination with weighted subtraction of the outputs of two basic band gap circuits.

IV. BGR prior art circuit

A BGR architecture without BJT and OP-AMP, proposed by Antonio is depicted in figure-2. Transistors M1, M2 M3 forms current mirror topology and M4-M8 maintains equality in node voltages. R1,R2 makes circuit invariant to temperature changes. Following equations governs the circuit operation.

$$V_{DD} = V_{DS_{M1}} + V_{SD_{M4}} + V_{R1} + V_{DS_{M6}}$$
$$V_{DD} = V_{DS_{M2}} + V_{DS_{M5}} + V_{DS_{M7}}$$
$$V_{DD} = V_{DS_{M3}} + V_{R2} + V_{DS_{M8}}$$
$$V_A = V_B \Leftrightarrow V_{R1} + V_{DS_{M6}} = V_{DS_{M7}}$$

$$V_{REF} = V_{GS_{M8}} + R_2 \cdot I \approx \frac{R_2}{R_1}$$

V. Conclusion and Future work

Author studied the theory behind BGR and further studied different BGR implementation mechanism. As stated in abstract a novel BGR circuit needs to be implemented using SkyWater SKY130 PDK and open source tools like ngspice, magic etc.

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