

Lab Assignment 7

Title: Smart Brightness

Learning Objective:

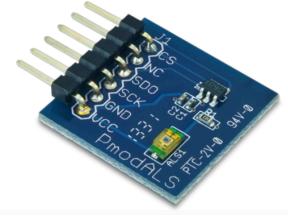
Learn how to control brightness of LED displays based on ambient light.

Specification:

Extend the circuit of Assignment 6 to control brightness of LED displays based on the intensity of the ambient light. Use light sensor module to sense the ambient light intensity.

Details:

This assignment extends the circuit of assignment 6 to have the LED brightness level derived from the ambient light intensity, instead of being specified by slide switches or up/down counter. There are several modules called Pmods (Peripheral Modules) that enhance the functionality of BASYS 3 boards. One such module, called PmodALS (Peripheral Module for Ambient Light Sensing) shown here is to be used for this assignment.



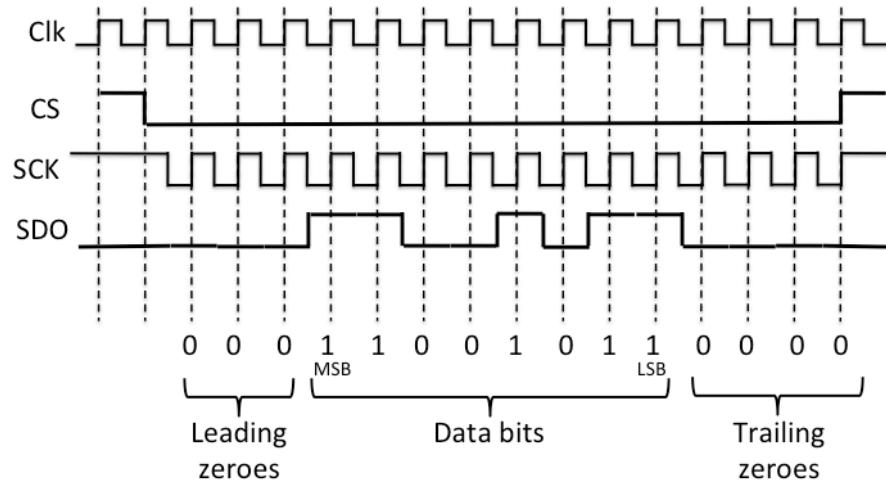
A BASYS 3 board has 3 Pmod ports and one XADC port (slide 13, Lec15). Each one of these has 12 pins as shown in slide 14, Lec15. Names of all the pins for various ports, as they appear in the constraint file Basys-3-Master.xdc are shown in slide 15, Lec15. Any of these 3 Pmod ports may be used to connect PmodALS. The following picture shows a PmodALS connected to port B of a BASYS 3 board.



PmodALS has a 6-pin connector. Therefore, both 12-pin cable as well as 6-pin cable are suitable for connecting the two. PmodALS pins connect to either upper half or the lower half of the BASYS 3 connector, that is, either JB1 to JB6 or JB7 to JB12, if B port is used. PmodALS follows SPI protocol as a slave to communicate with BASYS 3 as master. Pin names on the PmodALS connector are shown in the table below.

Pin	Signal	Description
1	CS	Chip Select
2	NC	Not Connected
3	SDO	Master-In-Slave_out
4	SCK	Serial Clock
5	GND	Power Supply Ground
6	VCC	Power Supply (3.3V/5V)

The protocol is shown in the figure below. SCK and CS are signals going from BASYS 3 to PmodALS and SDO is the signal going from PmodALS to BASYS 3.



PmodALS responds to the host board when CS is made low. It delivers a single reading in 15 SCLK clock cycles. Frequency of SCLK should be between 1 MHz and 4 MHz. Bits of data are placed on SDO by PmodALS on the falling edges of the SCLK and read by BASYS 3 on the subsequent rising edges of SCLK. Data consists of three leading zeroes, the eight bits of information with the MSB first, and four trailing zeroes.