Manoj Kumar
Third Year Undergraduate
Computer Science and Engineering Department
Indian Institute of Technology, Delhi

manoj.kumar.cs518@cse.iitd.ac.in
https://manoj2601.github.io
(+91) 9509196171
manoj2601

Education

year	Degree	Institute	%age or CGPA
- - - -	(Dual) B.Tech+M.Tech	Indian Institute of Technology, Delhi	8.042
2017	Class 12th	Navjeevan Public School, Sikar	98.20
2015	Class 10th	ABN Sr. sec. school, Maulasar(Raj)	93.50

Scholastic Achievements

2018 **Joint Entrance Examination(Advanced)** AIR 119(OB) among more than 1,500,000 students
2018 **Joint Entrance Examination(Mains)** AIR 405(OB) among more than 1,500,000 students
2017 Awarded with **silver medal** by Education Minister of Rajasthan for performing exceptionally well in class XII
2017 Secured **3rd merit** in Class XII(RBSE board) among more than **2,000,00** students who appeared in the exam
2020 Certified in Data Structures and Algorithms Program **(CCDSAP) by Codechef**

Engineering Courses

Computer Science	**Machine Learning*, Analysis and Design of Algorithms*, Principles of Artificial Intelligence*, Computer Networks***, Programming Languages, Discrete Mathematical Structures, **Data Structure and Algorithms, Computer Architecture**, Digital Logic and Systems, Design Practices
Mathematics	**Probability theory and Stochastic Process**, Linear Algebra and Differential Equations, Calculus
Electrical	Signals and Systems, Principle of Electronic Materials, Introduction to Electrical Engineering
Online Courses	Graph Search, Shortest Paths, and Data Structures; Machine Learning*

*courses currently pursuing

Major Projects

K-MEDIAN IN A DIRECTED TREE

Prof. Smruti Ranjan Sarangi, IIT Delhi

ALGORITHMS, C++ *February 2020 - April 2020*

- Module programmed in C++ that computes **k-medians** in a directed tree (edges directed from child to parent) in $O(Pk^2)$ complexity.
- The project aims to find the **optimal placement of *cache proxies*** in a computer network maintaining **minimum overall cost**.
- Implemented in 2 phases and each phase uses a space of **O(nk)** complexity (better than already established $O(n^2k)$ complexity).
- Method employs **dynamic programming** for efficiency whereas best known algorithm for undirected tree is **NP-hard**.

**k is the number of resources(proxies) to be placed ,'P' is the path length of tree & 'n' is number of vertices/nodes in tree.*

SOFTWARE COMPARISON

Prof. Smruti Ranjan Sarangi, IIT Delhi

SOFTWARE ENGINEERING *December 2019 - January 2020*

- Comparison of softwares used as *web browsers, pdf readers, music players, mail clients* etc. based on with similar functionalities.
- Analyzing the reasons for the **less efficiency of a feature** of one software as compared to other softwares with same functionality.
- Debugging the software features of **statically linked, non-stripped** version of the software using **Flamegraph**.
- Replacement of **less efficient** feature of one software with a **well efficient** corresponding feature in other software of same class.

MIPS ARCHITECTURE PROCESSOR

Prof. Preeti Ranjan Panda, IIT Delhi

COMPUTER ARCHITECTURE, VHDL, C++ *January 2020 - July 2020*

- Module consists the VHDL implementation of a **multi-cycle MIPS architecture processor** on FPGA and **pipelined simulation** of the processor with *Variable delays* and *single-layer Cache memory* in C++.
- **BlockRAM Memory Generation** is used to store the data as well as machine code and initialize the machine code using the ***coe* file**.
- Demonstrated on FPGA which contains the different components **ALU, Register File** and **Memory** and executes a large subset of the MIPS instructions. A *state machine* is used to implement the control of the processor.
- Implemented a **5-stage pipelined MIPS** C++ simulation by removing data hazards by avoiding stalls via **forwarding or bypassing**.
- Analyzed the efficiency of the processor by varying *HIT and MISS* probabilities; and **variable delays** after each memory access.

ENCRYPTED VOTING PROTOCOL
Prof. Subodh Sharma, IIT Delhi

MODERN CRYPTOGRAPHY — *August 2020 -present*

- An individually verifiable voting protocol with complete recorded-as-intended and counted-as-recorded guarantees.
- Protocol does rely on several **cryptographic** constructs to establish its correctness and maintain indiv. & community **vote secrecy**.
- Software independent and bare-handed. Uses random distribution of pre-printed ballots with optional **cast-or-audit** component.
- The protocol optionally supports **voter verifiable paper audit trails(VVPAT).**

ProLog and Toy OCaml Interpreter
Prof. Sanjiva Prasad, HOD (IIT Delhi)

PROGRAMMING LANGUAGES, OCAML — *February 2020 - March 2020*

- Module programmed and implemented in OCaml using **OCamllex** and **OCamlyacc** for reading and parsing the inputs respectively.
- Basic functionalities of **ProLog** implemented using the techniques of **back-tracking, rule unification** for the resolution of queries.
- **SECD, Krivine machine** is used to implement Ocaml functionalities.

3D Structures using Graphs
Prof. Subodh Kumar, IIT Delhi

DATA STRUCTURES AND ALGORITHMS, JAVA — *November 2019 - December 2019*

- **Graph data structure** implemented by storing vertices and edges of a triangle in nodes to created 3D structures by linking triangles.
- Queries handled such as insert, neighbors, **topological distance**, centroid, **connected components**, **diameter** of the shape etc.
- **Djikstra Algorithm** is implemented to find the minimum distance between two connected triangle nodes.

Multi-threaded Producer Consumer Platform
Prof. Subodh Kumar, IIT Delhi

DATA STRUCTURES AND ALGORITHMS, JAVA — *September 2019 - October 2019*

- Module programmed in Java for multiple buyers and sellers to purchase and sell items using **thread synchronization** and **locks**
- Maintained inventory and catalogue which sells product of the **most preferred seller** by maintaining priorities of each seller.
- Solved the problem of multiple threads to remain **synchronized** and sell the products from catalogue maintaining **thread safety**.

UART Implementation on FPGA
Prof. Anshul Kumar, IIT Delhi

DIGITAL LOGIC & SYSTEM DESIGN, VHDL — *October 2019 - November 2019*

- The **Universal Asynchronous Receiver -Transmitter** (UART) implemented in VHDL for asynchronous serial communication that takes in **serial data** at given **baud rate** with a higher frequency of receiver to check discrepancies and converts it to **parallel 8-bits** for storage, which is then fed to the transmitter that generates serial data output.
- Implemented a **memory** of size **256 bytes** to store bytes (8 parallel bits) and by a single push signal, transmitter transfers the byte to the computer serially. **GTK terminal** is used for communication.

Technical Skills

Programming Skills	Proficient in **C/C++, JAVA,** Python, OCaml, MATLAB, Prolog, LaTeX, javascript
Softwares	Android Studio, Visual Studio, Git
Hardwares	Xilinx ISE Design Suite and Vivado (VHDL and Verilog), MIPS assembly
Web Development	HTML, CSS, JavaScript(Basic)

Extracurricular Activities

Representative, Indoor Sports Club (ISC), IIT Delhi
April 2019 - March 2020

- Responsible for **administering all hostel affairs** related to *Chess, Carrom and Snooker Pool* in allotted hostel budget.
- Guided participants to **secure Silver** in Chess & Snooker Pool clinching **Prestigious ISC Trophy among 13 hostels.**
- Managed and executed various competitions- Inter-hostel and Inter-IIT Open Trials to increase Indoor Sports culture.

Volunteer, National Service Scheme (NSS), IIT Delhi
September 2018 - PRESENT

- Regular volunteer in NSS, IIT Delhi, that consists the work on a diverse range of **social issues** through various **events** and **projects** which are aimed towards the benefit of people in and around IIT Delhi.
- Selected as Best Volunteer in **APNA PARIVAAR** project that aims to provide opportunities to **orphan kids** to gain confidence and develop their personality. It also consists of organizing **educational trips**, doubt clearing and teaching sessions.
- Volunteered in project **BACHPAN** that aims at improving the quality of life of the **less fortunate children** by providing them **education** and healthy childhood in and around IIT campus which include children of the construction site workers inside the campus.

Academic Mentorship, Board of Student Wellfair, IIT Delhi
July 2019 - December 2019

- Selected for **Academic Mentor** of MCP100 (Engg. Visualization & Comm.) for one semester on the basis of academic performance.
- Guided First year students by organizing doubt clearing meetings and **tutorial solving sessions** to prepare them for the exams.

- During COVID19 lockdown, conducted a **survey** in all over India to assess **in-home** and **out-of-home discretionary activity engagement**. Built a **static website** to collect responses and analyzed the data. — *April 2020 - June 2020*
- Worked as **Marketing Team Head** in *the biggest cultural fest of north India, **Rendezvous, IIT Delhi*** — *July 2019 - October 2019*
- Worked on the position of **Events Team Head** in ***Tryst***, annual technical fest of IIT Delhi — *February 2019 - March 2019*
- **Intellify:** Developed problem solving video content for unprivileged students of Delhi govt. schools. — *May 2020 - June 2020*
- Technical Content Writer at **GeeksforGeeks**. — *May 2020 - PRESENT*
- Worked for the post of Content Developer Expert (Mathematics) intern at **Doubtnut**. — *May 2020 - June 2020*
- **Common Room Committee** member, Girnar House, IIT Delhi. — *May 2029 - April, 2020*
- **Hobbies:** Competitive Coding, blog writing, indoor games