

# Simple and Complex Circuit Simulation Demonstrations



Simulations to demonstrate knowledge and ability in electronics design and development. The circuits were relevant to problems I encountered with my projects.

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Page Modified: 2014-02-14

Page Created : 2013-03-25

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## Simulated Circuit Demonstrations

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## Simple Circuits

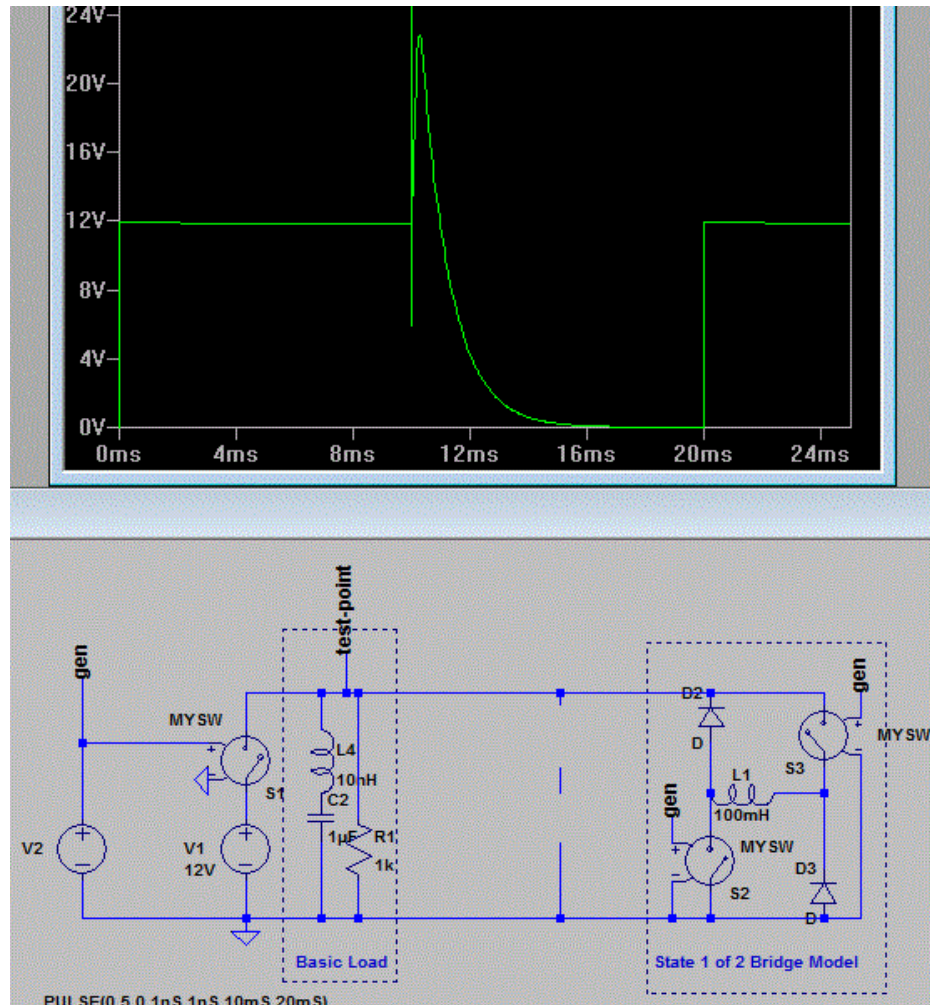
### Load Dump Protection from a Bridged Inductive Load

Say you have 2 loads on the same power supply. One basic resistive load and the other an inductive load. When the power is cut the inductive load releases its stored energy. This can be bad if the energy dumps into the basic load causing overvoltage or reverse voltage. Take the more complicated case where the inductive load is driven by a full bridge driver. There's 2 possibilities for the inductive load to dump into the basic load. It can dump negatively or positively. Say one disrespects the internal circuitry of the bridge driver and only considers the worst possible effects on the basic load.

Notice the positive spike.

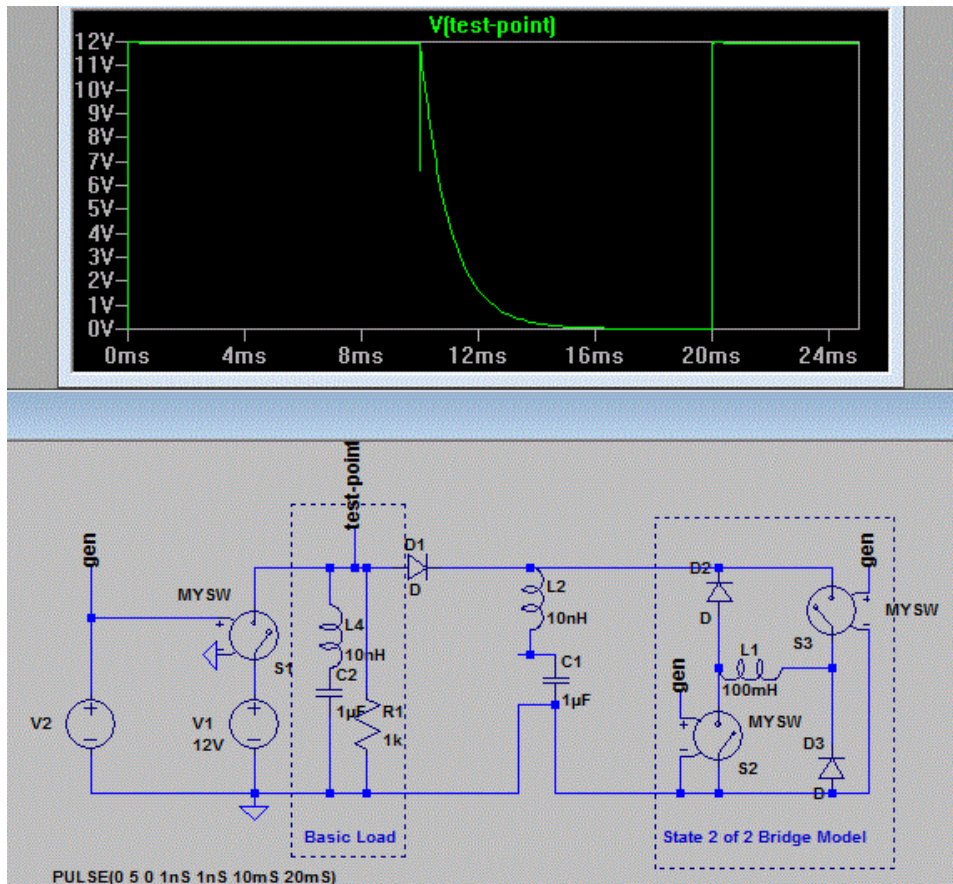
→Cuk Converter  
Radiated EMI

→Resonant Capacitor  
Swapping



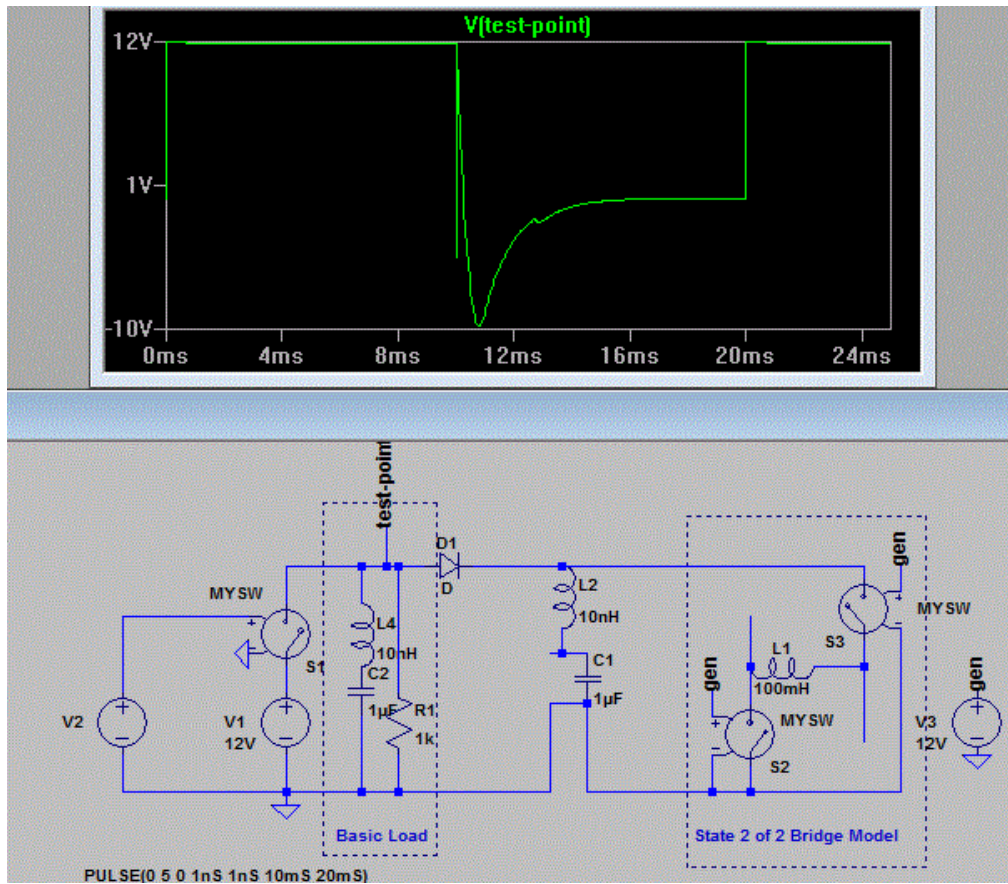
If the bridge driver powers down as modeled in the schematic above, the basic load gets overvolted as seen by the waveform on "test-point".

To protect the basic load from overvoltage, a blocking diode and capacitor are added to the circuit. The inductor dumps into the capacitor.



That takes care of the case where the bridge driver powers down that way. But what if the bridge driver powers down the other way?

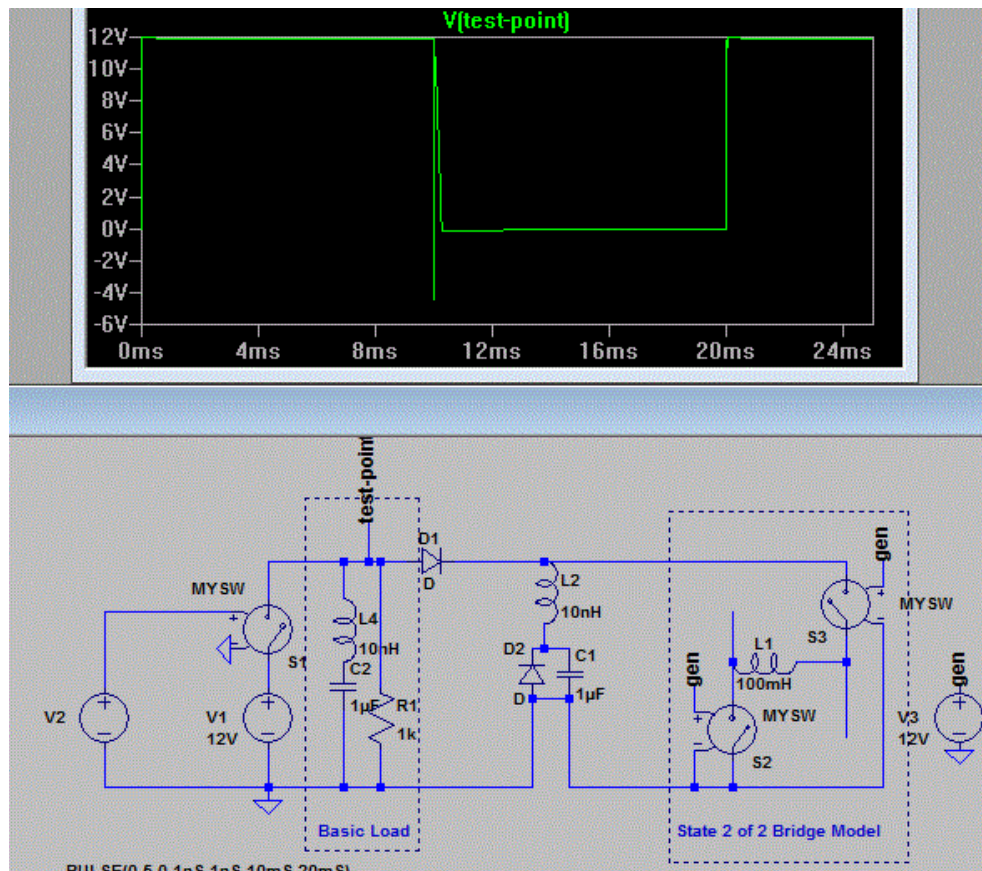
Notice the negative spike.



Ouch! Say that basic load is not allowed to go negative.

The fix is to add a flyback diode.

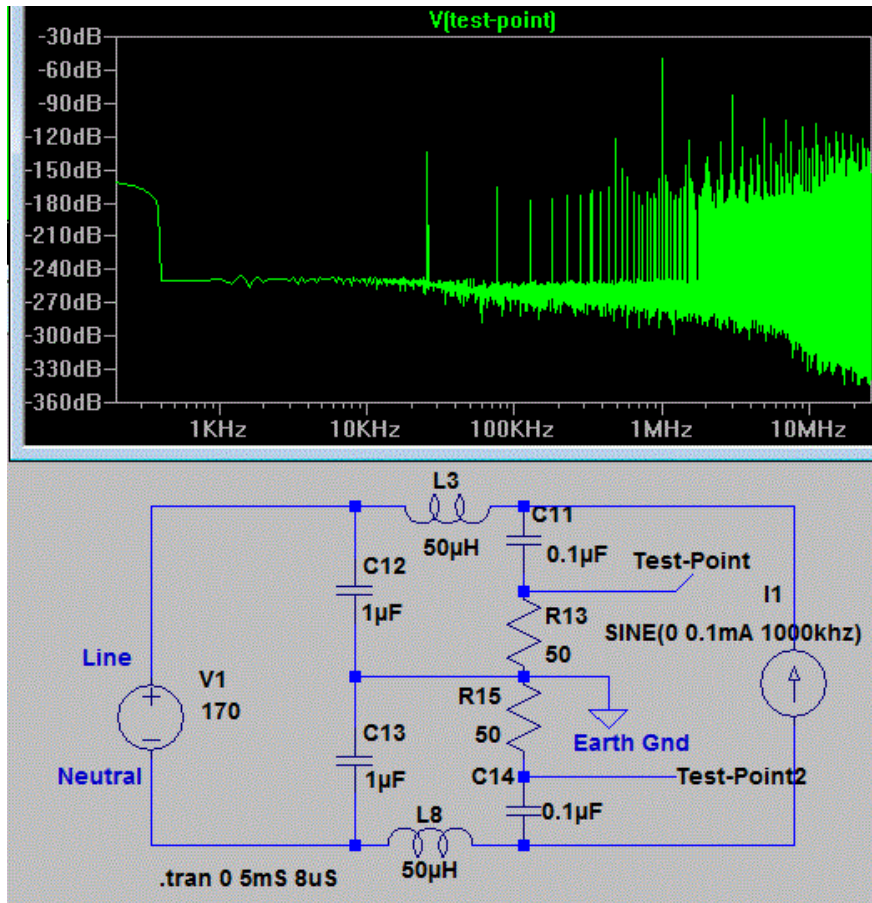




Done. Never mind that glitch between 8mS and 12mS lol.

### Simulation of Conducted EMI with a Line Impedance Stabilization Network

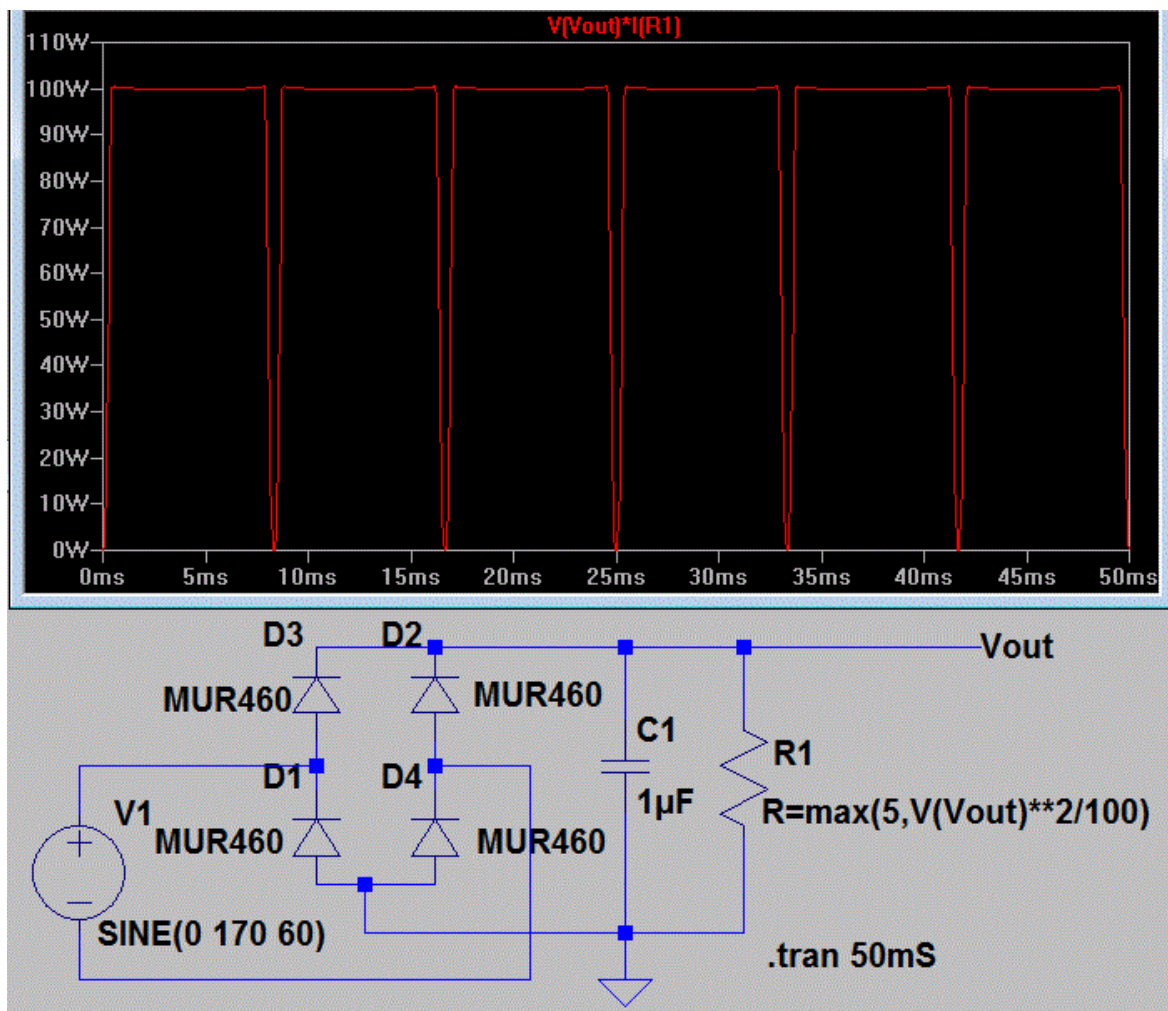
One of many specs to meet compliance is FCC Sec. 15.107 where in the 0.5Mhz - 5Mhz range the quasi peak is 56dBuV and the average 46dBuV.  $\text{dBuV} = 20\log_{10}(\mu\text{V}/1\mu\text{V})$



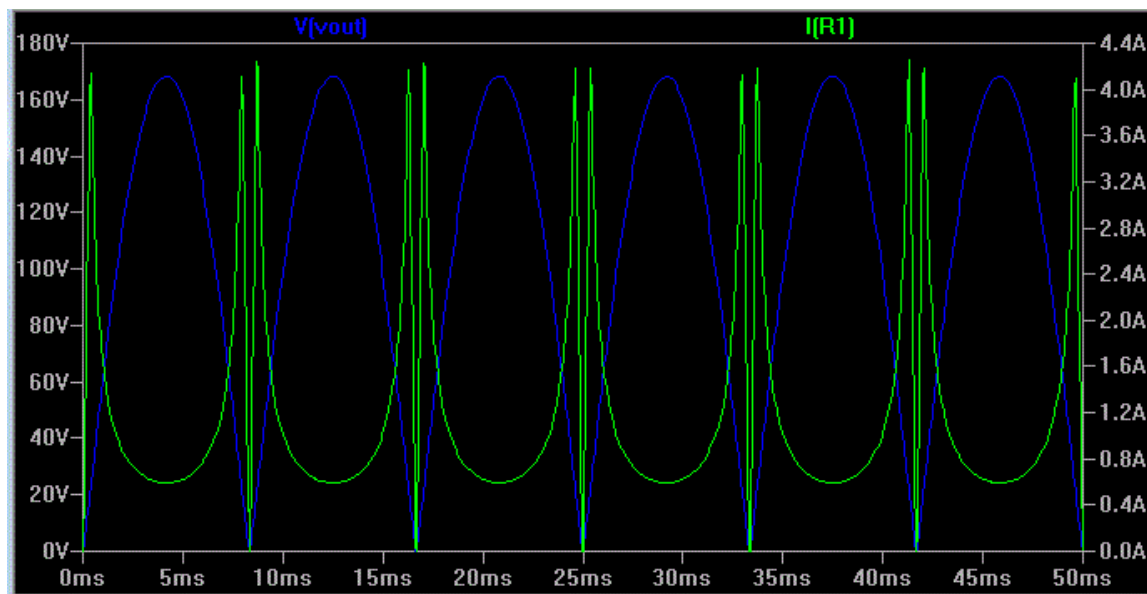
V1 can be DC to 60Hz. The test noise load is a 100uA 1Mhz sine current. The largest peak is -46dBV(74dbuV) at the expected 1Mhz. The differential current is over the EMI limit for FCC section 15 for Class B devices. Another way to get an FCC fail is with excessive common mode currents.

### Constant Power Load

It won't simulate if R1 is simply set to  $V_{out}^2/P$ . Starting at  $V_{out} = 0$  means starting  $R1 = 0$  resistance. But starting at 0 resistance makes it impossible for there to be any voltage change to change R1. Nothing makes nothing. The simulation jams at 0. And so, if it could, the diodes would explode as circuit currents aim for infinity. One correction is to use the LTSpice max function to keep R1 off 0. R1min is set to 5 ohms in the circuit below.



Load dissipates 100Watt up to a current limit after which the load turns resistive.



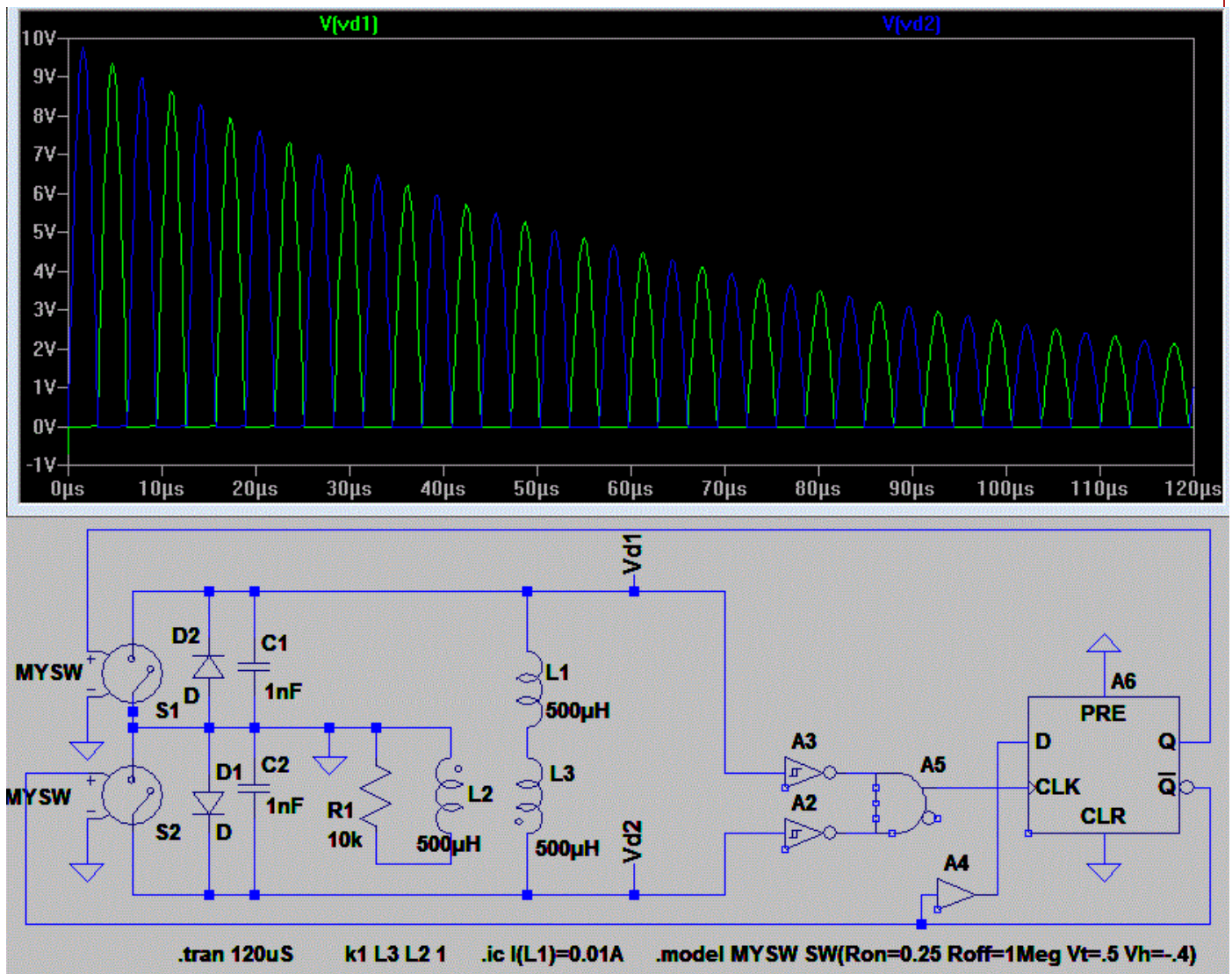
The load has 2 states. Constant power and resistive. Once voltage drops to certain point the loads switches from constant power to resistive.

## Complex Circuit Demonstrations



## Resonant Capacitor Swapping

I created this circuit to gain insight on using mosfet parasitic capacitances in a resonant power supply. C1 and C2 take turns being the resonant capacitor in the tank. The tank was energized by an initial current in L1. The tank decays due to energy lost by the load model composed of R1, L2 and L3.



A4 is a delay line to get T flip flop function from a D flip flop. LTSpice doesn't have a T flip flop model.

## Cuk Converter Radiated EMI

Aside from all the hard switching harmonics there can be 2 other frequencies of significance as a result of parasitic inductance L2. L2 is the sum of conductor inductance and loop inductance. Loop inductance depends on the diameter of the arrangement of components M1, C1 and D1. 340Mhz and 190Mhz ringing occurs on the switching frequency in the circuit below. C2 is a hypothetical interwinding capacitance on L5.



