HyperLynx® 3D EM Designer

Quick Start Guide for Stacked Die Packages

Release 15.2

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OBJECTIVE OF GUIDE

The objective of this guide is to demonstrate how to import a stacked-DIE type of package with wire bonding, in CDNSiP database, into ***HyperLynx 3D EM Designer*** for EM model extraction. A typical design (*stacked_die.sip*) will be discussed in the following sections to exemplify the main features of ***HyperLynx 3D EM Designer*** covering thick/thin model, HALO function, solder balls, bond wires, different types of nets as well as vias and ports.

WHAT IS HYPERLYNX 3D EM Designer

HyperLynx 3D EM Designer is specially designed to fill the gap between IC packaging designers and circuit/signal integrity engineers. ***HyperLynx 3D EM Designer*** provides an interface to Cadence's Allegro Package Design and CDNSiP tools to enable a layout-to-EM-model flow. Circuit/IC designers without solid EM background can use ***HyperLynx 3D EM Designer*** to quickly generate EM models and obtain accurate EM simulation results.

HyperLynx 3D EM Designer IMPORT FLOW

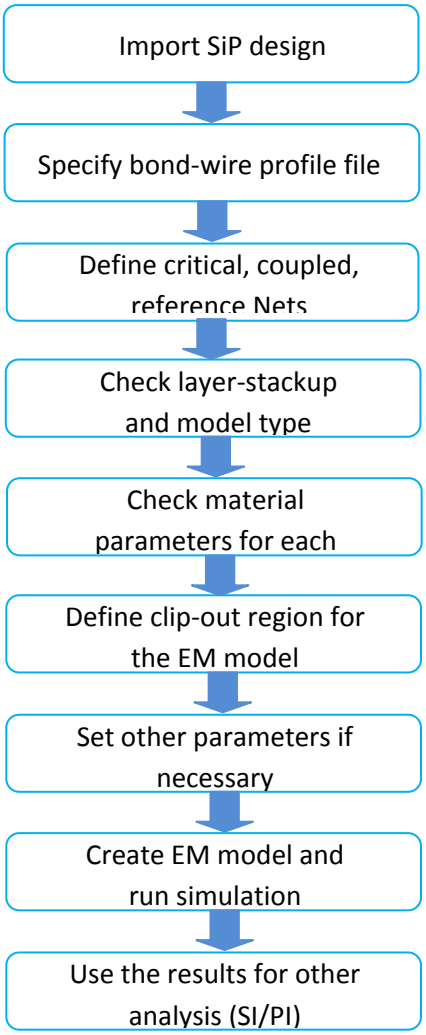


Fig. 1 Automated Packaging Database Translation to *HyperLynx 3D EM Designer*

Fig. 2 shows the stacked die design that will be imported into ***HyperLynx 3D EM Designer*** for EM simulations:

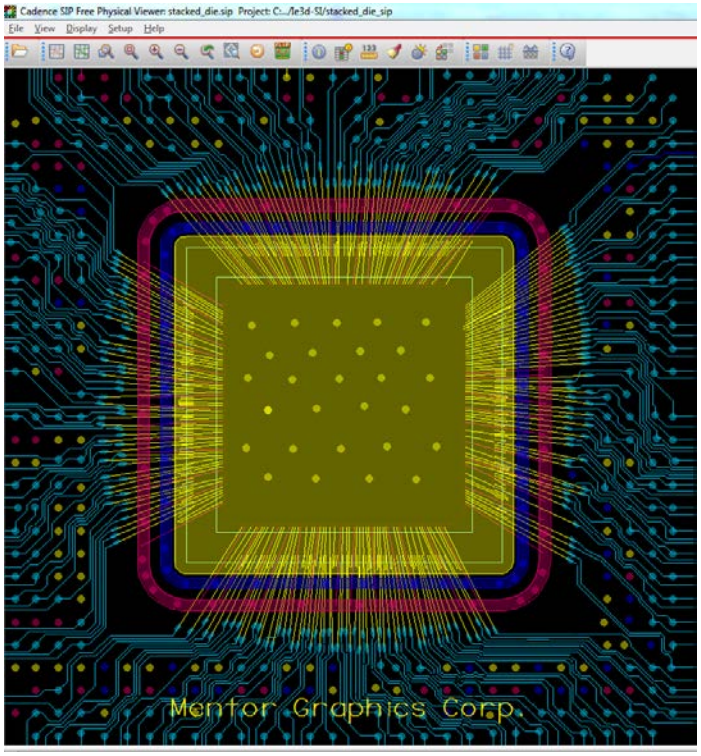


Fig. 2 A Typical Stacked Die Package Design

The following gives the step-by-step procedure to import a .sip file into ***HyperLynx 3D EM Designer***. This procedure requires that the Cadence's CDNSiP be installed on the same computer as ***HyperLynx 3D EM Designer***.

1. Navigate to ***AGIF*** on ***HyperLynx 3D EM Designer Program Manager*** as shown in the following picture:

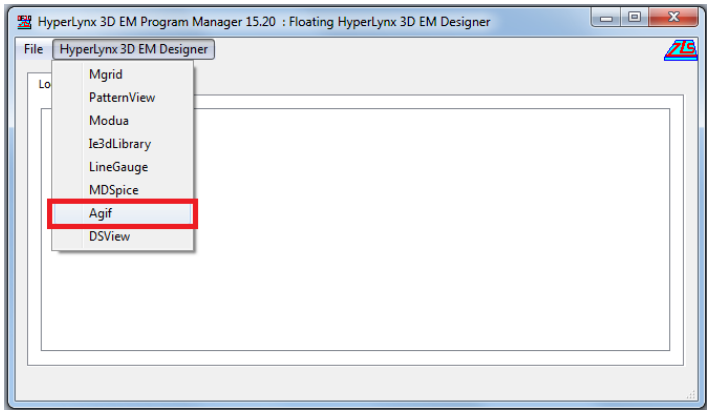


Fig. 3 HyperLynx 3D EM Designer Program Manager

2. Select **Cadence Allgero to HyperLynx 3D EM flow (From APD or SiP File)** and click **OK**

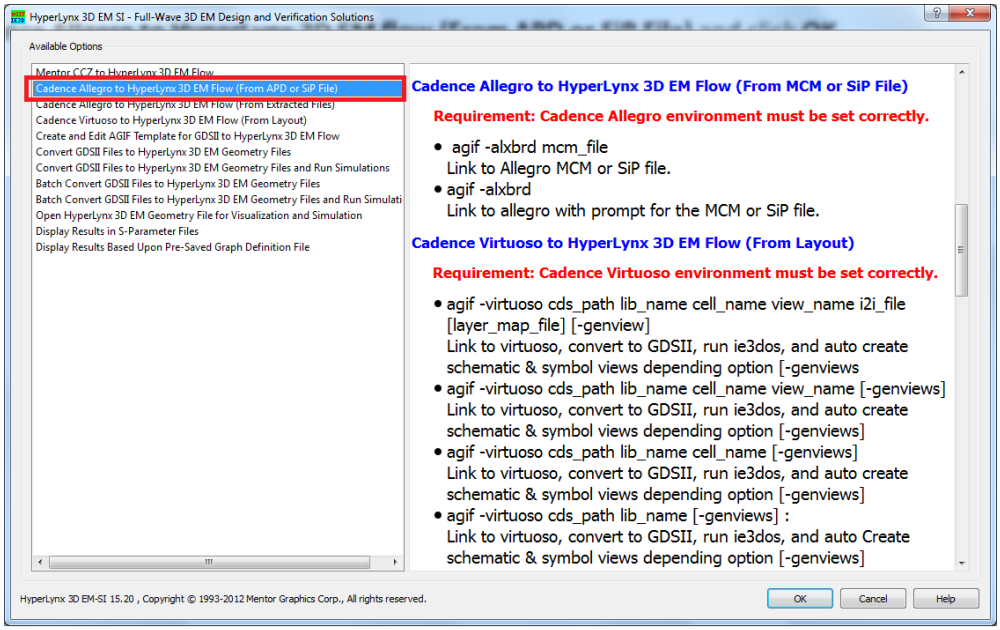


Fig. 4 AGIF Main Menu

3. Browse to the **.\SDD_HOME\IE3D\Ie3d-SI\stacked_die_sip** directory and select **stacked_die.sip** and click **Open.**

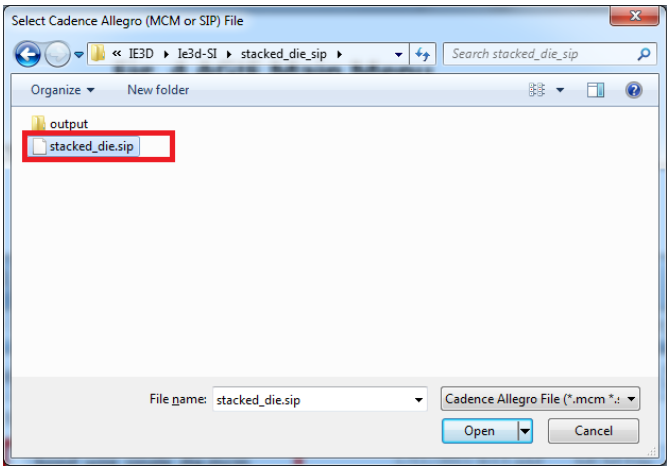


Fig. 5 Select Package Design

4. The following window appears asking if there are bond wires in the design:

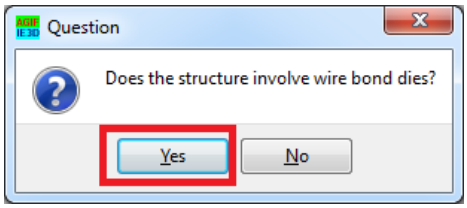


Fig. 6 Question about Bond Wire Information

5. Click *Yes* button to proceed since there are bond wires in the example, the program will prompt for the bond wire profile:

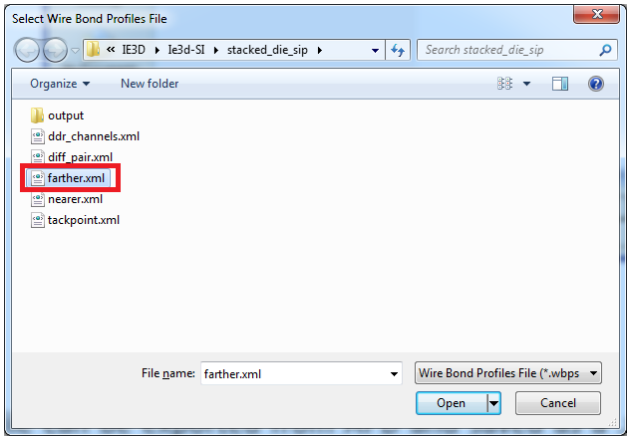


Fig. 7 Bond Wire Profile File

Note that the bond wire profile can be exported from CDNSiP and saved in a .xml file. User can refer to Cadence's CDNSiP manual about exporting wire profiles. For this case, the wire bond profile files are:

farther.xml
nearer.xml
tackpoint.xml

Select any one of these files and click *Open* button.

6. The following window will show up after the entire database has been successfully read into AGIF:

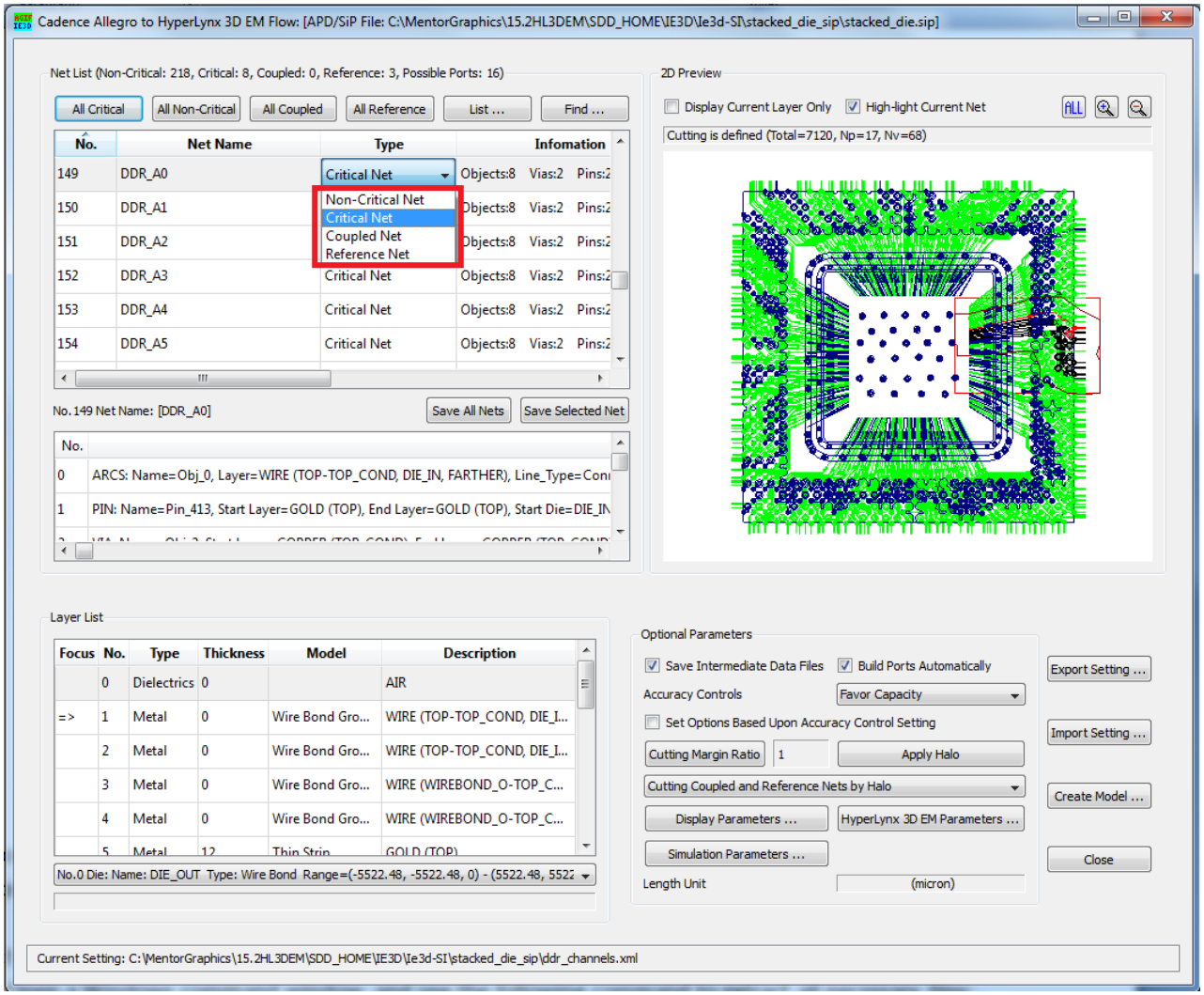


Fig. 8 Imported SiP Design

If your Cadence CDNSiP is not installed on the same computer where ***HyperLynx 3D EM Designer*** is installed, you can follow the steps below to import your Cadence .sip design:

1. Extract necessary files by using Cadence EXTRACTA. The EXTRACTA normally is in \Cadence\SPB_16.3\tools\pcb \bin\. Open a Windows command window, and use the following command to extract all necessary files:

   extracta -c -q -r "X: \stacked_die.sip " "X:\stacked_die.txt" "X:\stacked_die.xsec" "X: \stacked_die.nets" "X: \stacked_die.dstk" "X:\stacked_die.pstk"

   Totally four files will be generated with *.xsec*, *.nets*, *.dstk* and *.pstk* extensions respectively. These four files will be used for importing the .sip design in AGIF. Please remember the wire bond profile file should also be generated separately from Cadence CDNSiP as shown above.

2. Select **Cadence Allgero to HyperLynx 3D EM Designer flow (From Extracted Files)** and click **OK**:

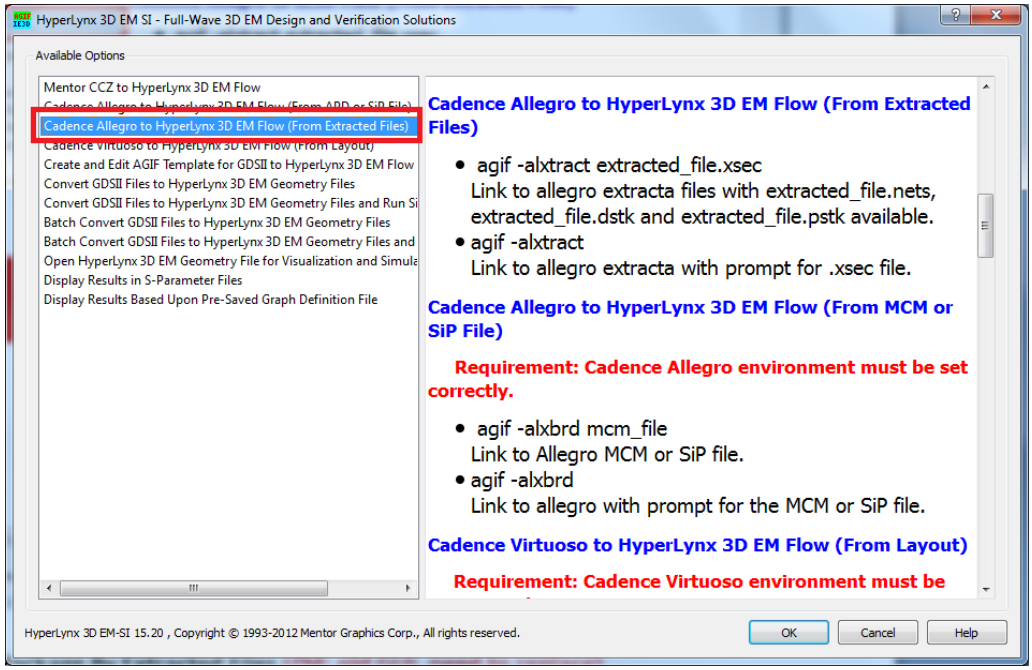


Fig. 9 Import Package Design By Extracted Files

3. Select the **.xsec** file and click **OK**:

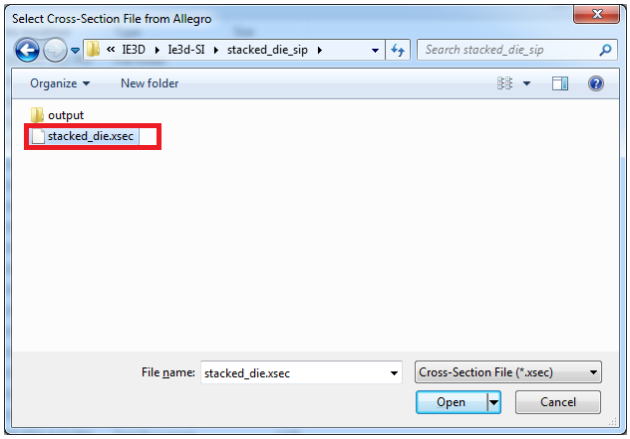


Fig. 10 Select the .xsec file

4. The program shows that all other three files are automatically used for importing data:

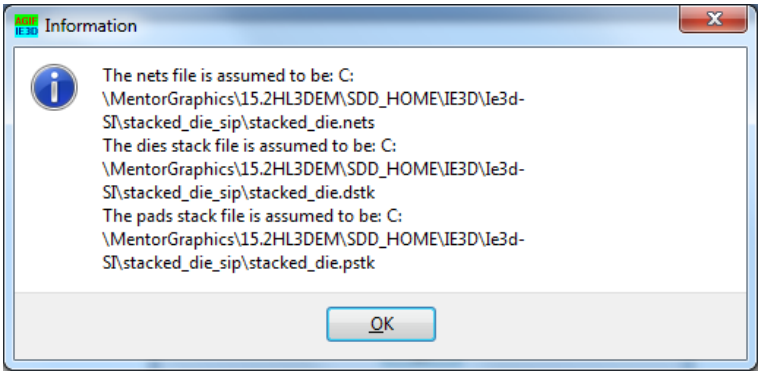


Fig. 11 Information for Other Files

5. Again, the program will ask if there are any bond wires in the design:

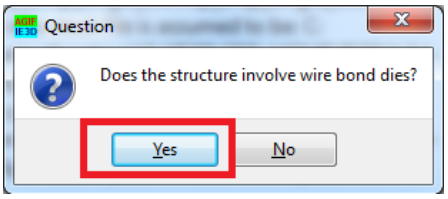


Fig. 12 Query on Bond Wires

6. Click *Yes* to proceed.
7. Select the bond wire profile as shown in Fig 7.
8. The imported structure should be showing up as shown in Fig. 8.

AGIF PARAMETER SETTINGS

After the structure is sucessfully imported into AGIF, some parameter settings need to be taken care of in order to get correct EM model:

- Define Critical/Coupled/Reference nets in the net list window
- Define layer type for each metal layer. Change material parameters if necessary
- Define other parameters, such as clip-out region by using HALO, simulation parameters etc.
- Define other geometry-handling parameters
- Create EM model

The Cadence CDNSiP to ***HyperLynx 3D EM*** flow has been further automated on version 15.2 to make the flow smooth and less confusing when extracting EM models. The following steps show how to define other parameters for the stacked die example:

1. Under *Netlist* section, select and define No.149 net "**DDR_A0**" to No.156 net **"DDR_A7"** as **critical nets**, and No. 104th net "**POWER2"**, No. 227th net **"VSS"** and No. 228th **"PWR1"** as **Reference Net** respectively. You may click

"*List…*" button to get the complete list of the defined nets, or "*Find…*" button to search for a specific net by name.

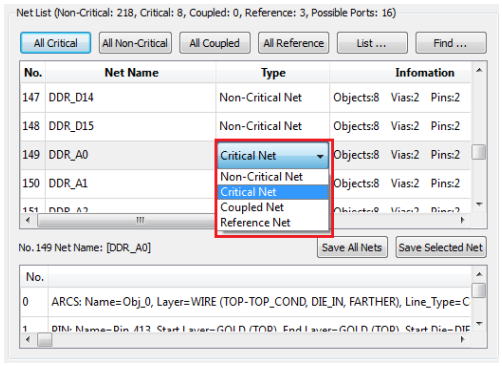


Fig. 13 Define Net Types

2. In the *Layer List* window, click the combo box in *Type* column to define model type of each metal layer. As can be seen in Fig 14, No. 1~4 layers have been automatically defined as bond wire layers. Metal layers can be either *Thin* or *Thick* type. If a metal layer is not intended to be included in the EM model, define it as *Void*. To change the material parameters of a metal or substrate layer, double click the layer and change the parameters in the material window. For this example, Layer 9 and 15 should be defined as *Thick* model since the thickness should be applied to traces to preserve high simulation accuracy:

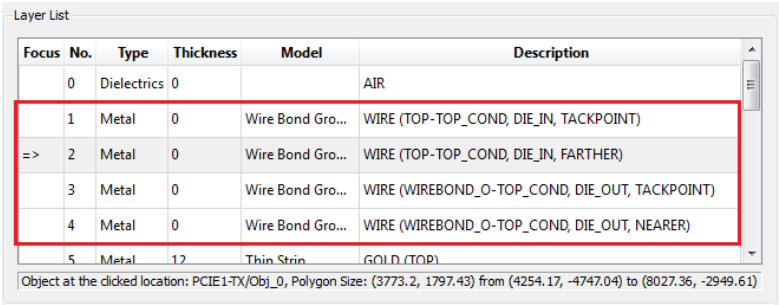


Fig. 14 Define Layer Type

3. Define other parameters in the *Optional Parameters* region:

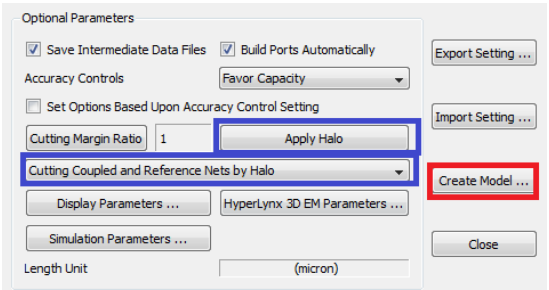


Fig. 15 Optional Parameters

Optional parameters include *Display Parameters*, *HyperLynx 3D EM Parameters*, *Simulation Parameters*, and EM model boundary parameters. Normally the default values/settings serve well for most structures. One useful function is the *HALO* function that automatically define the closest boundary surrounding the defined nets for optimal EM simulation region. User have options to define either rectangular clip-out region, or optimized region using *HALO* function.Please refer to *AGIF User Manual* for more details on these parameters. For this example, we use rectangular region, and the margin value is 1.

4. Click *Create Full Model* button, and the *HyperLynx 3D EM Parameters* window will show up to let user double check if *HyperLynx 3D EM* parameters have been defined correctly. You can give a new name in the Geometry File Name edit box. Click *OK* to proceed:

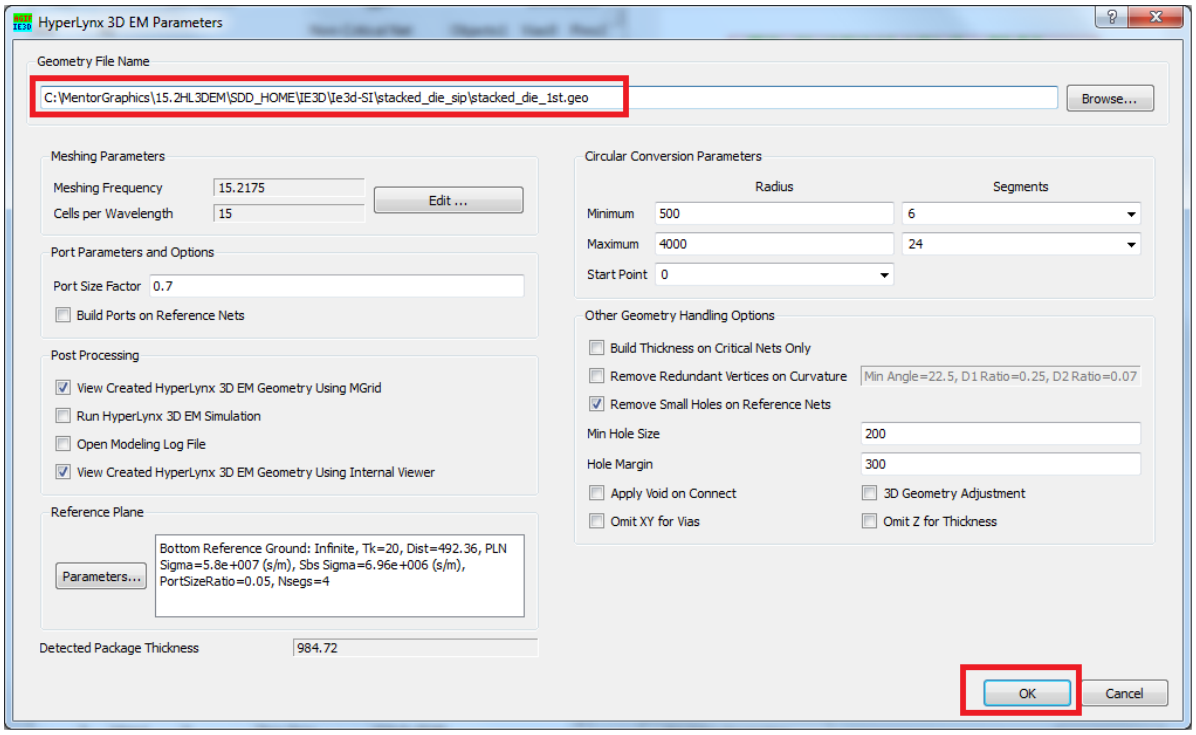


Fig. 16 *HyperLynx 3D EM* Parameters

5. A progress window will show up as follows:

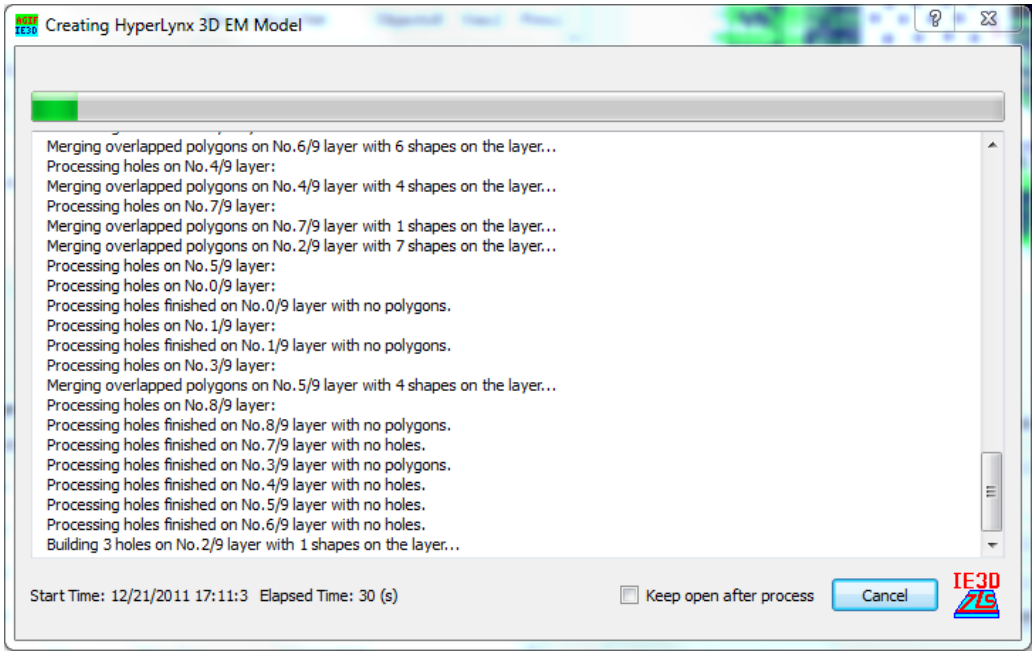


Fig. 17 Progress of Model Creation

After the whole process is completed, the created EM model will be automatically shown:

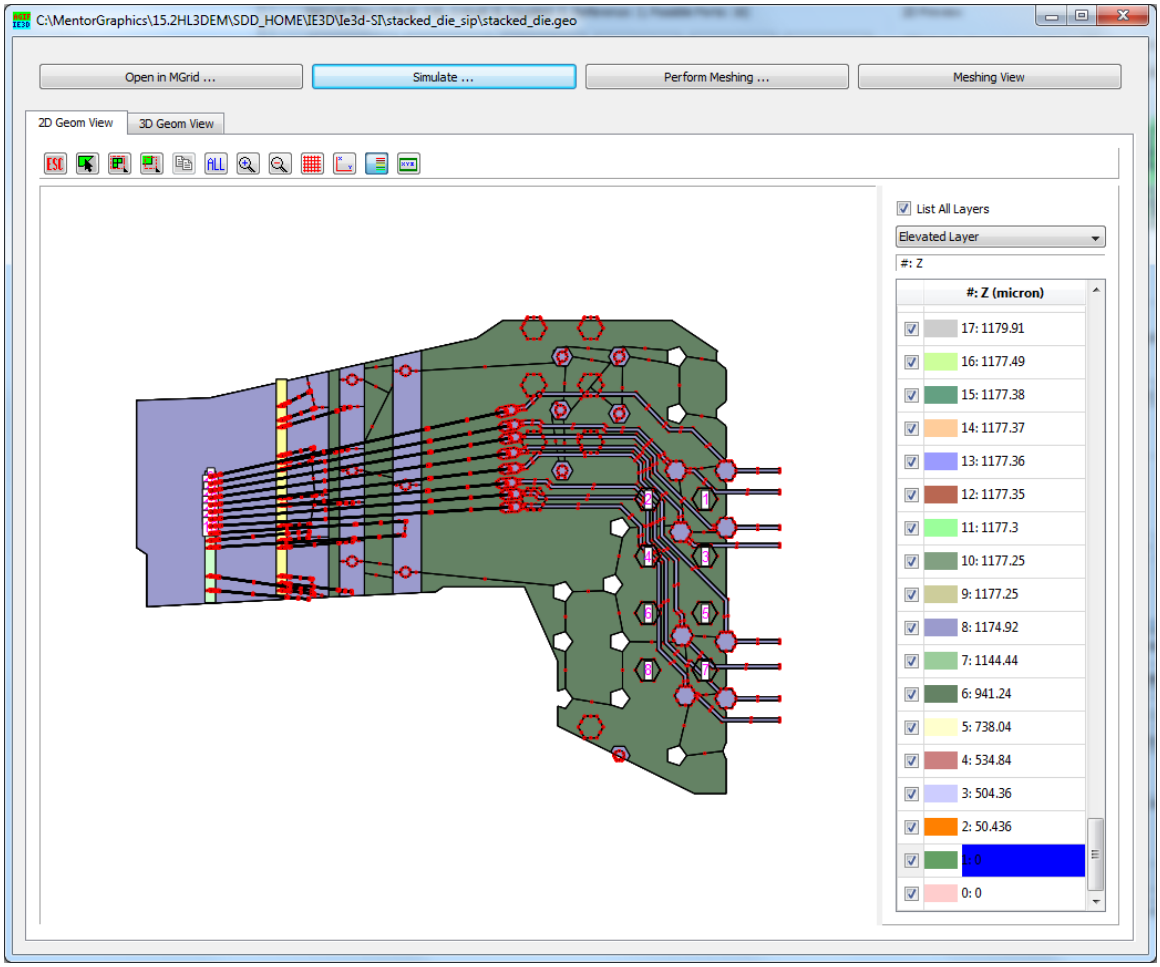


Fig. 18 Created EM Model on QT Interface

On Windows OS, the created EM model will also be automatically sent to MGrid for further modification if necessary. Users can launch simulations either from the interface shown in Fig. 18, i.e. QT interface, or from MGrid. The created model in MGrid is shown below:

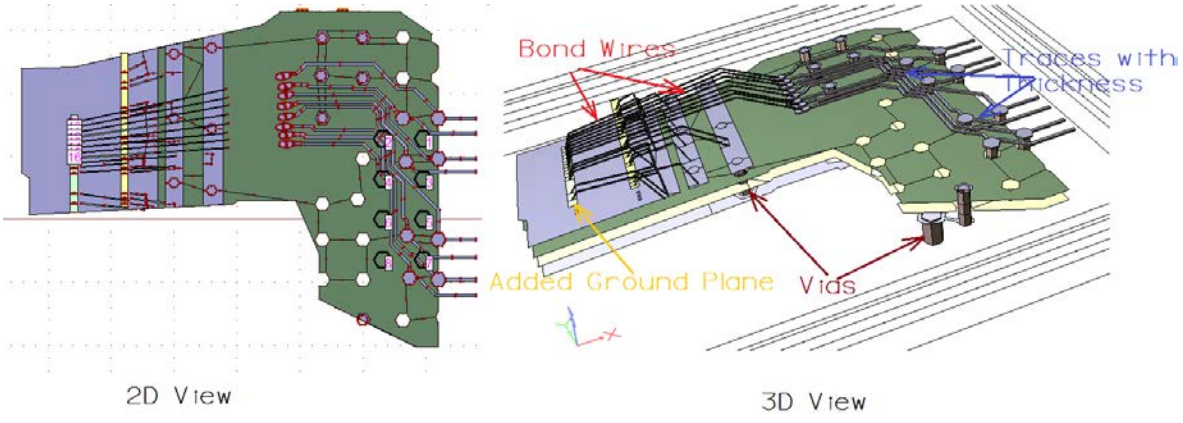


Fig. 19 2D and 3D View of the Created EM Model

As can been seen in the 3D view, the entire EM model has been automatically set up including 3D objects. The ports are also automatically created. The added reference plane, where bond wires land, representing the die layer in the original design is automatically created for terminating bond wires. The created structure can also be further editted in case, for example, some parts in the EM model are irrelevant and can be removed, or some necessary objects need to be added to the EM model.

HYPERLYNX 3D EM FULL-WAVE EM SIMULATION

After the EM model has been successfully created, we are ready to simulate the structure. Basically the structure can be simuated through two interfaces: one is shown in Fig. 16, the other is MGrid. The following paragraphs show the procedure of simulation via both interfaces:

1. QT Interface

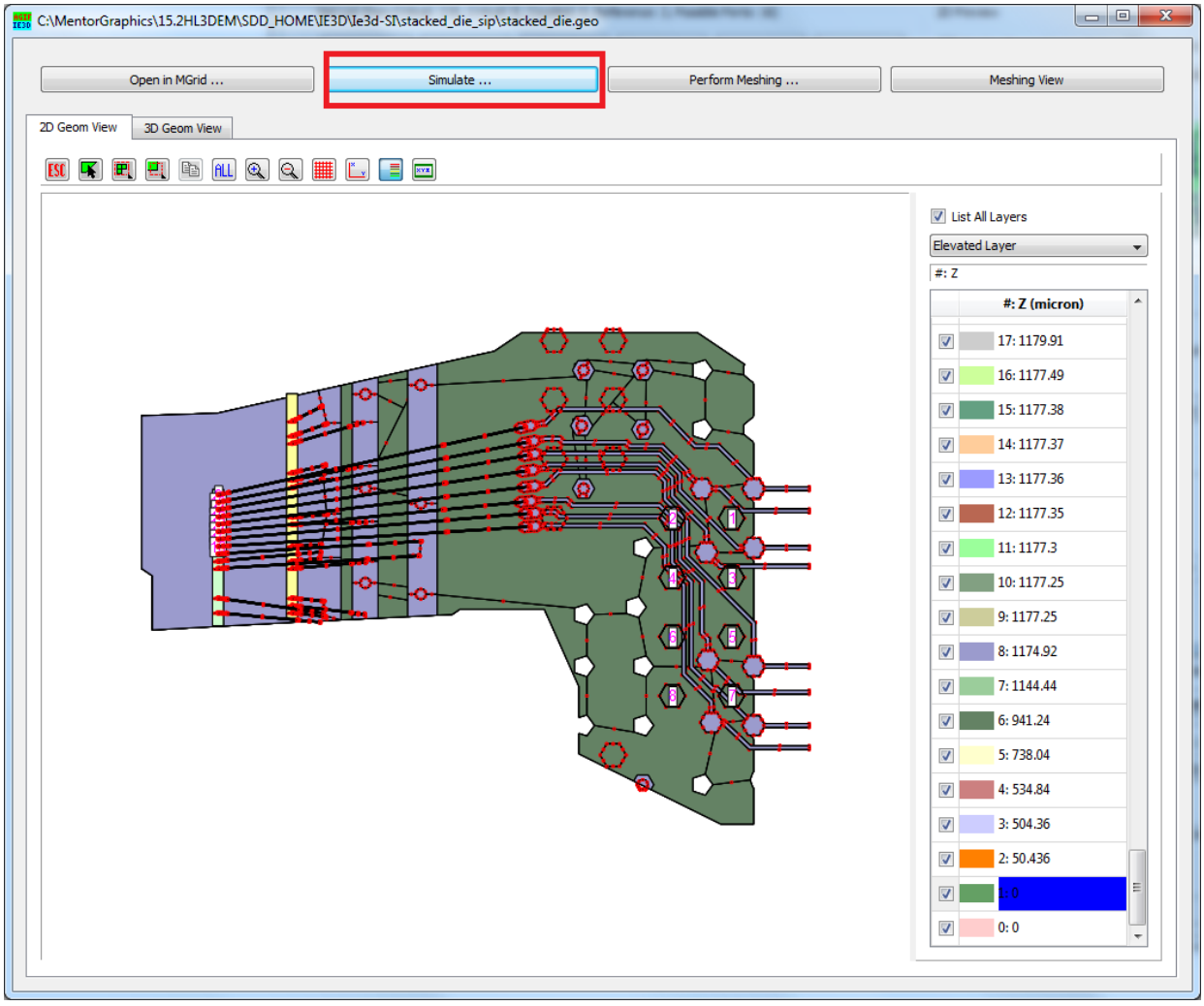


Fig. 20 QT Interface

Click the *Simulate* button on the QT interface, and the *Simulation Setup* window will show up as shown below:

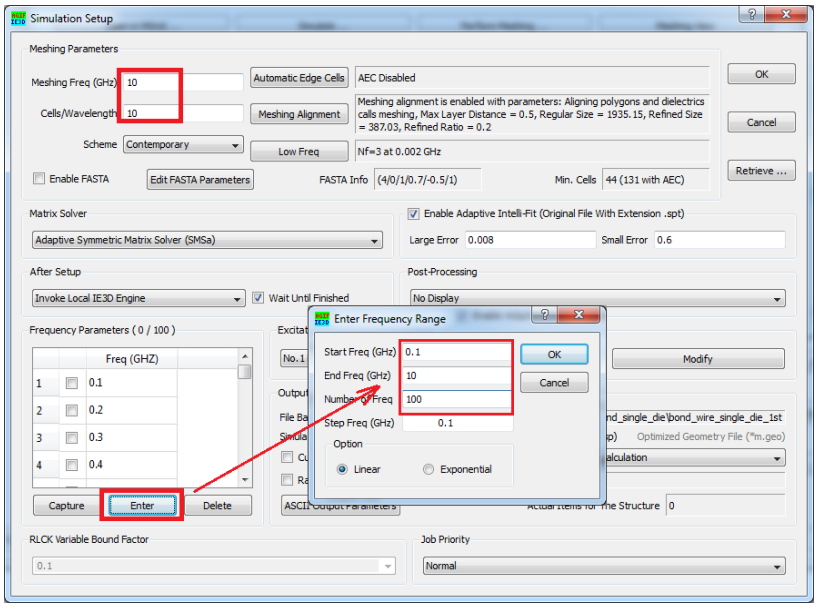


Fig. 21 Simulation Setup Window

Enter **10** for both *Meshing Frequency* and *Cell/Wavelength*, which define how the structure will be meshed; then define the frequency range and number of frequencies in *Frequency Parameters* list box. Click the *Delete* button to delete all or some of the predefined frequency points, and click *Enter* button to redefine the freqeuncy range and number in case that the predefined frequency range and number are not correct. For this case, we define the frequency range is from 0.1GHz to 10GHz, and 100 frequency points. Finally hit the *OK* button to start the simulation.

2. MGrid

MGrid provides more sophisticated functions than the QT interface where the automatically created EM model can be editted and modified.

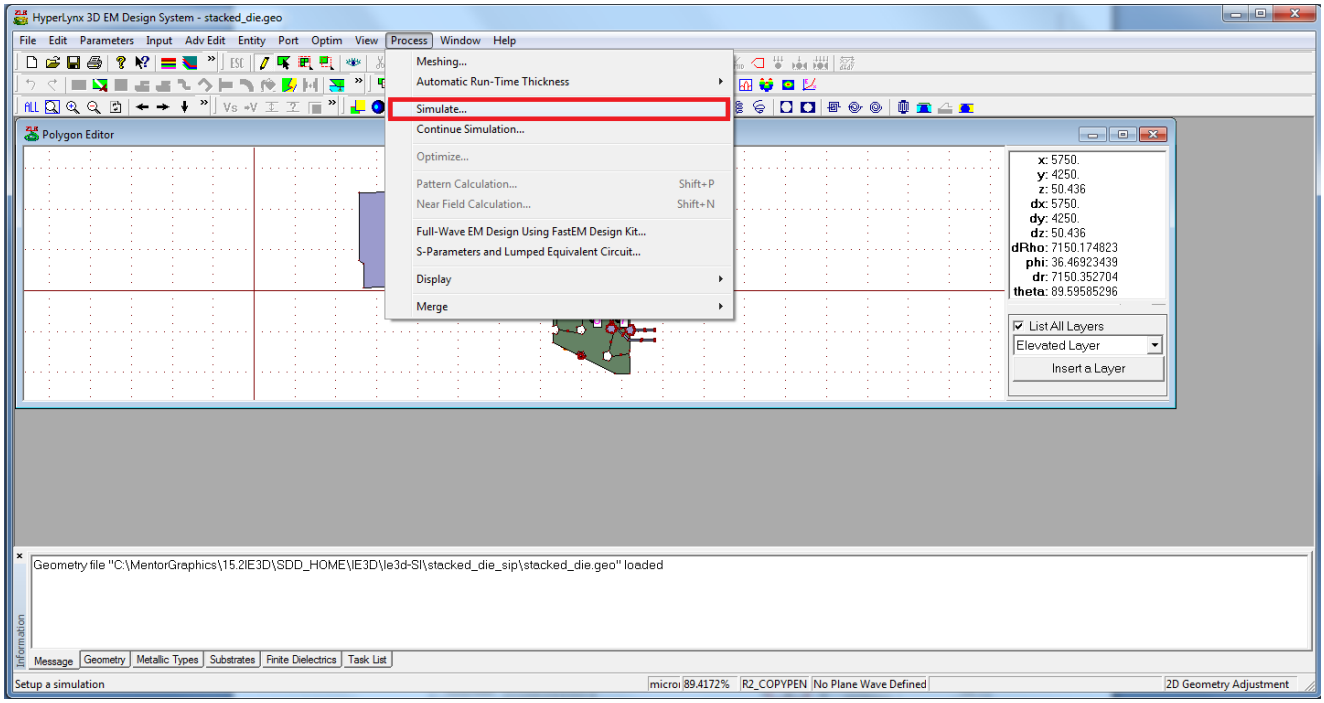


Fig. 22 EM Model in MGrid

Fig. 22 shows the EM model in MGrid. Go to *Process* and then *Simulate…*, a similar *Simulation Setup* window will show up as shown below:

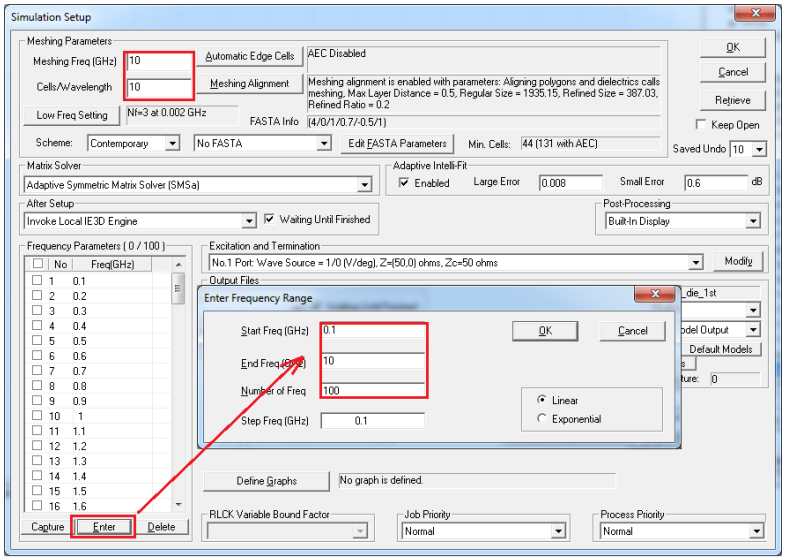


Fig. 23 Simulation Setup Window in MGrid

Use the same parameters as those shown in the QT simulation setup window to start the simulation.

SIMULATION RESULTS POST-PROCESSING

After the simulation is completed, the result window will automatically show up and wait for user's data post-processing:

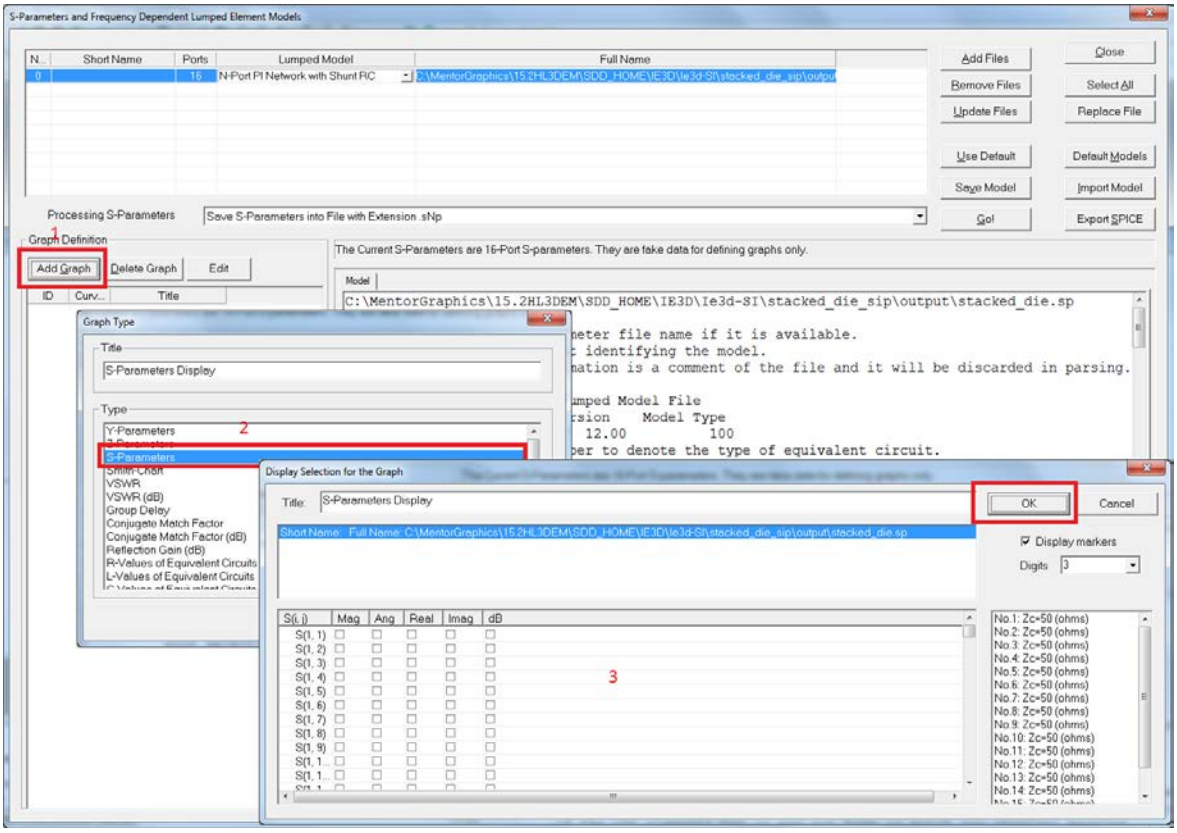


Fig. 24 How to Display Results

HyperLynx 3D EM provides a wide range of simulation results from a single simulation, for example, S-parameters, Z-parameters, Y-parameters, RLGC values of the equvelent circuit etc. Fig 25 illustrates how to get the S-parameters of port 1:

- Click *Add Graph* button
- Highlight *S-parameters*
- Check *S(1,1) ~ S(1,16)* in *dB* column
- Click *OK*
- Click *plot_0* tab to see the S-parameters of port 1

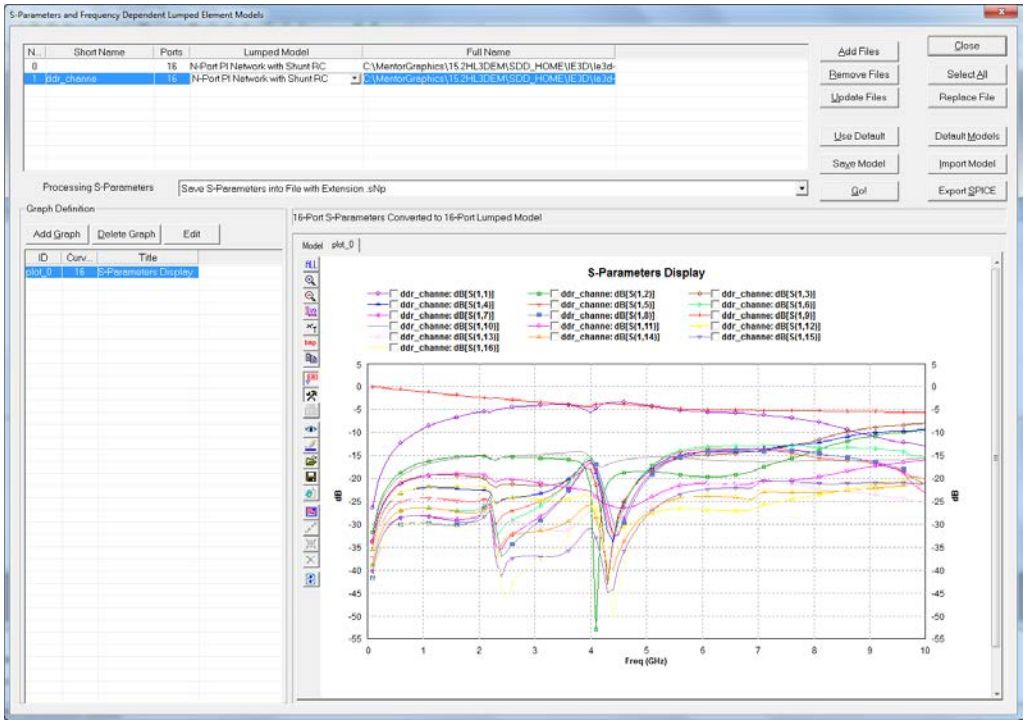


Fig. 25 S-parameters Display

Users can use the above S-parameter model for time-domain simulations using Mentor Graphics' *HyperLynx*.

An interesting experiment for demonstrating the difference between thin and thick model has been carried on by defining the trace layers (layer 9 and 15) as *Thin* model:

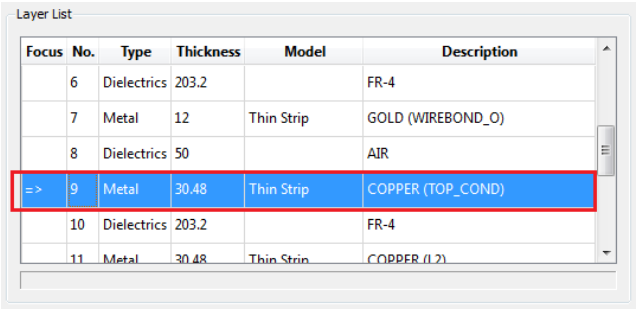


Fig. 26 Thin Layer Model

Create the EM model by follwing the steps shown above, and run EM simulation. You can also open the *ddr_channels_thin_model.geo* file in the <install_dir>\Ie3d-SI\stacked_die_sip\ directory, and run EM simulation directly. The comparison between the S-parameters are shown in Fig. 27:

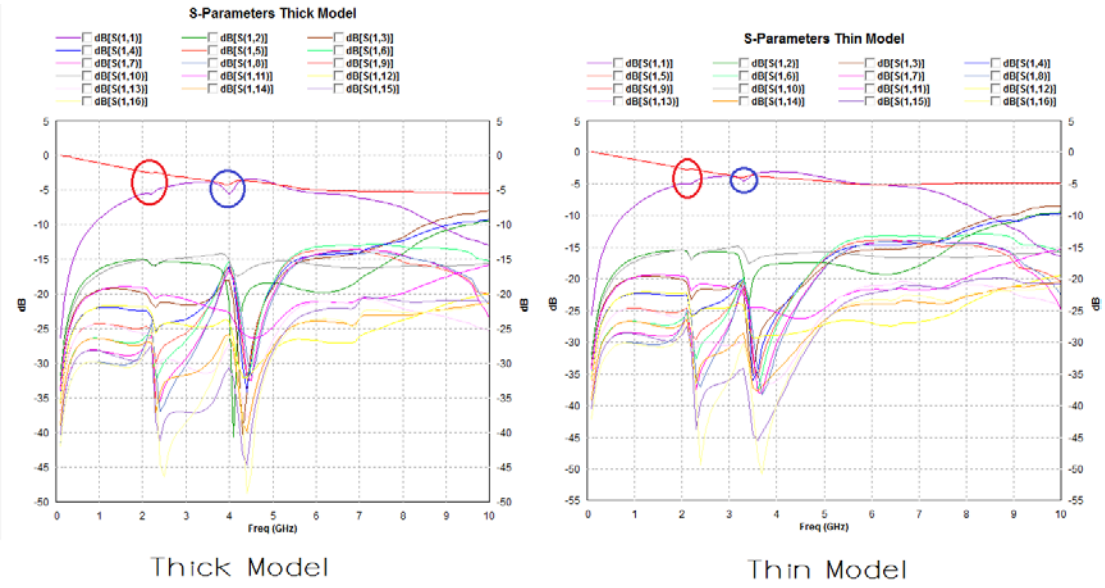


Fig. 27 Comparison between Thin and Thick Trace Models

Basically the shape of each curve looks alike, but the resonances occur at different frequency points between the two model. This is why it is recommended to apply metal thickness on the signal traces in order to get more accurate results.

SPICE Equivalent Circuit

HyperLynx 3D EM Designer provides SPICE model extraction based on the simulated S-parameters. It is recommended to use the S-parameters directly in a SPICE simulator for wide band transient analysis. However, some designers may also want to use RLC equivalent circuit and perform SPICE simulation on the extracted RLC equivalent circuit.

Basically there are two types of SPICE equivalent circuit models users can obtain from ***HyperLynx 3D EM Designer***:

- ✓ Low frequency RLC equivalent circuit with physical meaning, and
- ✓ Wide-band SPICE equivalent circuit without physical meaning

Both equivalent circuit can be obtained by using *Modua*

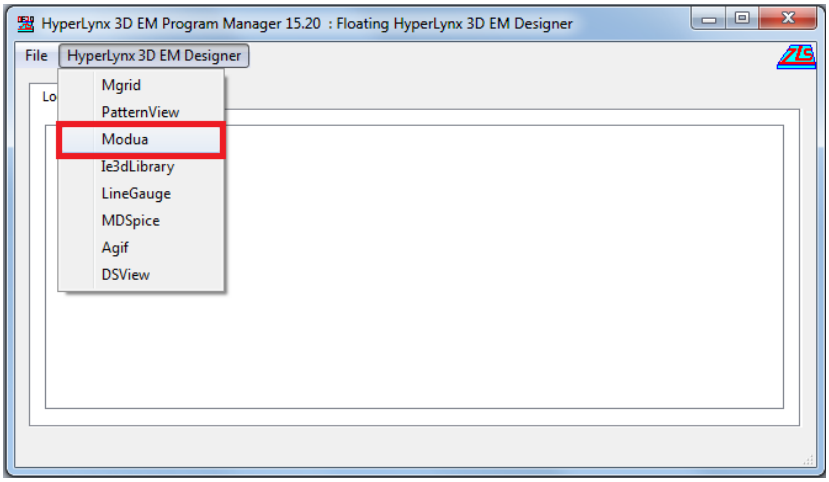


Fig. 28 Modua On HyperLynx 3D EM Designer Program Manager

(1) Low Frequency RLC Equivalent Circuit Extraction:

1. Launch *Modua* from ***HyperLynx 3D EM Designer Program Manager*** (see Fig 28).

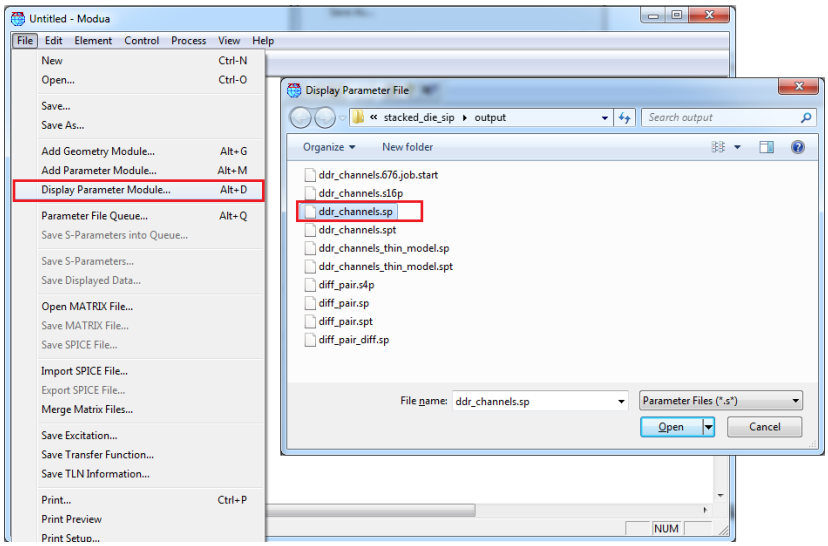


Fig. 29 Modua Window for Displaying S-parameter File.

2. Select **MODUA->File->Display Parameter Module** (see Fig. 29). Select the file:

   .\SDD_HOME\IE3D\Ie3d-SI\stacked_die_sip\output\ddr_channels.sp.

   Modua is a utility for frequency-domain circuit simulation. It automatically sets up a black box for the S-parameter data block. You can see the S-parameters displayed on the window.

3. Select **Modua->Control->Display Toggle** and you will see the 16-port black box representing the 16-port S-parameters data on Modua.

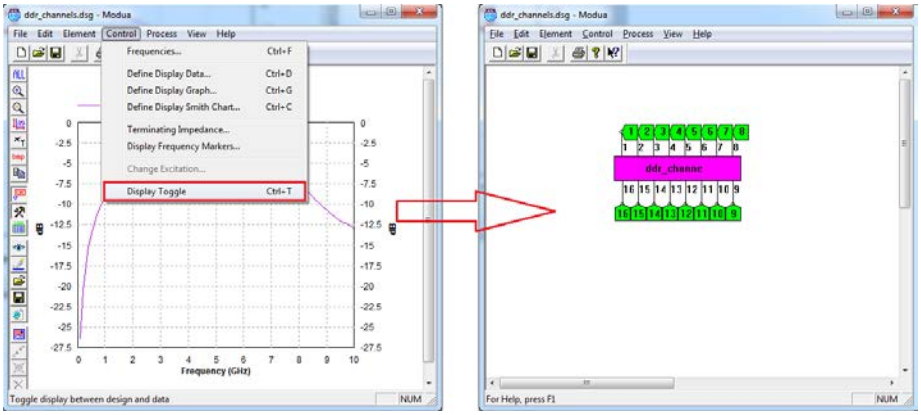


Fig. 30 S-parameters Display to Circuit Model

4. Select **Modua->Process->LC-Equivalent** command. Modua will prompt you the simulation results will be abondoned. Select *YES* to continue.

5. In the *Define Frequency* dialog, uncheck the the main check box to de-select all frequency points (see Fig. 31). Check the check box for *No.1: 0.1 GHz* frequency point. We are going to extract the RLC equivalent circuit at 0.1 GHz. Select *OK* to continue.

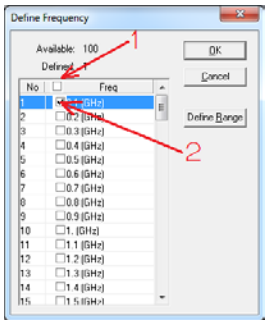


Fig. 31 Select Frequency Point for SPICE Model Extraction

6. Make sure the selection is "*First N/2 Ports for Output ports (Style 1)*" when Modua prompts you for *Port Definition Style for the Equivalence*. This command is to extract the RLC equivalent circuit of coupled interconnects. For our example, we have 16 ports or N = 16. We are extracting the coupled RLC equivalent circuit from it (see Fig. 32).

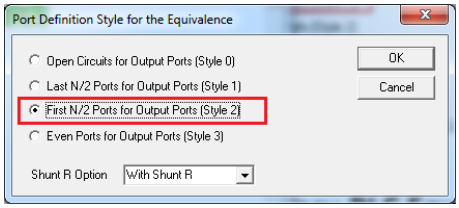
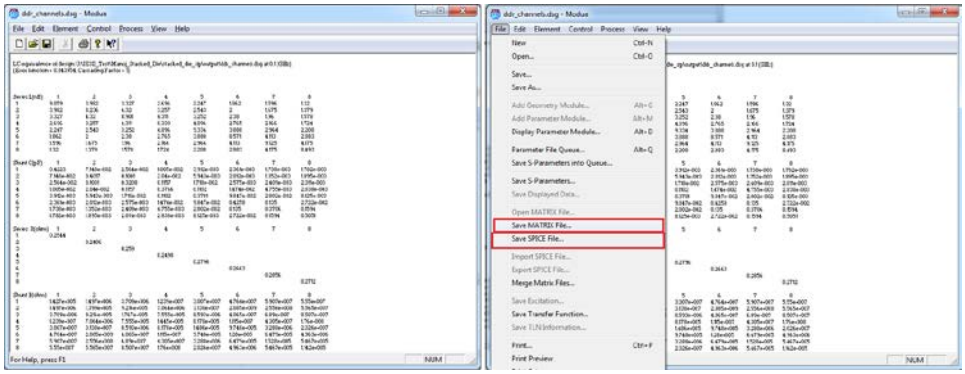


Fig. 32 Extracting Low Frequency RLC Equivalent Circuit on Modua



(a) (b)

Fig. 33 Extracting RLC Equivalent Circuit of the Coupled Interconnects

7. Select OK and Modua will extract the RLC and display the results in matrix form (see Fig. 33a). You can also select:

- ✓ *MODUA->FILE->Save MATRIX File* to save the data into the matrix form in an ASCII file (see Fig. 33b), or
- ✓ *MODUA->FILE->Save SPICE File* to save the data into a SPICE sub-circuit (see Fig. 33b). The SPICE data is saved into file: *ddr_channels.lib*. You can import the .lib file into other SPICE simulators to do circuit simulations.

(2) Wide-Band SPICE Equivalent Circuit:

Wide-band SPICE equivalent cirucit can be performed on S-parameters data on either Modua or on MGrid:

- ✓ On Modua, you can select *Process->General Lumped Equivalent Circuit*.
- ✓ On MGRID, you can open *Window->S-Parameters Display* button. Then, you can select *Export Spice* and choose *Wide Band Extraction*.

The elements of the extracted SPICE netlist do not have physical meaning. The subcircuit does not guarantee all the components are passive due to the fact of fitting an N-port S-parameters into some specific topology. Designers are strongly suggested to perform time-domain analysis directly on S-parameters by using *Mentor Graphics Hyperlynx*.

The example showing here is primarily for new ***HyperLynx 3D EM Designer*** AGIF users. For more details and advanced topics, please refer to AGIF User Manual where more complicated structures and more funtionalities on AGIF will be discussed.

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