



HyperLynx[®] 3D EM

RFID Tag Design Quick Start Guide

Software Version 15.2

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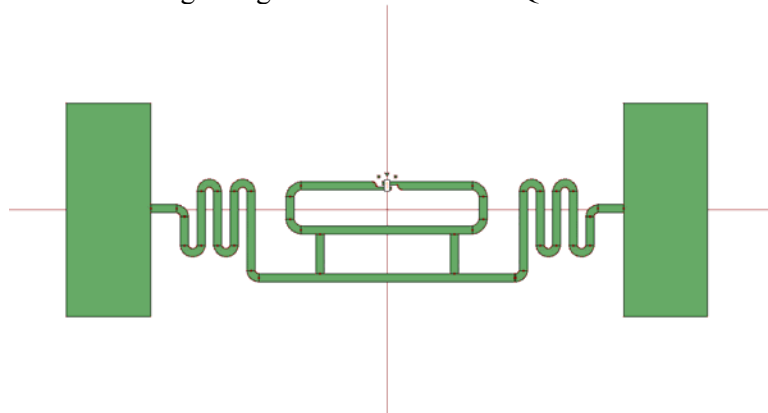
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Introduction

Purpose of Guide

This manual is intended as a quick guide reference for using Mentor Graphics IE3D as the design tool for a RFID tag design. It does not replace the manual but rather shows the detailed steps and key strokes required to design a RFID tag based upon a set of requirements. It is expected that as the designer gains experience he will no longer need this quick start guide but rather will use the primary manual as his reference tool.

Tag Design Produced from the Quick Start Guide



Reference Files

These are files, provided by Mentor Graphics IE3D that can be used during the RFID Tag design process. They are the foundation of a reference library suite that the tag designer will develop to simplify future designs.

1. Reference Loops

Two reference loop designs are provided, one for each of two different die attach methods. The first is a strap design in which the die is attached to a small substrate that then provides attachment pads. These pads then allow connection to the antenna via some conductive adhesive. The second is a direct Flip Chip attachment, in which the die is directly attached to the antenna. Both designs are resonant at 915MHz with typical RFID I.C. parameters so they can be used as a starting point for a RFID tag design. These designs are intended as a starting point only. They **will require layout modification** to exactly match any particular process and will require inductance adjustment to match antenna and particular die specification. The following are the file names for these two designs:

- Ref 1mm Loop Strap.geo
- Ref 1mm Loop FC.geo

2. Reference IC Representations

There are multiple manufactures of RFID Tag chips and each has their own set of electrical characteristics. Typically the characteristics are specified as parallel Resistance and Capacitance. When designing a RFID tag it is necessary to convert these impedances to Series Equivalents in order to determine the conjugate match of the antenna. This can be accomplished with the following equations:

$$R_{chipSeries} = R_S / (1 + (\omega R_S C_S)^2) \quad X_{chipSeries} = -j\omega C_S R_S^2 / (1 + (\omega R_S C_S)^2)$$

In IE3D, however, has a method to convert the parallel R and C values into frequency depended series impedances for use in the tag design. This is accomplished with **IE3D Modua Module**. Modua allows the creation of a model, via an included schematic capture, of the parallel parameters and then specify the component values. It will then be attached to the antenna geometry post processing to determine the conjugate match.

The designer still must address the fact that a strap will add some parasitic capacitance but this can be accounted for by having two Modua modules, one for a strap and one for flip chip attachment. As a rule of thumb you can add approximately .1pF of capacitance to a strap design using the same IC as a flip chip.

So again as a starting point for a future reference design suite, this guide has provided two reference designs, one for a strap based design and another for a flip chip design. These are not representative of any particular IC but rather typical of generic RFID devices. As with the Reference Loops they **will require modification** to exactly match any particular IC. The following are the file names for these two designs:

- **Ref IC Z1 Strap.sp** *Modua Module with values entered for a strap*
- **Ref IC Z1 FC.sp** *Modua Module with values entered for a Flip Chip*

3. Reference Tag Designs

Provided are two tag designs used for evaluation in this guide. The first is the final output product of the design from this guide. It can be used to compare the results obtained during the example exercise. The second is a reference tag used for the substitution method of determining tag sensitivity. The file names are as follows:

- **Eng Design Ref.geo** *The expected design geometry resulting from following this guide*
- **Golden Ref.sp** *The output of a reference tag that has been characterized for performance*

It should be noted that the Golden Ref.sp is not a real tag but given as an example for this guide. The tag designer is required to select and characterize his own reference tag.

4. Reference Geometries

One file is provided but the designer will add additional requirements as he becomes familiar with his typical requirements. These files are intended to be used as common geometries that can be imported into new designs. They will save the designer the time required to construct them on his own. The file name of the file provided is as follows:

- **1mm Meandering.geo** *Pre constructed geometries for use in new designs*

Section Definitions

This guide is divided into the following sections. The intent of each is also described.

1. Introduction

2. Requirements

The requirements are divided into two sub sets. The first is typical from a market driven specification. The second however, is the engineering interpretation of those marketing requirements. The engineering requirements are primarily used for the tag design while the marketing requirements will be used to qualify tag performance.

3. IE3D Setup and Additional Background

Opening an IE3D session and preparing the initial parameters. Also information concerning the actual manufacture of a RFID tag to use as background for the IE3D settings.

4. Initial Design Layout

This section details the how to construct the initial tag layout using IE3D M-Grid (Geometry layout editor). The objective is to converge upon a fundamental design that will prove concept and allow final optimization.

5. Tag Optimization

This is the modification of the Initial Design that will meet the Engineering Requirements.

6. Tag Qualification

This is the final simulations that confirm the tag will meet marketing application and operational frequency requirements.

Requirements

Typical requirements are driven by customers and come from marketing to solve a particular customer need. The designer must take these requirements and extract a set of engineering requirements that represent the actual design requirements. The following is a typical set of marketing requirements and an attempt to place engineering requirements that will reflect the same. This is not an exhaustive list and is to be used only as an example. The actual requirements and engineering interpretation will vary from company to company and from designer to designer.

Marketing Requirements

- | | |
|--------------------------|--|
| 1. Size | 1 inch (25.4mm) x 3 inch (76.2mm) |
| 2. Mechanical | Z-Axis of tag to be flat within 5microns (thickness) |
| 3. I.C. | Die, Company #1 ($R_p=1500\text{ohms}$ $C_p=.87\text{pF}$) |
| 4. Operational Bands | US, Europe, China |
| 5. Application | Plastic Bottle, 1mm thick, without metalized label |
| 6. Read Range | 2 meters minimum |
| 7. Polarity of Operation | Bottles aligned in a vertical manner |
| 8. Miscellaneous | Alternate operation of tag on corrugate and free space |

Engineering Requirements

1. Mechanical

- Size as specified, 24.4mm x 76.2mm
- Flip Chip Design to insure flatness
- Minimum Trace Width = 1mm, from existing process and manufacturing tolerances.
- Trace Height = .005mm, from existing process
- Trace Composition = Copper from existing process
- Substrate Layer Thickness = .06mm

2. Electrical

- IC characteristics, from the Zealand#1 die
 - a. $R_p = 1500\Omega$, as specified
 - b. $C_p = .87\text{pF}$, since the process will be flip chip there is no need to add .1pF parasitic capacitance
- Trace Conductivity = 4.7×10^7 , per copper specifications
- Relative Permeability = 1
- Loss Tangent for Dielectric and Permeability = 0
- Relative Dielectric Constants and material thickness
 - a. Plastic 2.9 @ 1mm
 - b. Corrugate, 1.2 @ 3.2 mm
 - c. Substrate, 2.9 @ .06 mm

3. Bandwidth

The requirements specify free space operation in the US (902 – 928 MHz), Europe (866 MHz) and China (a subset of the two). To cover these bands of operation the frequency bandwidth must be greater than (860 - 928) MHz = 62 MHz. The requirements also require operation applied to both 3.2mm of corrugate and 1mm of plastic. Operation on any non free space dielectric has the effect of shifting the bandwidth down to a lower center frequency. Since the dielectric constant of plastic is much larger than that of corrugate we can assume that if the tag functions on plastic it will also function on corrugate. An engineering estimation of the shift due to 1mm of plastic is around 50 MHz. If this shift is added to the free space requirements we see a new minimum bandwidth requirement of 62 MHz + 50 MHz = 112 MHz.

Another consideration when determining the bandwidth is the manufacturing tolerances of the die, its attachment method and the antenna itself. An engineering estimate of this shift is up to +/-20 MHz. When this tolerances is added to minimum as calculated above the engineering requirement for bandwidth become $BW = 112 \text{ MHz} + 40 \text{ MHz} = 152 \text{ MHz}$.

Also since it is known that the effects of additional dielectric are to move the center frequency of the bandwidth, it can be stated that the lower corner frequency of the free space bandwidth should be the lowest specified operational frequency. In this case it is 860 MHz. The following therefore become the engineering bandwidth requirements.

- $BW = 150 \text{ MHz}$
- $F_{L(\text{Free Space})} = 860 \text{ MHz}$

4. Turn-On Sensitivity

The turn on sensitivity is the amount of attenuation a reference RFID reader and antenna pair can accept and still power the tag at a reference distance. A typical distance that a tag is tested to determine this parameter is 1 foot. In addition in order to remove the effects of the tag backscatter (tag to reader communication) a circulator network is utilized to insure that the response is only due to the forward attenuation path (reader to tag communication). For example if a tag could accept 28 dB of attenuation in transmit power from reader in free space at 1foot and still be read, then the tag is considered a 28 dB tag. The Golden Ref Tag as included in this guide can be assumed to have been characterized on this type of test system to yield a Turn-On-Sensitivity and non attenuated read range on a reference setup as follows:

Golden Ref_{T-O-S} = 30 dB

Golden Ref_{READ RANGE} = 4 meters (See Tag Qualification at the end of this guide for Read Range Definition)

This number can be related to read range with the following equation:

$$RR = R_{REF} * 10^{\Delta dB/20} \quad (\text{where } \Delta dB \text{ is the attenuation at T-O-S at the reference distance})$$

if $R_{REF} = 1 \text{ foot}(.3048\text{m})$ then $RR = .3048 * 10^{\Delta dB/20} \text{ meters}$

It can be calculated from the above equations that the new design will require a minimum of $30-6 = 24\text{dB}$ to read at 2 meters. From this we can then specify that the match for the new design to provide adequate turn-on-sensitivity must be within 6dB of the golden ref in free space for both free space and when applied to the specified plastic. The following are requirements can now be deduced.

- Maximum Free Space Mismatch = 6 dB from the Free Space Golden Ref Design
- Maximum Free Space Variation over the 150 MHz bandwidth = +/- 3 dB, *our definition of bandwidth.*
- Maximum On Plastic Mismatch = 6 dB from the Free Space Golden Ref Design.
- Maximum On Plastic Variation over the 150 MHz bandwidth = +/- 3 dB, *our definition of bandwidth.*
- Maximum Delta dB between Free Space and Plastic over the entire user band = -3 dB, *desired characteristic.*

5. Backscatter Sensitivity

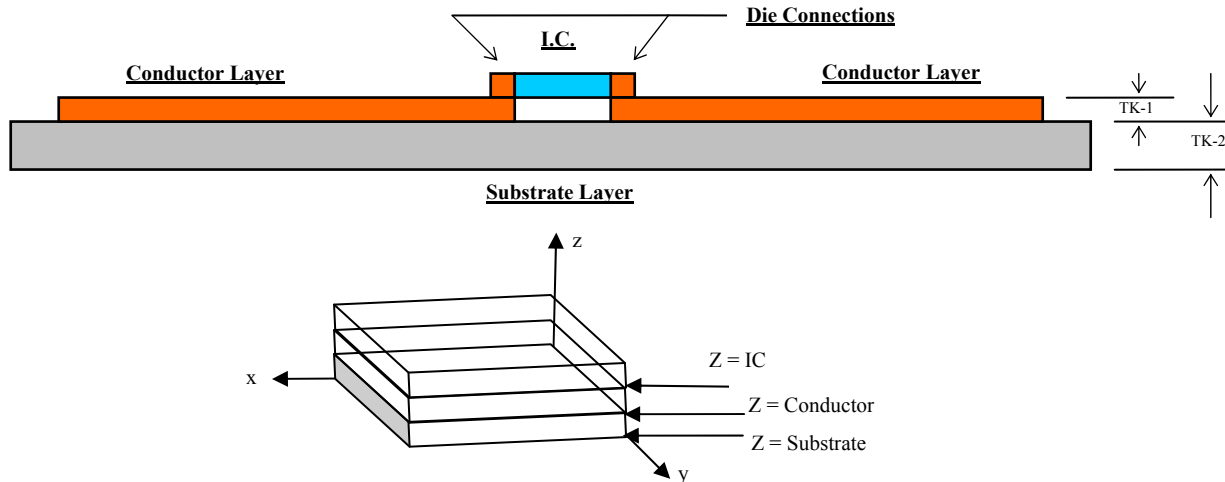
This was not specified in the requirements and as such will not be included in the engineering specifications. It is however a parameter that is sometimes an issue.

- BS, not specified

IE3D Setup and Additional Background

RFID Tag Construction

A typical RFID tag is comprised of four main components as shown in the following figure. The physical properties of each component must be defined in IE3D in order to get an accurate performance simulation.



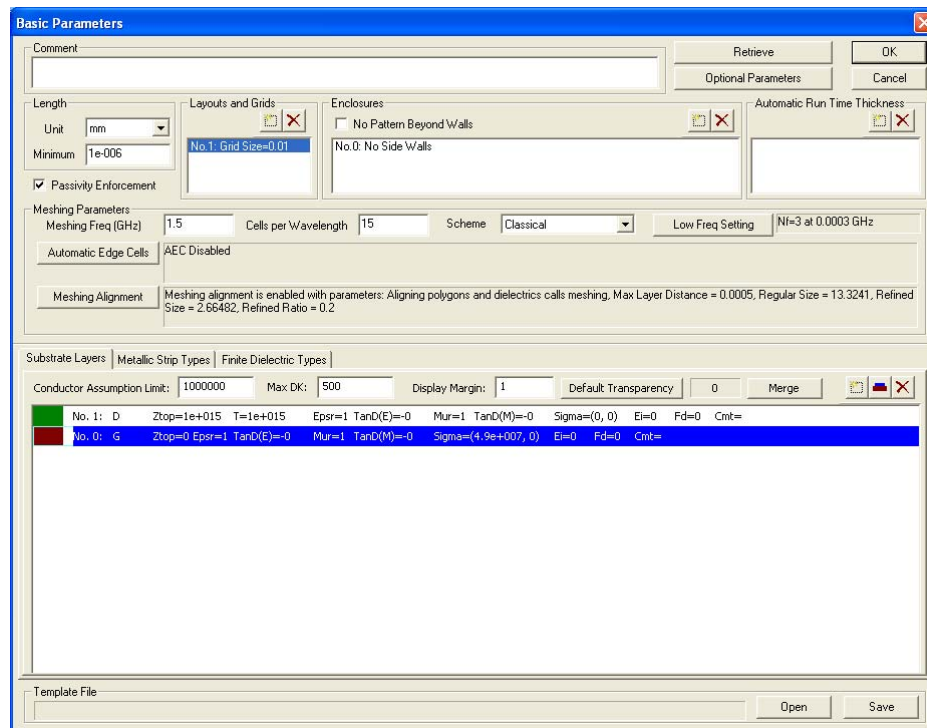
Opening IE3D

To start the design, accomplish the following:

1. Select the IE3D Program Manager **“ie3dpm” Icon** on the computer to be used for simulations
2. Select “MGrid” option from the ie3dpm menu list.
3. Select **“File” and “New”** to enable the **Basic Parameter** Window

Initial Basic Parameters

IE3D **“Basic Parameters”** is where the RFID tag’s substrate and conductor layer properties are defined as well as some drawing and simulation parameters. With reference to the window shown enter the following parameters.



1. Basic Drawing Parameters

Some basic drawing parameters are defined under **Basic Parameters** for this design the values chosen are as follows;

Enter, Unit of Length = mm
 Enter, Minimum Length = 1e-006
 Enter, Layouts and Grids = .01

2. Basic Simulation Parameters

Some basic simulation parameters are defined under Basic Parameters. They are of concern as they affect both the speed and accuracy of the simulation. The basic simulation parameters are as follows;

Enter, Meshing frequency = 1.5GHz to cover all frequencies
 Enter Cells per Wavelength = 15 initially
 Check the Scheme of Classical typically for tag designs

3. Substrate Layers

The substrate layer is the material that the conductor is applied to. It typically consists of some type of plastic with a defined dielectric constant as well as other mechanical and electrical properties. Initially IE3D requires the thickness and the specified dielectric constant to start the design. To enter the properties, select the **Substrate Layer Tab** and enter the parameters as shown in the following table.

| Substrate Layers Parameters (Red entries are different from the default of a new design) | | | | | |
|--|-------------------------|-----------------------|---------------------------|------------------------------------|--|
| Relative Dielectric Constant | Dielectric Loss Tangent | Relative Permeability | Permeability Loss Tangent | Conductivity Sigma Real, Imaginary | Comments |
| 1 | 0 | 1 | 0 | 0,0 | Ground Plane |
| 2.9 | 0 | 1 | 0 | 0,0 | Substrate Layer |
| 1 | 0 | 1 | 0 | 0,0 | Infinite Layer, exists after file save |

Double Click on the No. 0 G substrate data
 Enter **Real Part of Conductivity (s/m) = 0**

Click OK (Edit No.0 Substrate Layer)

Double Click on the No. 1 D substrate data
 Enter **Dielectric Constant, Epsr = 2.9**
 Enter **Top Surface, Ztop = .06**

Edit No.1 Substrate Layer

Comment

Top Surface, Ztop

0.06

Dielectric Constant, Epsr

2.9

Loss Tangent for Epsr, TanD(E)

-0

Permeability, Mur

1

Loss Tangent for Mur, TanD(M)

-0

Real Part of Conductivity (s/m)

0

Imag. Part of Conductivity (s/m)

0

Distance to No.0

0.06

Type

Normal

CAL Limit

1000000

Enclosure Index

No.0

Transparency

0.5

Distance to No.2

1.0000001e+015

Property

Dielectrics

Factor

2.9

Color

☒ Prompt users for merging multiple thin layers for simulation efficiency

Add Freq

Delete

Remove All

Import

Export

| Freq (GHz) | Epsr | TanD(E) | Mur | TanD(M) | Re(Sigma) | Im(Sigma) |
|------------|------|---------|-----|---------|-----------|-----------|
| | | | | | | |

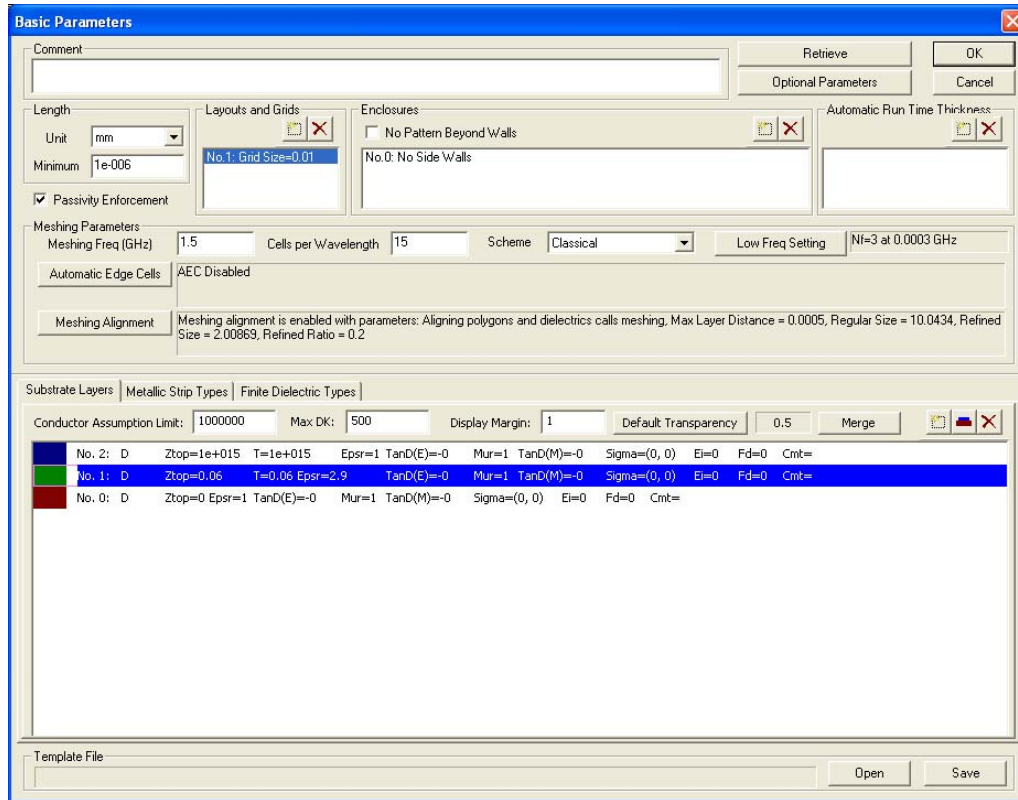
OK

Cancel

Click **OK** (Edit No.1 Substrate Layer)

The following shows the IE3D Basic Parameter Window with the Substrate Layer defined for this RFID tag design.

- Note, Layer No. 2 is at 1 e+15mm from the ground plane. This layer is added by IE3D when the design is saved.
- Notice the ground plane has a conductivity of 0,0 (i.e. ground plane not used for tag designs).



4. Metallic Strip Types

The conductor layer of the RFID tag is the electron path of the antenna that collects energy from the RF Field. It is typically made of either copper or aluminum but can also be of other conductors. For purposes of the initial design the Relative Dielectric Constant and Permeability are assumed to be “1”. The conductivity and thickness however need to be entered to reflect the design. To enter the properties, select the **Metallic Strip Types Tab** and enter the parameters as shown in the following table.

| Metallic Strip Type Parameters (Red entries are different from the default of a new design) | | | | | | | |
|---|-----------|------------------------------|-------------------------|-----------------------|---------------------------|------------------------------------|------------------------|
| | Thickness | Relative Dielectric Constant | Dielectric Loss Tangent | Relative Permeability | Permeability Loss Tangent | Conductivity Sigma Real, Imaginary | Comments |
| 1 | .005 | 1 | 0 | 1 | 0 | 4.9e+007 | Copper, default values |

The following shows the IE3D Basic Parameter Window with the Metallic Strip Types defined for a particular RFID tag design. Notice the conductivity is the default value for copper.

Basic Parameters

Comment:

Retrieve OK

Optional Parameters Cancel

Length: Unit: Minimum:

Layouts and Grids: No. 1: Grid Size=0.01

Enclosures: ☐ No Pattern Beyond Walls No. 0: No Side Walls

Automatic Run Time Thickness:

☒ Passivity Enforcement

Meshing Parameters: Meshing Freq (GHz): Cells per Wavelength: Scheme: Low Freq Setting:

Automatic Edge Cells: AEC Disabled

Meshing Alignment: Meshing alignment is enabled with parameters: Aligning polygons and dielectrics calls meshing. Max Layer Distance = 0.0005, Regular Size = 10.0434, Refined Size = 2.00869, Refined Ratio = 0.2

Substrate Layers: **Metallic Strip Types** Finite Dielectric Types

Non-Isotropic Metallic Types as Defined. Merge Identical Select/DeSelect All Batch Change

| No. | tk | Epsr | TanD(E) | Mur | TanD(M) | Sigma | Rough | Zs | Fd | Cmt |
|--------|----------|--------|-----------|-------|-----------|---------------------|---------|---------------|------|---------------|
| No. 1: | tk=0.005 | Epsr=1 | TanD(E)=0 | Mur=1 | TanD(M)=0 | Sigma=(4.9e+007, 0) | Rough=0 | Zs=0.00408163 | Fd=0 | Cmt=_derived0 |

Template File: Open Save

Exiting the Basic Parameter Window

To Exit the Basic Parameter Window and start the design accomplish the following:

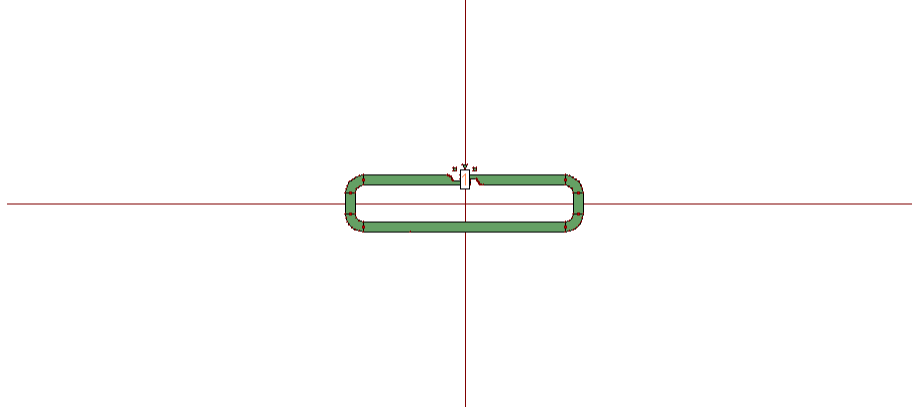
1. Select **“OK”** to accept the Basic Parameters
2. Select **“File”** and **“Save As” Design Example** to enable M-Grid

Initial Design Layout

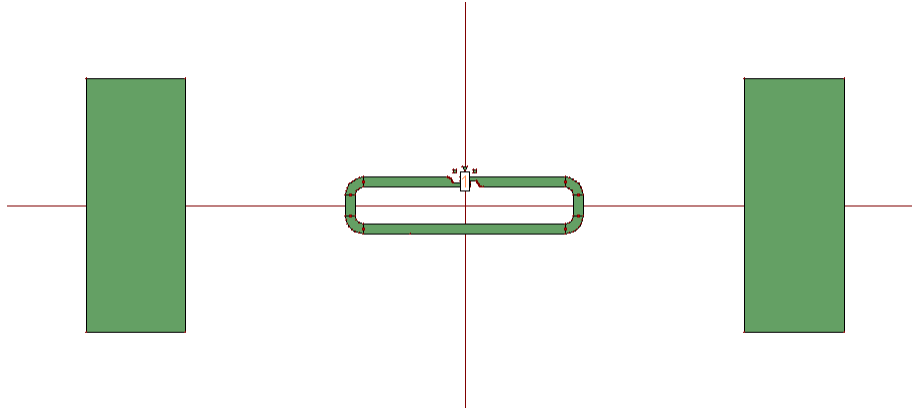
The initial dipole can be laid out with M-Grid (Mentor Graphics' CAD Package) or with Auto Cad as a DXF file and then imported via IE3D. It can also be any external CAD program supported by ADIX. The following is a suggested sequence for laying out the initial tag geometry. If the user chooses to use the M-Grid package, Appendix C outlines the exact key strokes for this approach.

Initial Loop Design

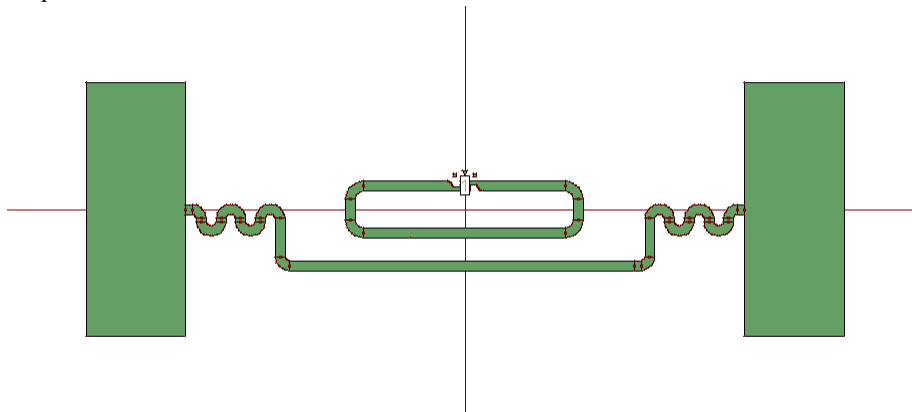
1. Convert one of the reference loop DXF files into the appropriate format.



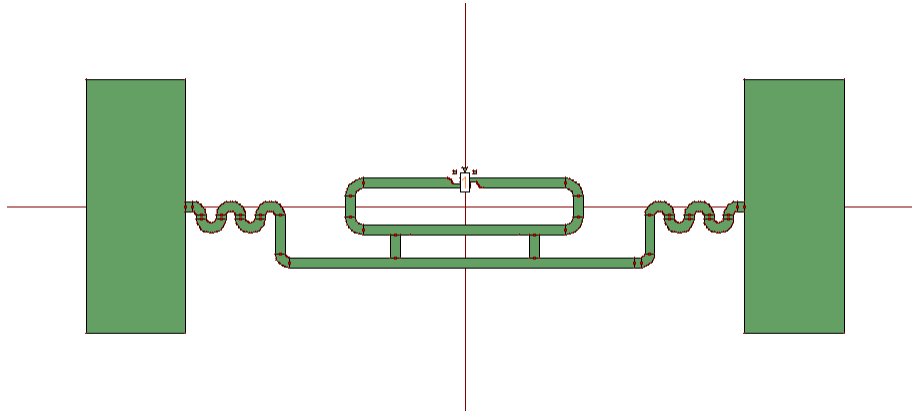
2. Add Capacitance Plates (10mm x 25.4mm) to each end of the proposed design with the outer extremes of the plates at the specified 76.2mm



3. Create a Meandered Dipole that runs from the middle of the capacitance plates to the just under the loop.



4. Connect the loop to the dipole as shown.

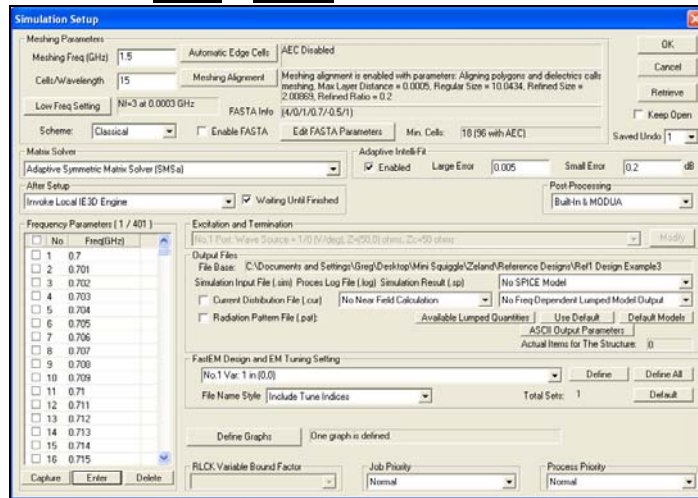


5. Import the file into IE3D as a GEO file.
6. Continue with the tag design at the next section

Tag Optimization

1. Simulation of “Design Example.geo”

Select **Process --- Simulate**



Select **OK** (Simulate)

2. Adjust Meandering Inductance

Increase Inductance

Select **Open --- Initial Design Example**

Select **Edit --- Select Vertices** ALT-S

Select **Left side of top half of the meandered loops** (as shown in example)

Select **Right side of top half of the meandered loops**

Select **Edit --- Move Objects** SHFT-M

Left Click Mouse

Enter **X-Position = 0** and **Y-Position = +2**

Select **OK** (Move Object Offsets to Original)

Select **File --- Save As --- Initial+M**

Select **Process --- Simulate**

Select **OK** (Simulation Setup) Step #1 for Screen Image

Reduce Inductance

Select **Open --- Initial Design Example**

Select **Edit --- Select Vertices** ALT-S

Select **Left side of top half of the meandered loops** (as shown in example)

Select **Right side of top half of the meandered loops**

Select **Edit --- Move Objects** SHFT-M

Left Click Mouse

Enter **X-Position = 0** and **Y-Position = -2**

Select **OK** (Move Object Offsets to Original)

Select **File --- Save As --- Initial-M**

Select **Process --- Simulate**

Select **OK** (Simulation Setup) Step #1 for Screen Image

3. Adjust Coupling Points

Tighten Coupling

Select **Open --- Initial Design Example**

Select **Edit --- Select Vertices** ALT-S

Select **Left Side Vertical Coupling Trace** (as shown in example)

Select **Edit --- Move Objects** SHFT-M

Left Click Mouse

Enter **X-Position = -1** and **Y-Position = 0**

Select **OK** (Move Object Offsets to Original)

Select **Right Side Vertical Coupling Trace** (as shown in example)

Select **Edit --- Move Objects** SHFT-M

Left Click Mouse

Enter **X-Position = 1** and **Y-Position = 0**

| | | |
|--------|--------------------------------------|--------------------------|
| Select | OK (Move Object Offsets to Original) | |
| Select | File --- Save As --- Initial+C | |
| Select | Process --- Simulate | Step #1 for Screen Image |
| Select | OK (Simulation Setup) | |

Loosen Coupling

| | | |
|------------------|---|--------------------------|
| Select | Open --- Initial Design Example | |
| Select | Edit --- Select Vertices | ALT-S |
| Select | Left Side Vertical Coupling Trace (as shown in example) | |
| Select | Edit --- Move Objects | SHFT-M |
| Left Click Mouse | | |
| Enter | X-Position = 1 and Y-Position = 0 | |
| Select | OK (Move Object Offsets to Original) | |
| Select | Right Side Vertical Coupling Trace (as shown in example) | |
| Select | Edit --- Move Objects | SHFT-M |
| Left Click Mouse | | |
| Enter | X-Position = -1 and Y-Position = 0 | |
| Select | OK (Move Object Offsets to Original) | |
| Select | File --- Save As --- Initial-C | |
| Select | Process --- Simulate | Step #1 for Screen Image |
| Select | OK (Simulation Setup) | |

4. Adjust Loop Inductance

Increase Loop Inductance

| | | |
|------------------|---|--------------------------|
| Select | Open --- Initial Design Example | |
| Select | Edit --- Select Vertices | ALT-S |
| Select | top half of the loop (as shown in example) | |
| Select | Edit --- Move Objects | SHFT-M |
| Left Click Mouse | | |
| Enter | X-Position = 0 and Y-Position = .5 | |
| Select | OK (Move Object Offsets to Original) | |
| Select | File --- Save As --- Initial+L | |
| Select | Process --- Simulate | Step #1 for Screen Image |
| Select | OK (Simulation Setup) | |

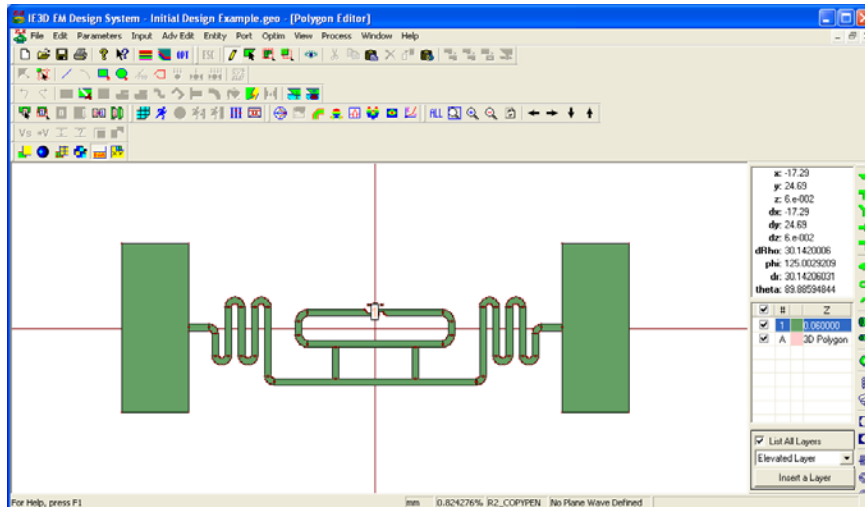
Reduce loop Inductance

| | | |
|------------------|---|--------------------------|
| Select | Open --- Initial Design Example | |
| Select | Edit --- Select Vertices | ALT-S |
| Select | top half of the loop (as shown in example) | |
| Select | Edit --- Move Objects | SHFT-M |
| Left Click Mouse | | |
| Enter | X-Position = 0 and Y-Position = -.5 | |
| Select | OK (Move Object Offsets to Original) | |
| Select | File --- Save As --- Initial-L | |
| Select | Process --- Simulate | Step #1 for Screen Image |
| Select | OK (Simulation Setup) | |

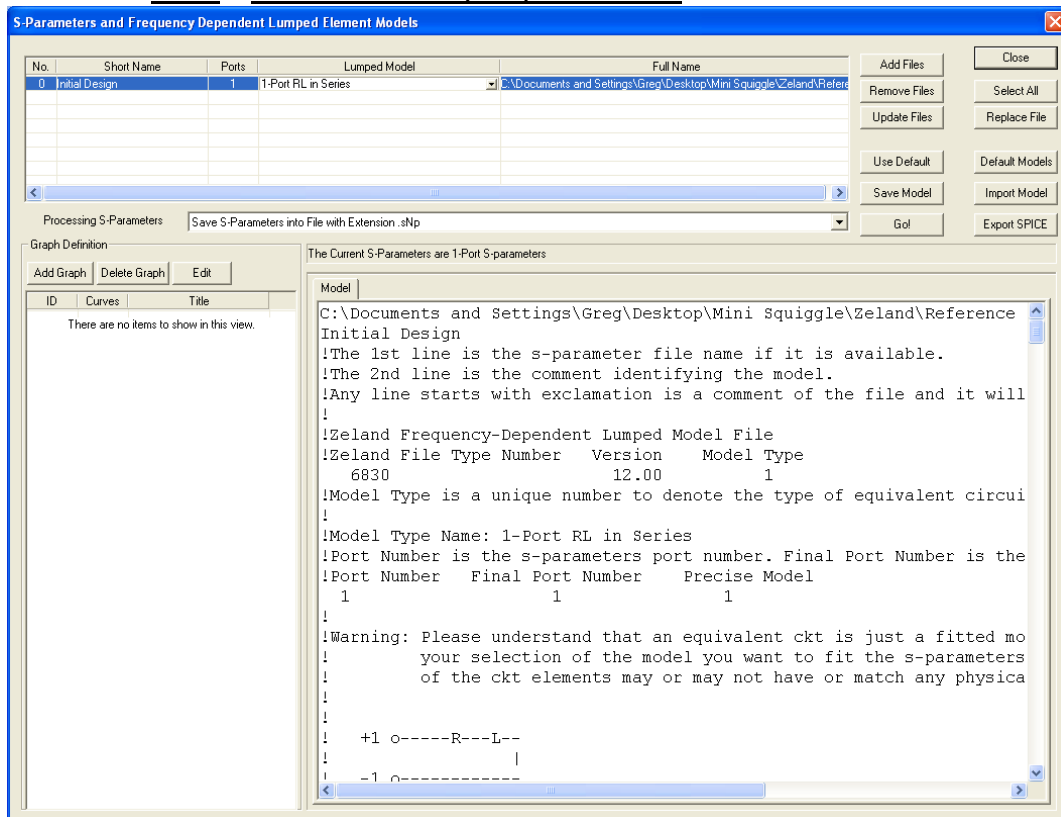
5. Conjugate Match Factor

Open Design Variation Files

| | |
|--------|---|
| Select | File --- Open --- Initial Design Example.geo |
|--------|---|



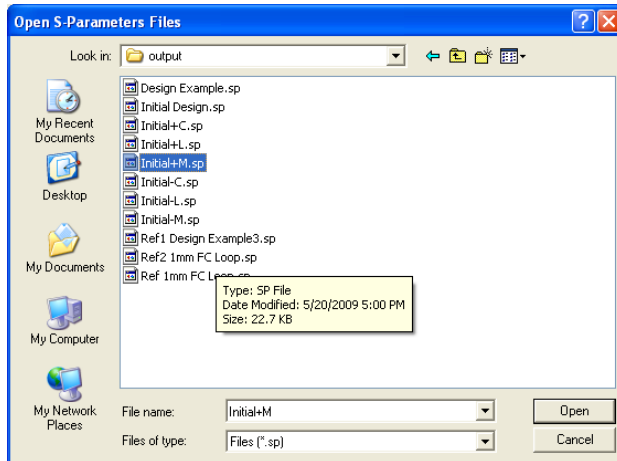
Select **Process --- S-Parameters and Lumped Equivalent Circuits**



Click On Space under **“Short Name”**

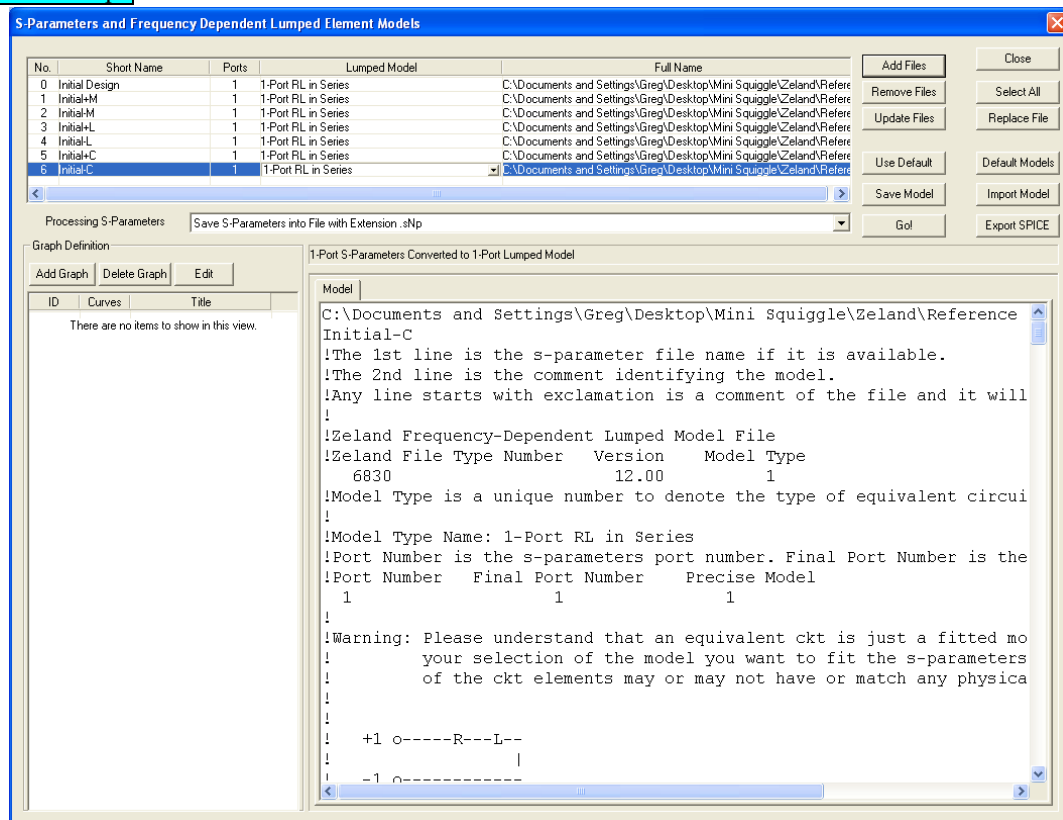
Enter **Initial Design**

Click **Add Files**



| | |
|-------|--|
| Enter | Initial+M.sp --- OPEN (Open S Parameter Files) |
| Click | Add Files |
| Enter | Initial-M.sp --- OPEN (Open S Parameter Files) |
| Click | Add Files |
| Enter | Initial+L.sp --- OPEN (Open S Parameter Files) |
| Click | Add Files |
| Enter | Initial-L.sp --- OPEN (Open S Parameter Files) |
| Click | Add Files |
| Enter | Initial+C.sp --- OPEN (Open S Parameter Files) |
| Click | Add Files |
| Enter | Initial-C.sp --- OPEN (Open S Parameter Files) |

Define Graph



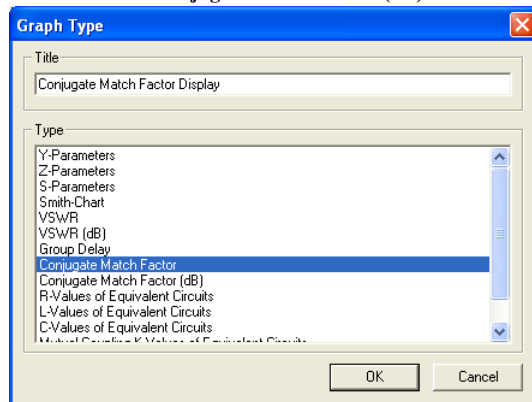
Click

ADD GRAPH

Plot 0

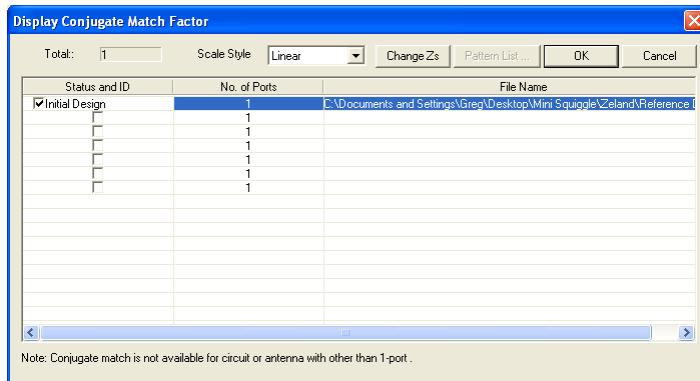
Select

Conjugate Match Factor (dB)

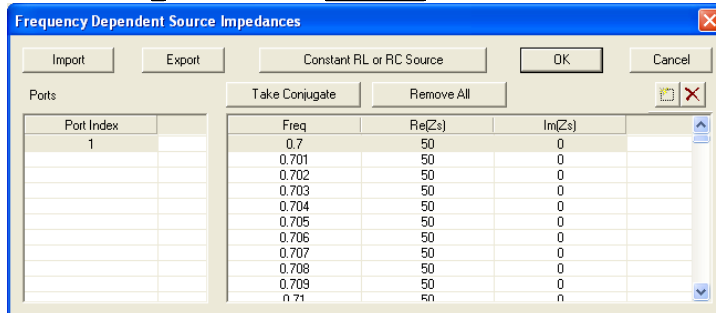


Select

OK (Graph Type)

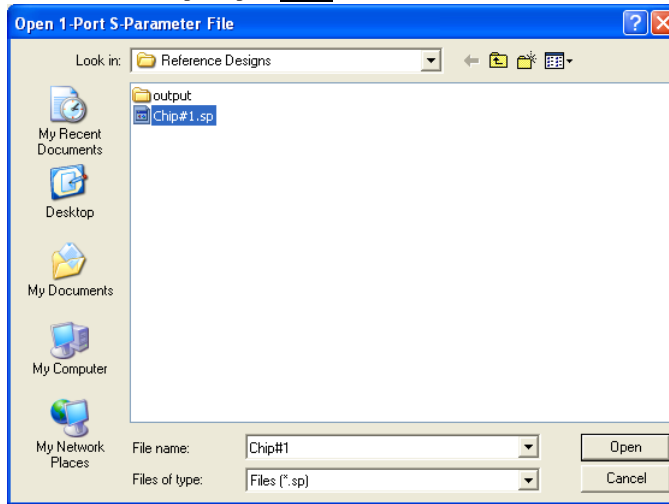


Check ☒ Initial Design --- ☐ Change Zs Initial Design Plot

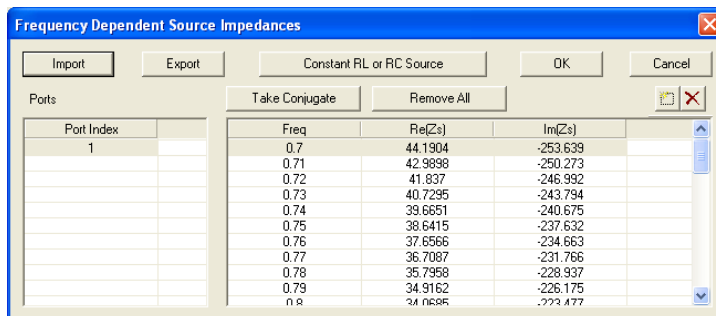


Select **Import**

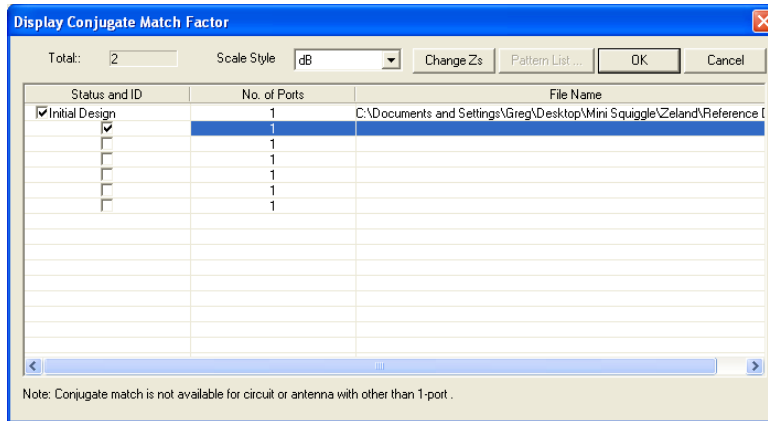
Select **Chip #1.sp** --- **Open** Attach chip parameters



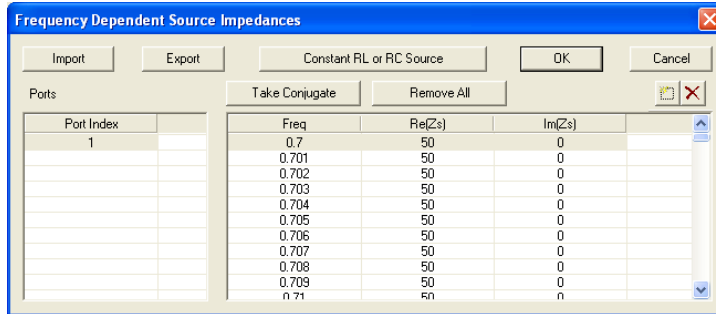
Select **Open** (Open 1=Port S-Parameter Designs



Select

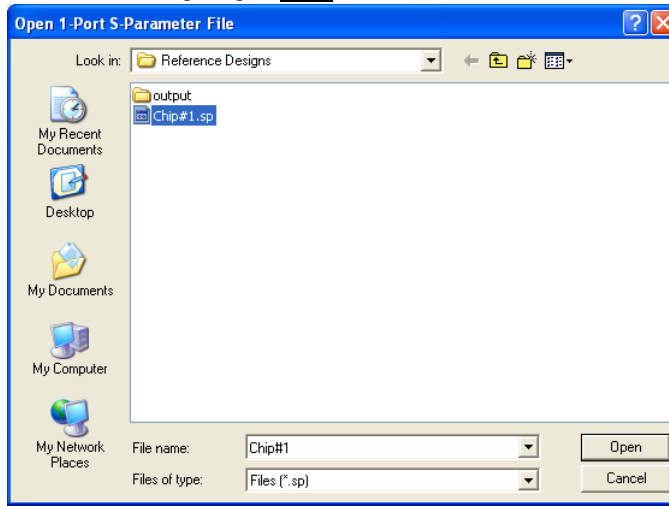


Check **Design Modification #1 --- Change Zs** Initial+M Plot



Select **Import**

Select **Chip #1.sp --- Open** Attach chip parameters



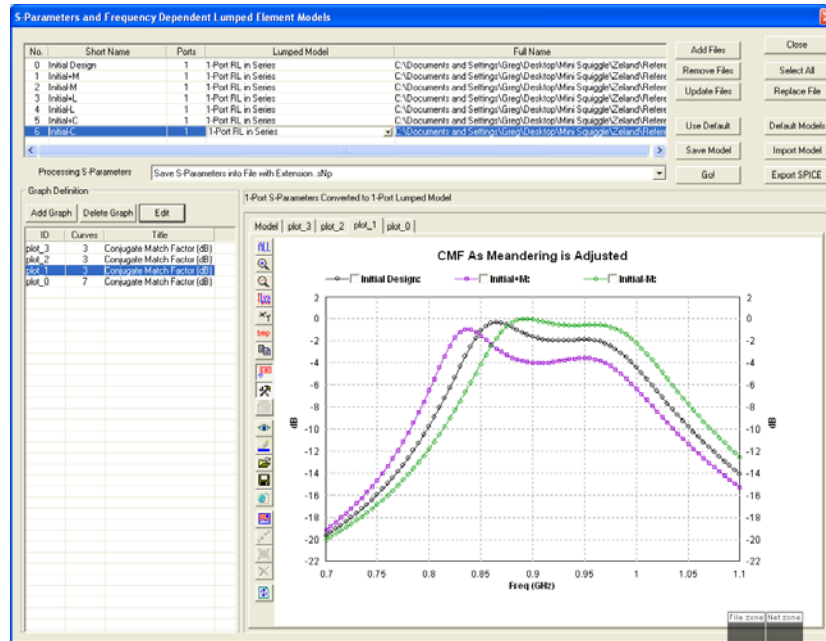
Select **OK**

| | | |
|--------|---|------------------------|
| Check | Design Modification #2 --- Change Zs | Initial-M Plot |
| Select | Import | |
| Select | Chip #1.sp --- Open | Attach chip parameters |
| Select | OK | |
| Check | Design Modification #3 --- Change Zs | Initial+L Plot |
| Select | Import | |
| Select | Chip #1.sp --- Open | Attach chip parameters |
| Select | OK | |
| Check | Design Modification #4 --- Change Zs | Initial-L Plot |
| Select | Import | |

| | | |
|--------|--|---------------------------------|
| Select | Chip #1.sp --- Open | Attach chip parameters |
| Select | OK | |
| Check | Design Modification #5 --- Change Zs | Initial+C Plot |
| Select | Import | |
| Select | Chip #1.sp --- Open | Attach chip parameters |
| Select | OK | |
| Check | Design Modification #6 --- Change Zs | Initial-C Plot |
| Select | Import | |
| Select | Chip #1.sp --- Open | Attach chip parameters |
| Select | OK | |
| Select | OK (Display Conjugate Match Factor) | |
| Select | plot 0 | All Data on plot_0 |
| Click | ADD GRAPH | plot_1 |
| Select | Conjugate Match Factor (dB) | |
| Select | OK (Graph Type) | |
| Select | Initial Design and the First Two Alt Designs | |
| Select | OK (Display Conjugate Match Factor) | |
| Select | plot 1 | Initial Design and +/- Meander |
| Click | ADD GRAPH | Plot 2 |
| Select | Conjugate Match Factor (dB) | |
| Select | OK (Graph Type) | |
| Select | Initial Design and the Second Two Alt Designs | |
| Select | OK (Display Conjugate Match Factor) | |
| Select | plot 2 | Initial Design and +/- Loops |
| Click | ADD GRAPH | Plot 3 |
| Select | Conjugate Match Factor (dB) | |
| Select | OK (Graph Type) | |
| Select | Initial Design and the Second Two Alt Designs | |
| Select | OK (Display Conjugate Match Factor) | |
| Select | plot 2 | Initial Design and +/- Coupling |

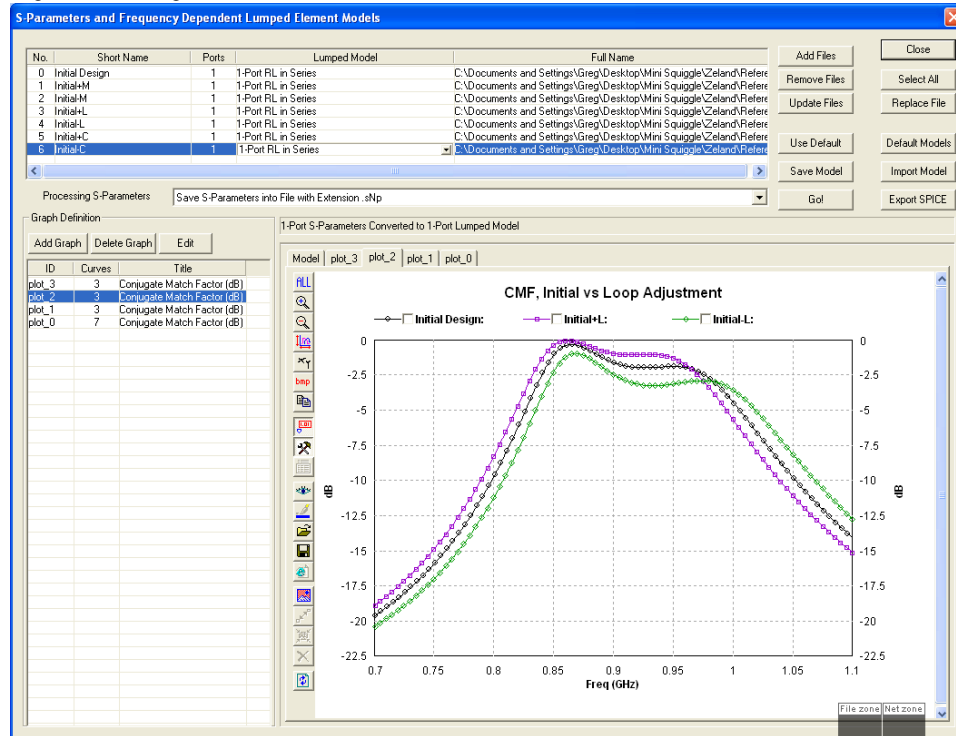
Meandering Adjustment

The graph below shows the effect of adjusting the Meandering inductance of the tag. Observe that the primary effect is frequency shift of the low frequency resonance. Also note that even though the frequency-shift of the higher resonance is less, its amplitude is affected more. In general it can be stated that meandering inductance adds effective length to the tag. As such more inductance will move the resonance of the dipole to a lower center frequency. The effects on the higher frequency resonance are a result of the mutual coupling between the dipole and loop.



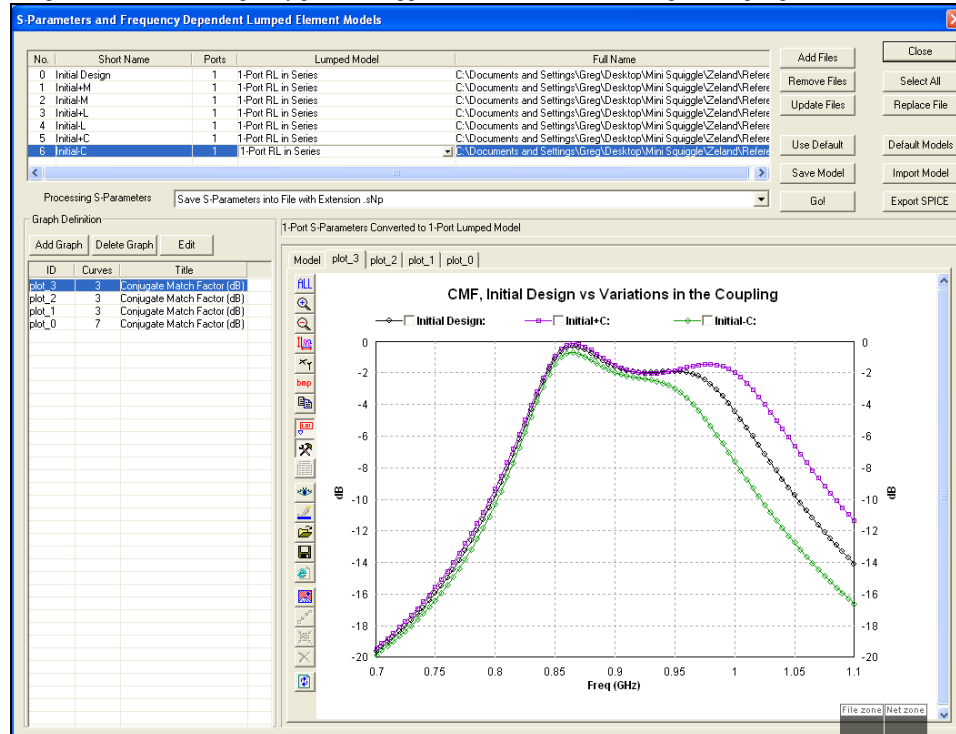
Loop Adjustment

The graph below shows the effect of adjusting the resonating loop inductance, of the tag. Observe that the primary effect is movement of the high frequency resonance with a much smaller effect upon the low frequency pole. Also notice however, the amplitude effects upon both resonances.



Coupling Points

The graph below shows the effect of adjusting the coupling between the dipole and the resonating loop of the tag. Observe that the primary effect is bandwidth. Increasing the coupling reduces the bandwidth by moving the high frequency resonance independent of the low frequency pole. The opposite is also true as decreasing the coupling increases the bandwidth..

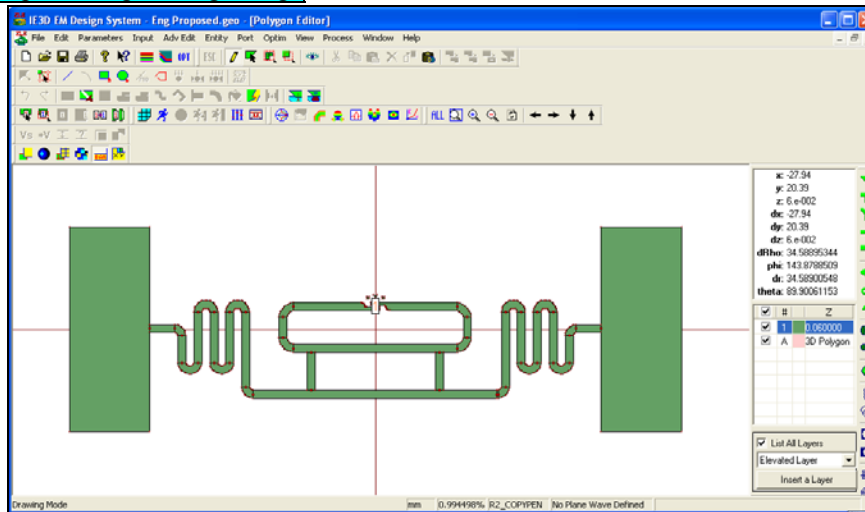


6. Optimize to Engineering Requirements

From the tag design variations it is observed that the flattest free space design is the Initial-M. This design is flat across the band to within .5dB. The bandwidth however is only ~90MHz. From the engineering requirements we are looking for ~150MHz so it is clear that we need more bandwidth. To obtain adequate bandwidth the coupling needs to be altered. As such the Initial+C design is selected as a starting point for this design.

Starting from the Initial+C design the meandering can be adjusted to position the low frequency resonance to the low frequency requirements as stated in the product specification, 860MHz. The loop size can then be adjusted to balance the resonant peaks. Following this process, the design below was achieved.

Proposed Engineering Design

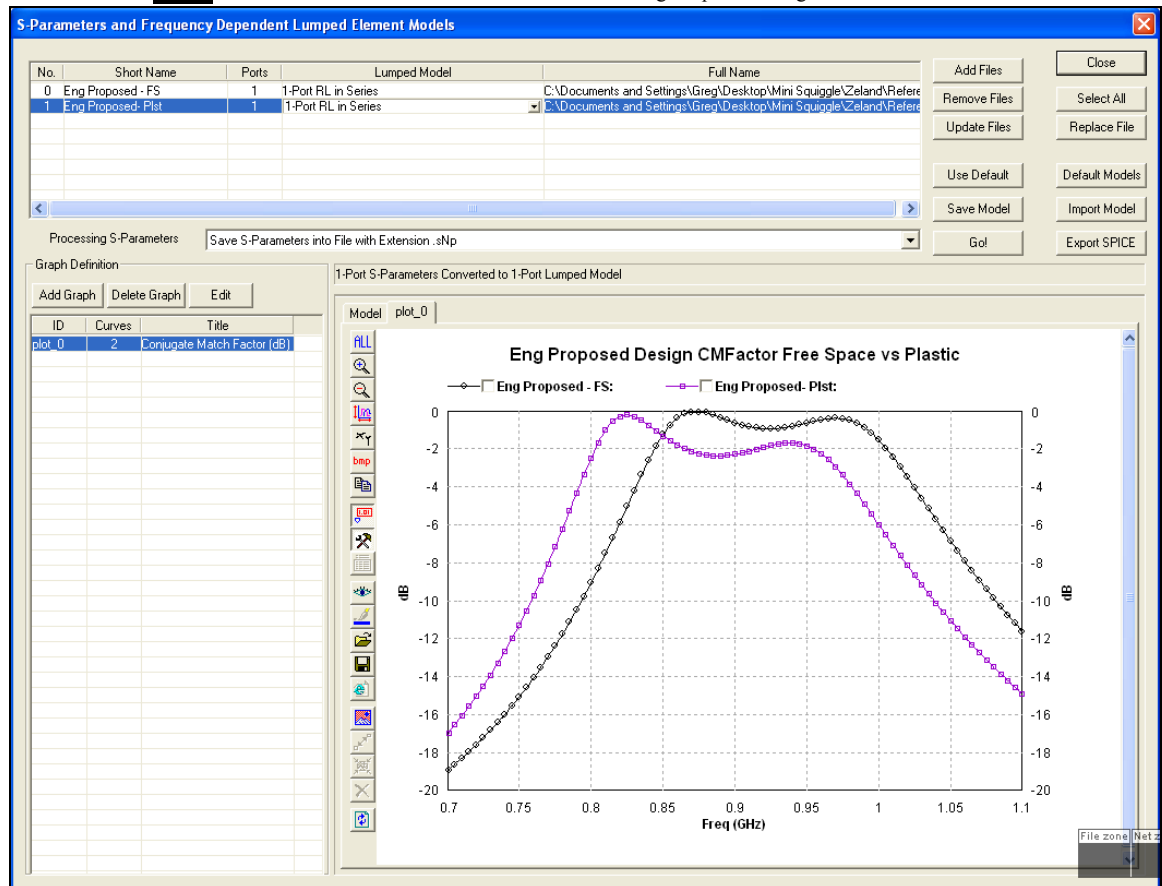


Simulation, Proposed Engineering Design

- | | | |
|-----------|--|------------------------------------|
| Select | File --- Open | CTR-O |
| Select | Eng Proposed Design.geo --- OPEN | |
| Select | Process --- Simulate --- OK (Simulation Setup) | |
| Select | File --- Save As --- Eng Proposed Design.geo | |
| Select | Parameters --- Basic Parameters | |
| Dbl Click | No 1. D (Substrate Layer) | |
| Enter | Top Surface Ztop = 1.06 | 1mm for bottle + .06 for substrate |
| Click | OK (Basic Parameters) | |
| Select | Edit --- Select All --- Polygons | |
| Edit | Change Z-Coordinate | SHFT-Z |
| Enter | New Z-Coordinate = 1.06 | |
| Click | OK (Change Z-Coordinates of the Selected Objects) | |
| File | Save As --- Eng Proposed-P.geo | |

Frequency Response Plots, Proposed Engineering Design

Select **File --- Open** CTR-O
 Select **Eng Proposed Design.geo --- OPEN**
 Select **Process --- S-Parameter and lumped Equivalent Circuit**
 Dbl Click **Space below Short Name**
 Enter **Eng Proposed - FS**
 Click **Add Files**
 Enter **Eng Proposed - P.sp**
 Select **Open**
 Dbl Click **Second Space below Short Name**
 Enter **Eng Proposed - Plst**
 Click **ADD GRAPH** plot_0
 Select **Conjugate Match Factor (dB)**
 Select **OK** (Graph Type)
 Select **Eng Proposed -FS and the Eng Proposed - Plst**
 Select **Import**
 Select **Chip #1.sp --- Open** Attach chip parameters
 Select **OK**
 Select **OK** (Display Conjugate Match Factor)
 Select **plot_0** Eng Proposed Design FS & Plst



Compliance Matrix, Proposed Engineering Design

| | BW MHz | Max Turn On Mismatch over F.S. BW (dB) | Max Turn On Variation over F.S. BW (dB) | Max Turn On Mismatch over On Plastic BW (dB) | Max Turn On Variation over On Plastic BW (dB) | Max Turn On Delta FS to Plastic (dB) |
|---------------------|------------|---|--|---|---|---|
| Simulation | 150 | -1 | -1 | -2.4 | -2.3 | -2.4 |
| Eng Requirements | 150 | -6 | -3 | -6 | -3 | -3 |

Tag Qualification

Compliance Matrix

The following parameters meet / fail specification as shown:

| <i>Parameter</i> | <i>Specification</i> | <i>Pass</i> | <i>Fail</i> | <i>Comments</i> |
|---------------------------------|------------------------|-------------|-------------|-----------------------------------|
| • Size | 25.4 mm x 76.2mm | ✓ | | by design |
| • Flatness | less than 5microns | ✓ | | by FC design |
| • Copper Thickness | .005mm | ✓ | | by process |
| • Trace Width | 1mm | ✓ | | by design |
| • Trace Composition | Copper | ✓ | | by process |
| • Trace Conductivity | 4.7 e7 | ✓ | | by definition |
| • Substrate Thickness | .06mm | ✓ | | by process |
| • IC (Rp=1500Ω Cp=.87pF) | Company #1 | | ✓ | by design |
| • Relative Permeability | 1 | ✓ | | by definition |
| • Loss Tangent | 0 | ✓ | | by definition |
| • Relative Dielectric Constants | | | | |
| Plastic | 2.9 | ✓ | | by definition, 1mm |
| Corrugate | 1.2 | ✓ | | by definition, 3.2mm |
| Substrate | 2.9 | ✓ | | by definition, .06mm |
| • Polarity of Operation | Vertical | ✓ | | by application process |
| • Application | FS, Corrugate, Plastic | ✓ | | by design |
| • Operational Frequencies | US, Europe, China | ✓ | | per Eng Requirement Acceptance |
| • Read Range | 2 meters minimum | ✓ | | 3.0 meters, see Below for details |
| • Back Scatter | NA | ✓ | | See Below for details |

Read Range

The read range as specified in the marketing document is the measurement of the distance that the tag can be read with a RFID reader. There is no industry standard definition for read range but in later years it is starting to become accepted that read range is the distance where a tag responds to most of the frequencies in the band rather than at a point where is only responds to a few.

To further complicate the read range issue, it can be seen that read range is a system parameter rather than a tag specification. If however, we calculate read range based upon a Substitution Method using Turn-On-Sensitivity (dB) relative to a characterized Golden Reference Tag we can quantify a fairly reproducible metric of read range.

Given $RR = R_{REF} * 10^{\Delta dB/20}$
 And the Golden Ref Characteristics RR = 4 meters
 From Substitution we get 2 meters = 4 meter * $10^{\Delta dB/20}$
 Division yields $(2/4) = 10^{\Delta dB/20}$
 Log of both sides $\text{Log}_{10} (2/4) = \Delta dB/20$
 Multiplication yields $20 * \text{Log}_{10} (2/4) = \Delta dB$
 Subtraction yields $\Delta dB = 20 * \text{Log}_{10} (2/4) = 6dB$
 So for 2 meters the Design Example Tag must be within 6dB of the Golden Reference

So to verify read range we can plot the golden reference CMF vs. Frequency and compare at the frequencies of concern to the Design Example for both in Free Space and on Plastic.

Select **File --- Open** CTR-O
 Select **Golden Ref.geo --- OPEN**
 Select **Process --- Simulate**
 Select **File --- Save --- Golden Ref.geo**
 Select **Process --- S-Parameter and lumped Equivalent Circuit**
 Dbl Click **Space below Short Name**
 Enter **Golden Ref - FS**
 Click **Add Files**
 Enter **Eng Proposed.sp and Eng Proposed-P.sp**
 Select **Open**
 Dbl Click **Second Space below Short Name**
 Enter **Eng Proposed - FS**
 Dbl Click **Third Space below Short Name**
 Enter **Eng Proposed - Plst**
 Click **ADD GRAPH** plot_0
 Select **Conjugate Match Factor (dB)**
 Select **OK** (Graph Type)
 Select **Golden Ref - Eng Proposed -FS and the Eng Proposed - Plst**
 Select **Import**
 Select **Chip #1.sp --- Open** Attach chip parameters

Select
Select
Select

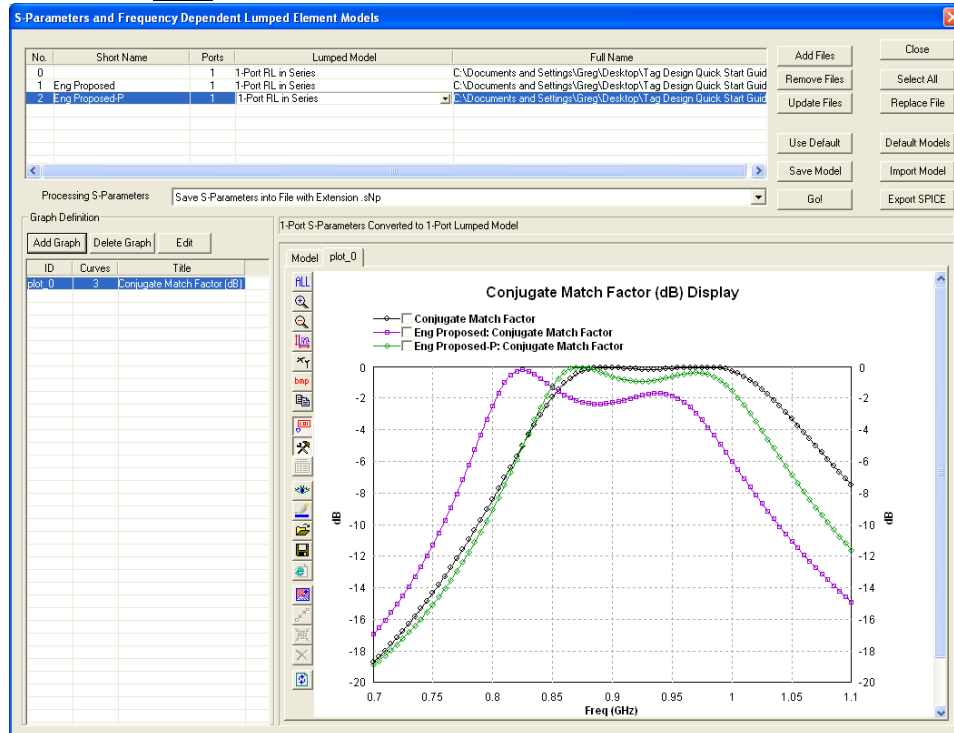
OK

OK

plot 0

(Display Conjugate Match Factor)

Eng Proposed Design FS & Plst



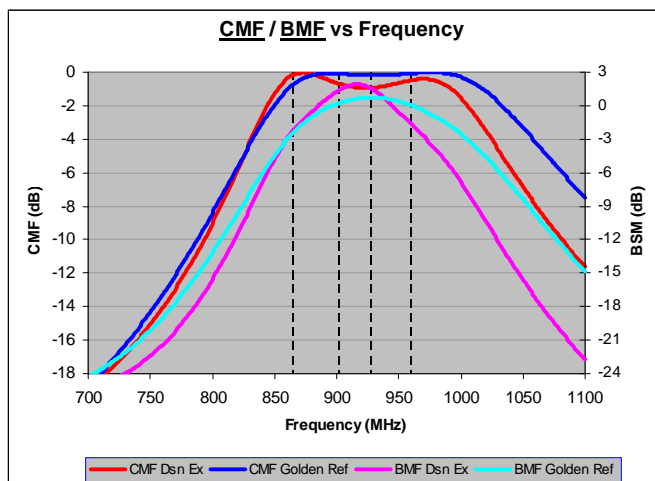
As can be observed from the results of the following plots, the Design Example is in the worst case 2.5 dB below the Free Space CMF of the Golden Reference Tag. As such we can calculate the read range as follows:

$$RR = 4 \text{ meters} * 10^{(27.5-30) \text{ dB}/20}$$

$$RR \text{ (Design Example)} = 3.0 \text{ meters}$$

Backscatter

Backscatter was not specified in the requirements for this design. IE3D however, incorporates a new module to help predict the tag backscatter (*see appendix B*). The following plot shows the backscatter along with the Conjugate Match Factor of the Design Example and the Golden Reference. As can be seen the backscatter bandwidth does not track the CMF bandwidth. In these two designs the backscatter BW is centered about the CMF bandwidth. This is the optimal situation for a RFID tag design. From these curves it should become clear that backscatter considerations are needed along with sensitivity to properly design a RFID tag.

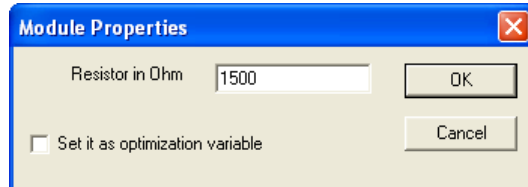


Appendix A

RFID Tag Design, IC Modeling using Modua

Enter Parallel Resistance

Open **Zealand Program Manager**
Dbl Click on **Modua**
Select **Element --- Resistor**

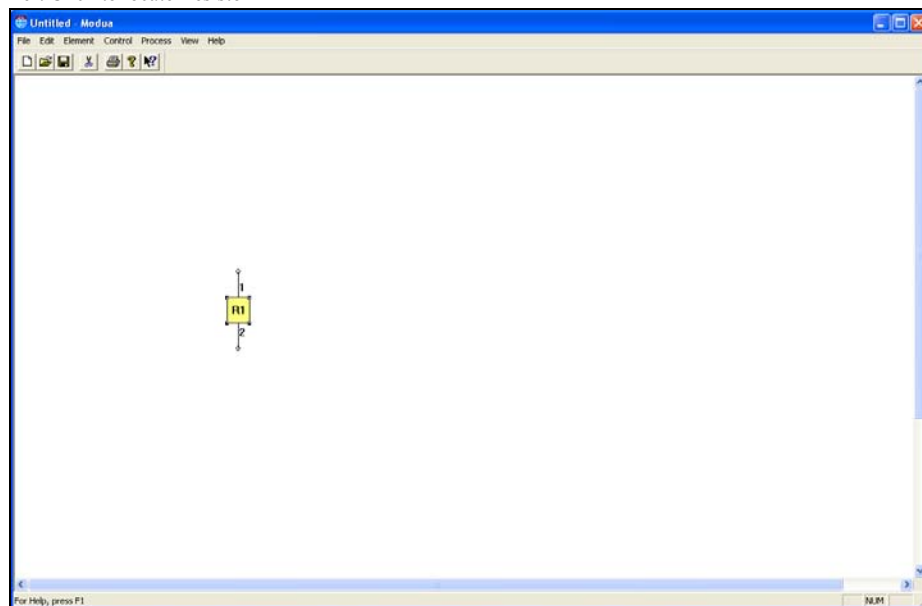


Enter --- 1500

Click OK

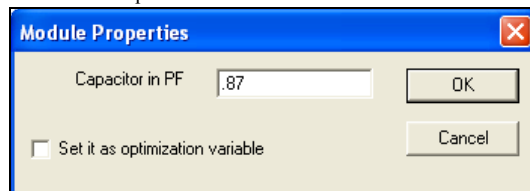
Place R1 as shown

Left Click to locate Resistor



Click away from R1 to deselect

Element --- Capacitor

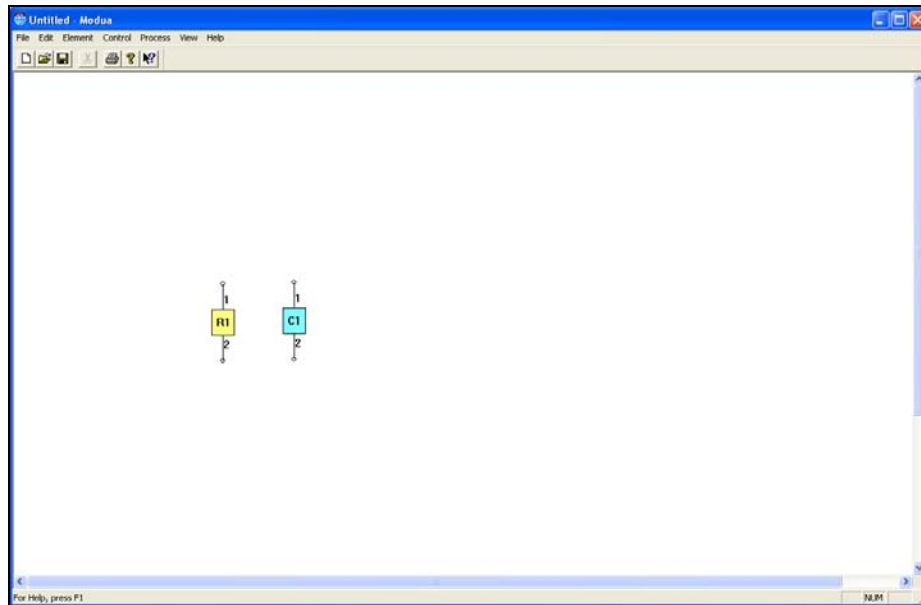


Enter --- .87

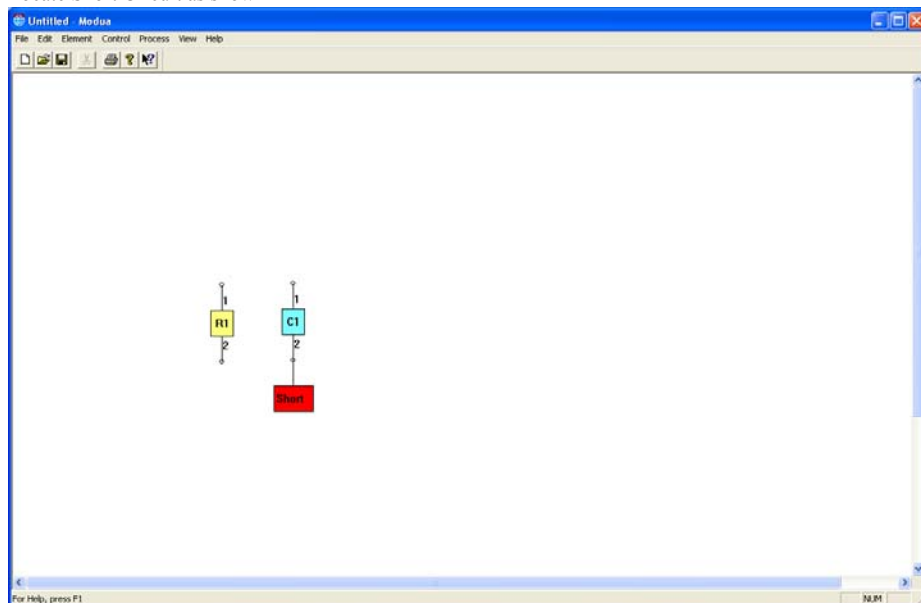
Click OK

Place C1 as shown

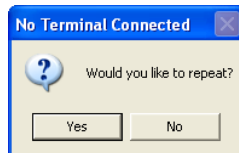
Left Click Mouse to locate Capacitor



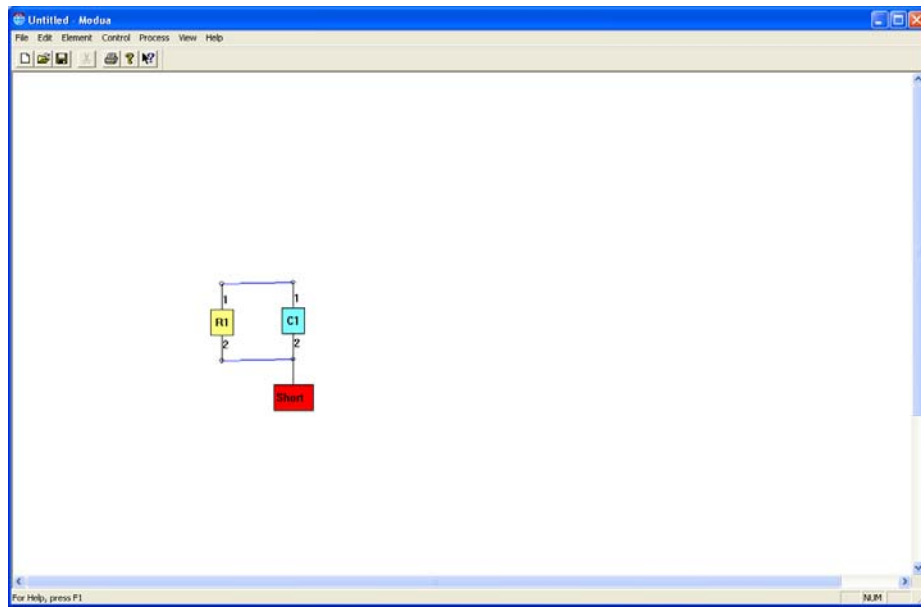
Click away from C1 to deselect
 Element --- Short Circuit
 Locate Short Circuit as shown



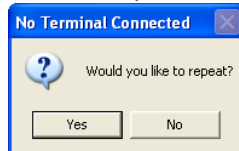
Left Click to locate Short Circuit



Click No
 Element --- Connection
 Left Click top of R1
 Left Click top of C1
 Left Click bottom of R1
 Left Click bottom of C1



Left Click away from network



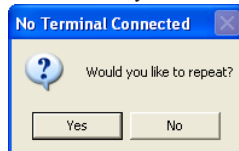
Click No

Element --- Port

Right Click to Position Port Orientation as shown

Left Click to Locate Port

Left Click away from Network to deselect



Click No

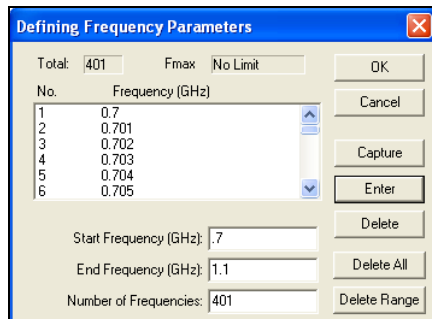
Process --- Simulate

Enter --- Start Frequency = .7

Enter --- Stop Frequency = 1.1

Enter --- Number of Frequencies = 401

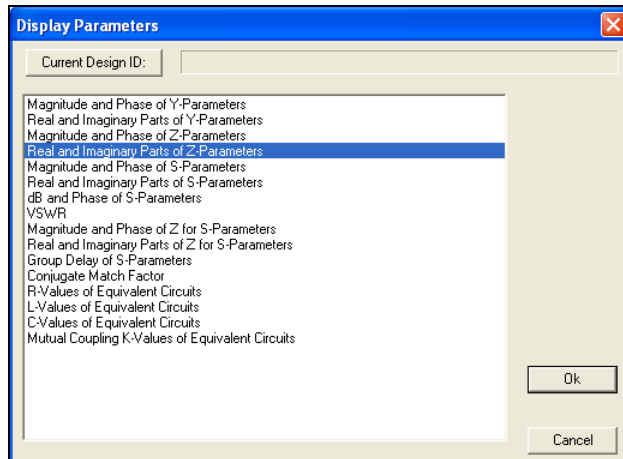
Select Enter



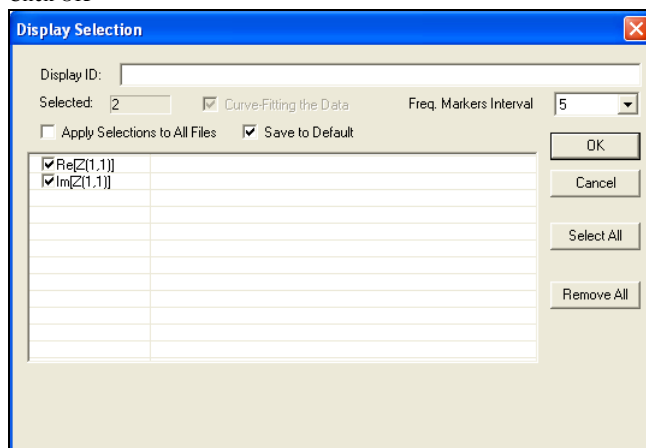
Select OK

Control --- Define Display Data

Click --- Real and Imaginary Parts of Z-Parameters



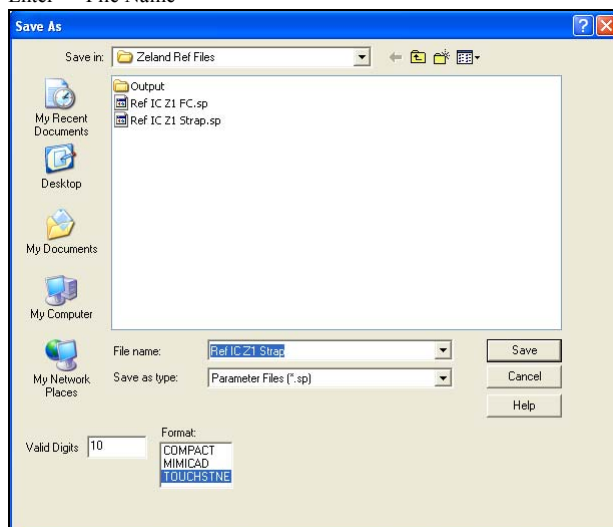
Click OK



Click OK

File --- Save S-Parameters

Enter --- File Name



Select Save

Close Modua

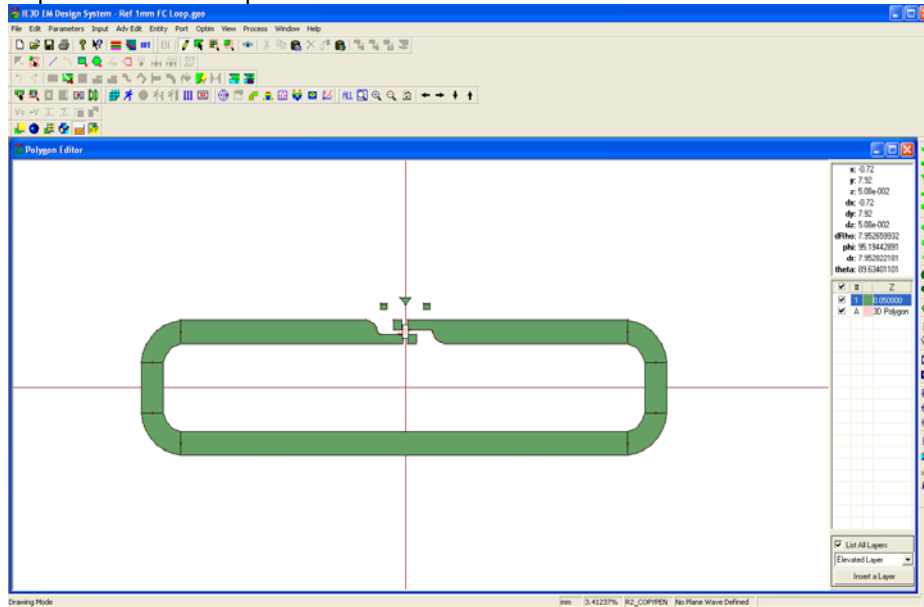
Appendix B
RFID Tag Design, Back Scatter Module

Appendix C

RFID Tag Design, Layout using M-Grid

Initial Loop Design

1. Import Reference Loop



Copy “Ref 1mm Loop FC.geo” file

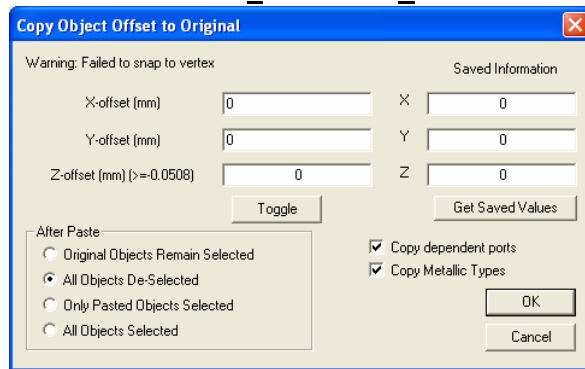
Select **File** --- **Open** then select **Ref 1mm Loop FC.geo**
Select **Edit** --- **Select All** --- **Polygons**
Select **Edit** --- **Copy**

CTR-C

Save “Ref 1mm Loop FC.geo” file to Design Example.geo file

Select **File** --- **Open** then select **Design Example.geo**
Select **Edit** --- **Paste**
Enter **X Offset = 0** and **Y Offset = 0**

CTR-V



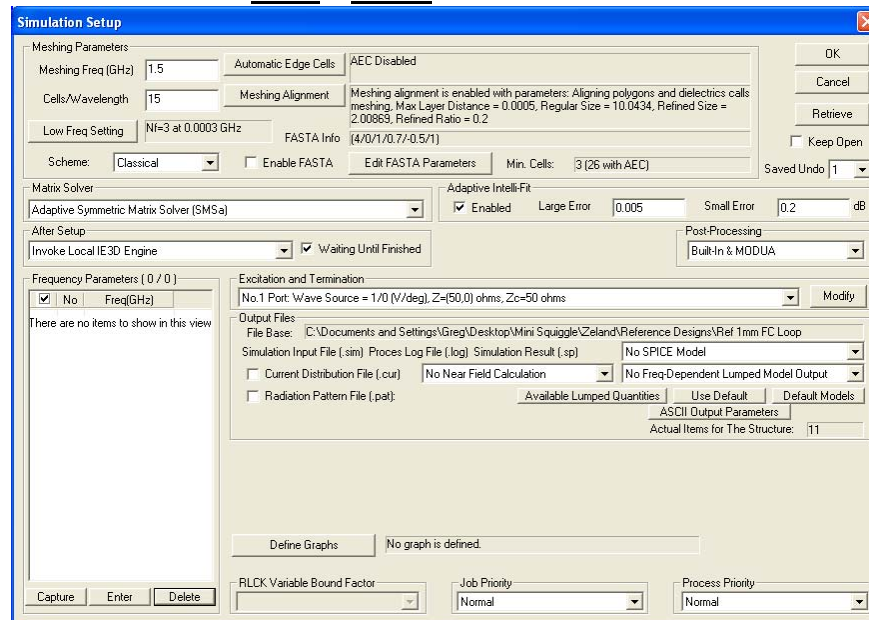
Select **OK** (Copy Object Offset to Original)
Select **ALL** to view the entire structure
Select **File** --- **Save** (Design Example.geo)

2. Simulation of “Design Example.geo”

Start Simulation

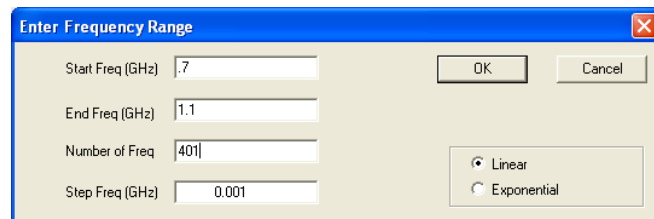
Select

Process --- Simulate



Select

Enter (Frequencies)



Input **Start Freq (GHz) = .7 --- End Freq (GHz) = 1.1 --- Number of Freq = 401**
 Select **OK** (Enter Frequency Range) --- **OK** (Start Simulation)

Apply IC Electrical Parameters

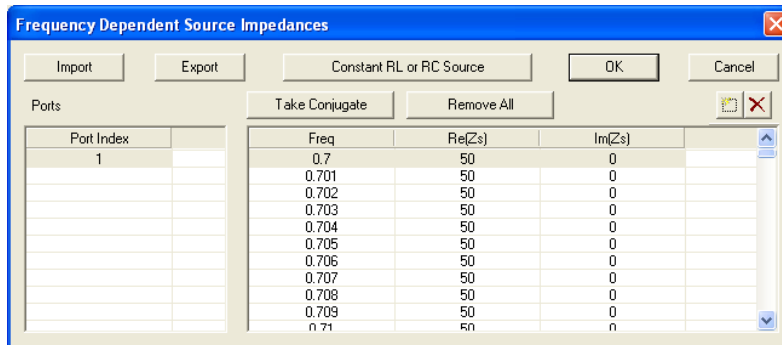
The simulation excites the geometry with a 50 ohm source. The following post process attaches a conversion file (**Ref IC Z1 FC.sp**) to the simulation that converts the 50 ohm source to the proper impedances that reflects the particular IC that is used. See Appendix QS-RFID TAG-A for additional information about creating this file.

Select

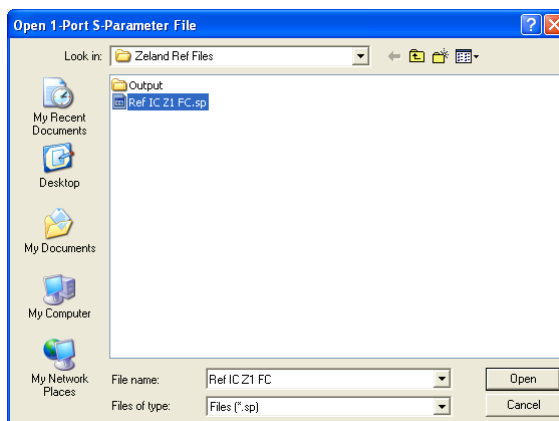
Process --- General Lumped Equivalent Circuit

Check ☒ under **Status and ID**

Select **Change Zs**



Select **Import**



Select **Ref IC Z1 FC.sp** --- **Open** (Open 1-Port S-Parameter File)

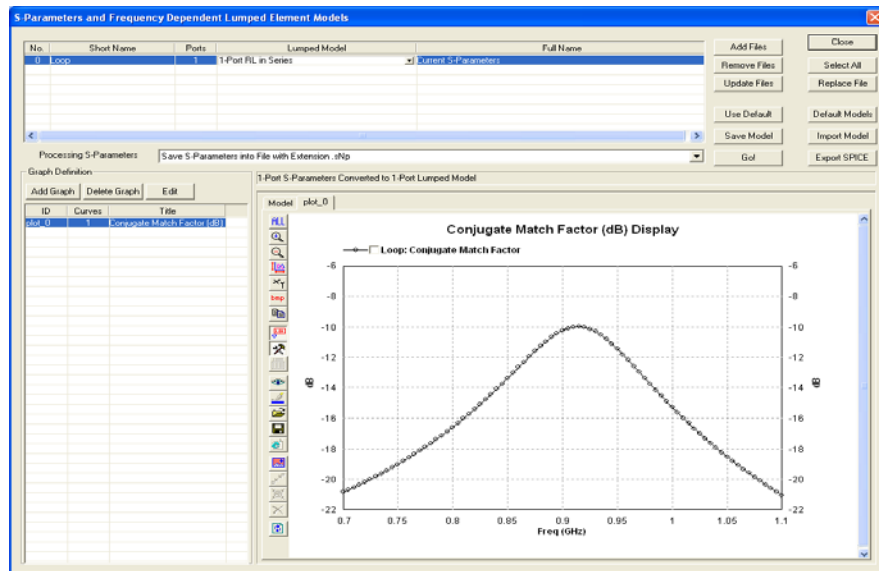
Display Conjugate Match Factor Graph

The Conjugate Match Factor is a parameter that measures the quantity of power applied to the chip. It is based upon the maximum available power transfer and is given in units of dB. As such 0dB indicates that all of the available power is transferred while 3dB indicates that one half of the available power is lost due to mismatch.

Select **OK** (Frequency Dependent Source Impedance)

Select **OK** (Display Conjugate Match Factor)

Select **Plot 0** (S-Parameters and Frequency Dependent Lumped Element Models)



3. Preliminary Loop Adjustment
 - Adjust the Loop Diameter as necessary achieve a resonance at highest required frequency
 - Repeat Simulation to observe Conjugate Match Factor (dB) Display
 - Continue to adjust and verify until desired Loop Frequency Response is achieved.
 - When desired results are obtained save the file as “Design Example.geo”

Initial Dipole Layout

1. Dimensional Reference Plane

Return to Polygon Editor

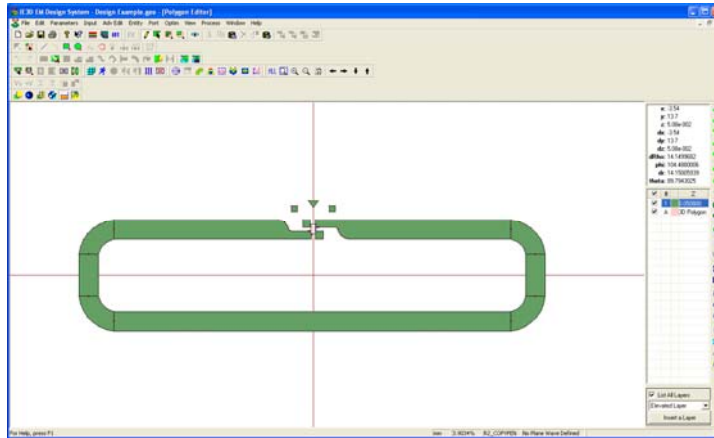
Select

Close

(S-Parameters and Frequency Dependent Lumped Elements)

Select

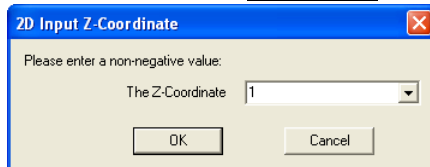
Window --- Display Polygon Editor



Insert Dimensional Reference

Select

Insert a Layer



Enter

The Z-Coordinate = 1

Select

OK (2D Input Z-Coordinate)

Click

#2 Z-Axis

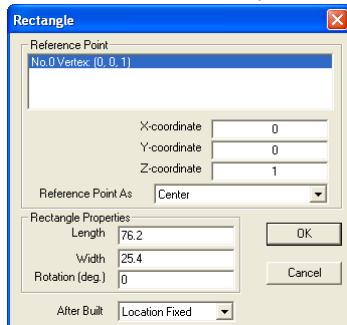
Select

Entity then **Rectangle**

Enter

Length = 76.2 --- Width = 25.4 --- X-coordinate = 0 --- Y coordinate = 0

Note: Size reflects the maximum size of the tag for reference



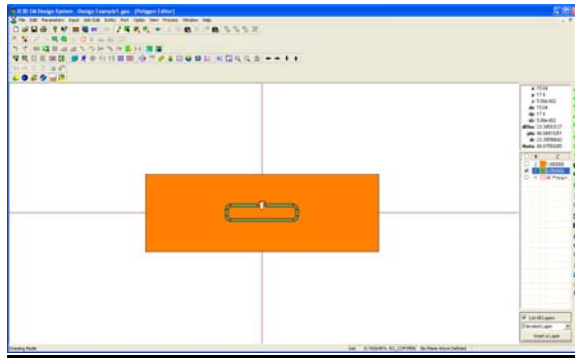
Select

OK

(Rectangle)

Select

#1 Z-Axis



Select

File --- Save

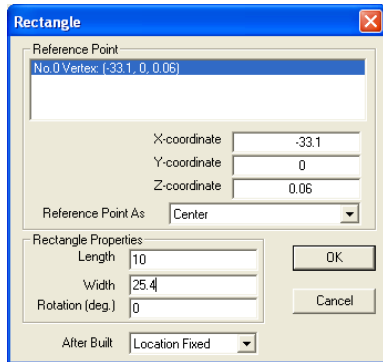
2. Dipole Construction

Left End Capacitance Plate

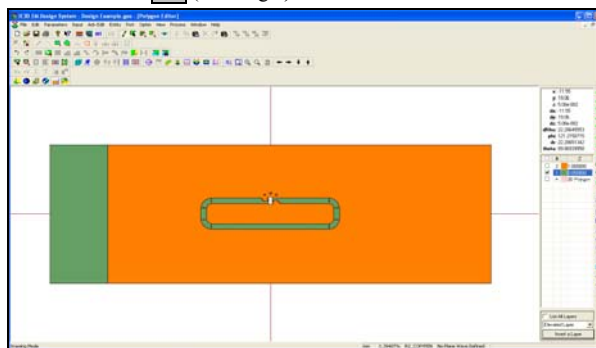
Place a 10mm x 25.4mm capacitance plate on the left end of the tag.

X position calculated from: $X = \text{Tag Width}/2$ -(half the width of the plate)

Select **Entity** then **Rectangle**
 Enter **Length = 10** and **Width = 25.4**
 Enter **X-Position = -33.1** and **Y-Position = 0**



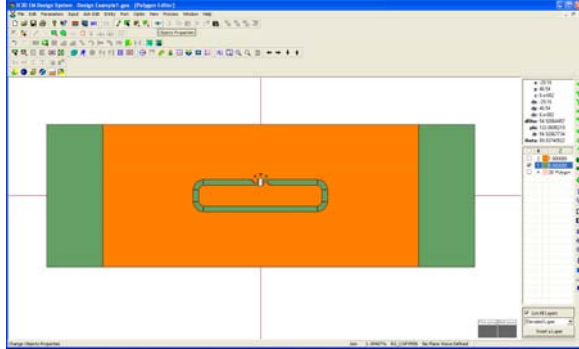
Select **OK** (Rectangle)



Right End Capacitance Plate

Repeat the left end capacitance plate process to enter the right end capacitance plate as follows:

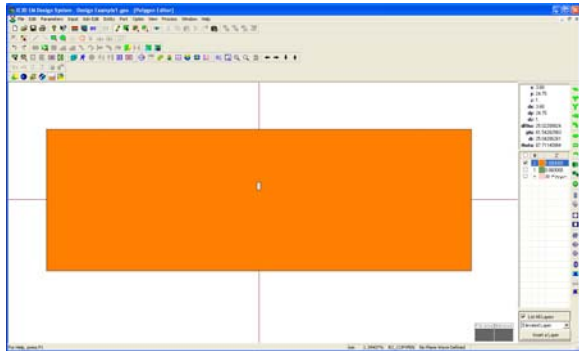
- Select **Entity** then **Rectangle**
- Enter **Length = 10** and **Width = 25.4**
- Enter **X-Position = 33.1** and **Y-Position = 0**
- Select **OK** (Rectangle)



Verify Geometry is contained within Dimensional Reference

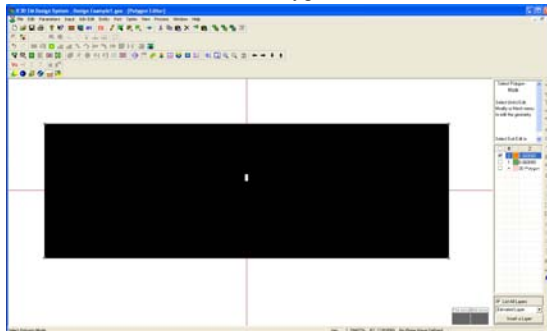
No Green should be visible if the tag outer extremes are within the size requirements.

- Click **Z-Coordinate = 2**

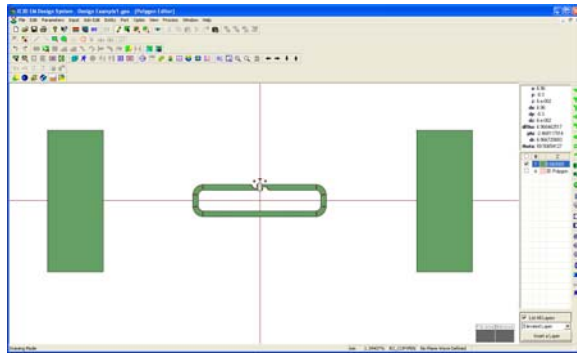


Delete Dimensional Reference

- Select **Edit --- Select Polygon** CTR-L
- Click on **Dimensional Polygon**



- Select **Edit --- Delete** DLT

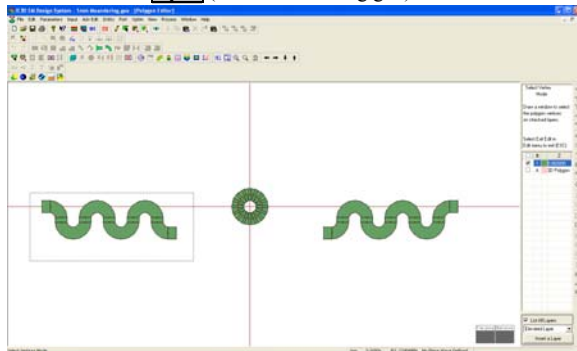


Select **File --- Save** CTR-S

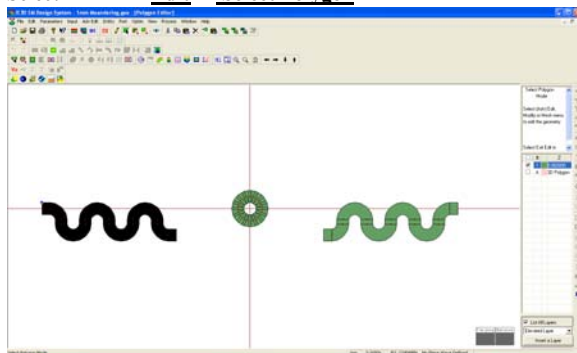
Left Dipole Meandering

Often a RFID tag will require additional inductance to achieve the desired location of the resonances. A typically used method is a trace called meandering. This guide has created reference files that contain 1mm meandering to save the designer the effort of creating them new each time a new tag is laid out.

Select **File --- Open**
 Select **Ref Design Folder - 1mm Meandering.geo**
 Select **Open** (1mm Meandering.geo)

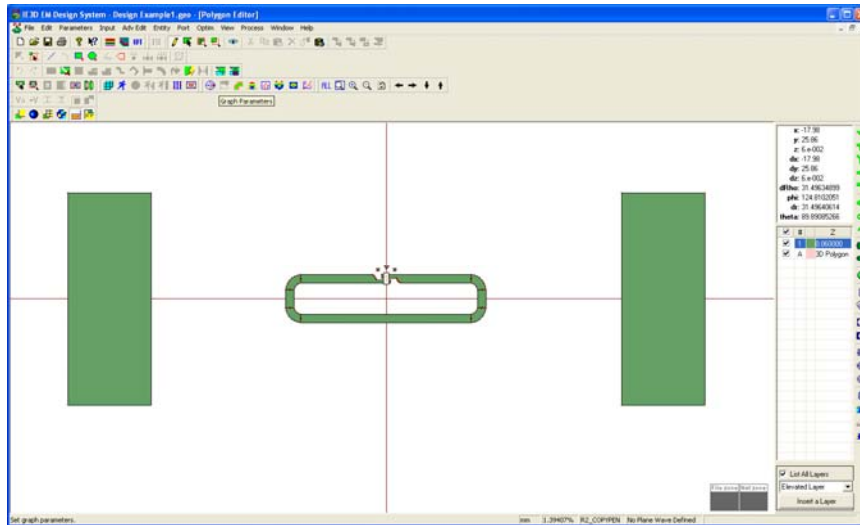


Select **Edit - Select Polygon Group** SHFT-Y
 Press & Hold Left mouse button and drag a rectangle around geometry as shown
 Select **Edit --- Select Polygon** CTR-L

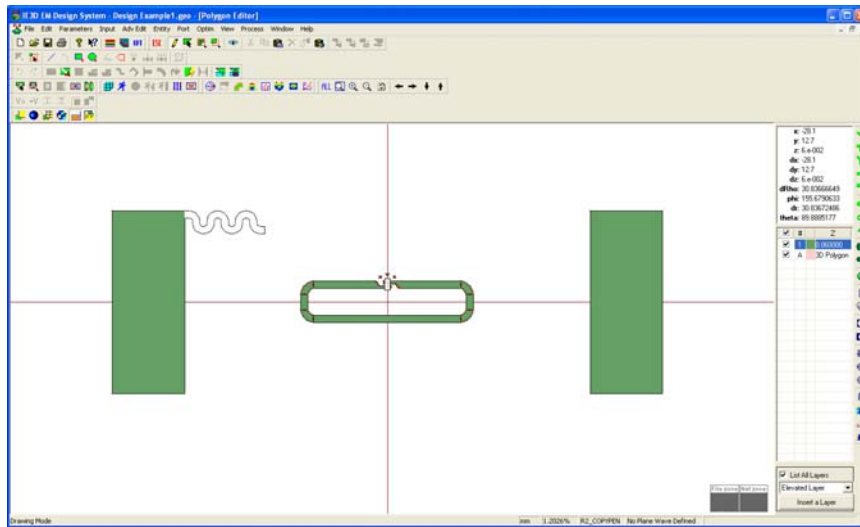


Press **Tab or Shift Tab until the upper left vertex is selected,**
(This will allow direct connection with the Design Example tag geo)

Select **Edit --- Copy** CTR-C
 Select **File - Open**
 Select **Design Example.geo --- Open** (Design Example.geo)

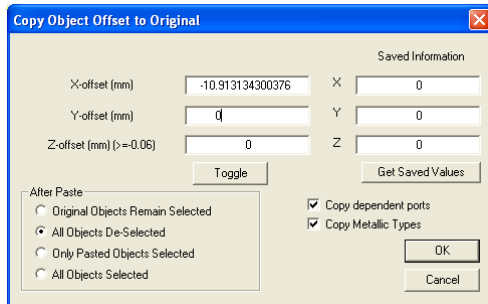


Select Edit then Paste CTR-V
 Locate **Meander Geometry to the upper right corner of the left capacitance plate**
 The vertex should snap to the upper right corner

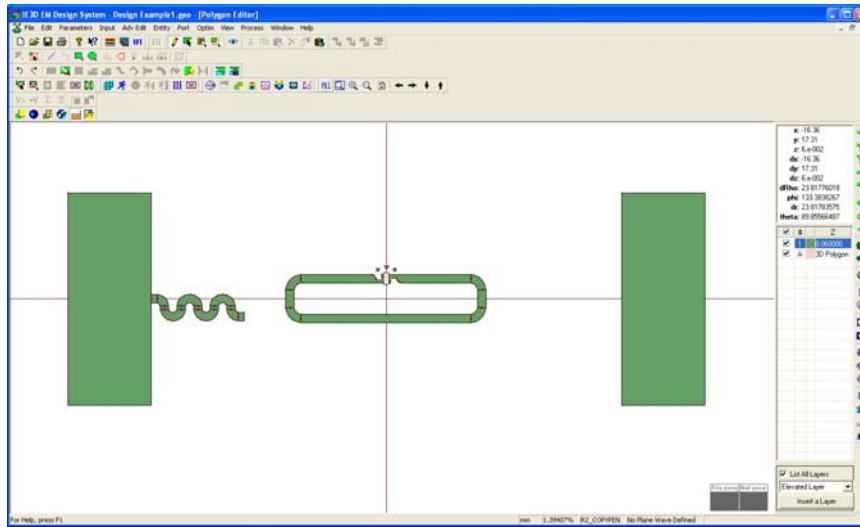


Click **The left mouse button**

Enter **Y-offset(mm) = 0** **X-offset(mm) is -10.913134300376 by default**



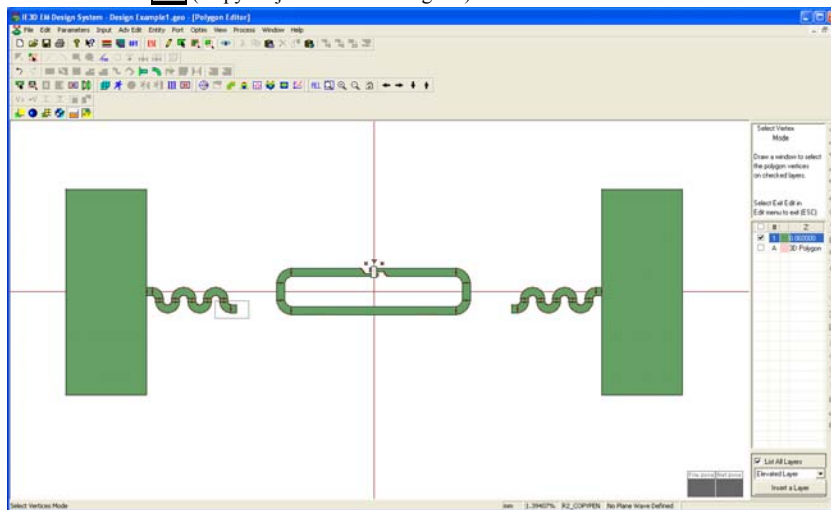
Click **OK** (Copy Object Offset to Original)



Right Dipole Meandering

Using the same procedure as for the Left Dipole Meandering import the right dipole meandering.

- Select **File --- Open**
- Select **Ref Design Folder - 1mm Meandering.geo**
- Click **Open** (1mm Meandering.geo)
- Select **Edit --- Select Polygon Group** SHFT-Y
- Press & Hold Left mouse button and drag a rectangle around the right side meandering
- Select **Edit --- Select Polygon** CTR-L
- Press **Tab or Shift Tab until the upper right vertex is selected,**
(This will allow direct connection with the Design Example tag geo)
- Select **Edit --- Copy** CTR-C
- Select **File --- Open**
- Select **Design Example.geo --- Open** (Design Example.geo)
- Select **Edit then Paste** CTR-V
- Locate **Meander Geometry to the upper left corner of the right capacitance plate**
The vertex should snap to the upper left corner
- Click **The left mouse button**
- Enter **Y-offset(mm) = 0 X-offset(mm) is 10.913134300376 by default**
- Click **OK** (Copy Object Offset to Original)



Select **File --- Save**

CTR-S

Dipole Connection

Connect the two meandered lines together

Select **Edit --- Select Vertices** ALT-S

Select **The inside quarter radius of the left side meandering**

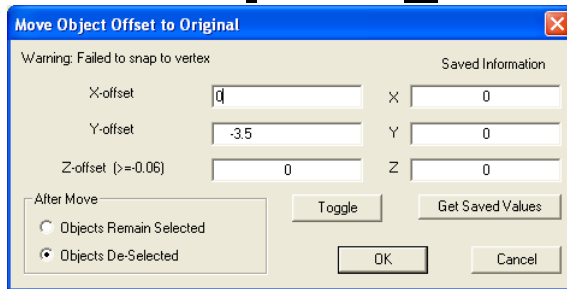
Press the left mouse button and drag a rectangle around the geometries as shown

Select **The inside quarter radius of the right side meandering**

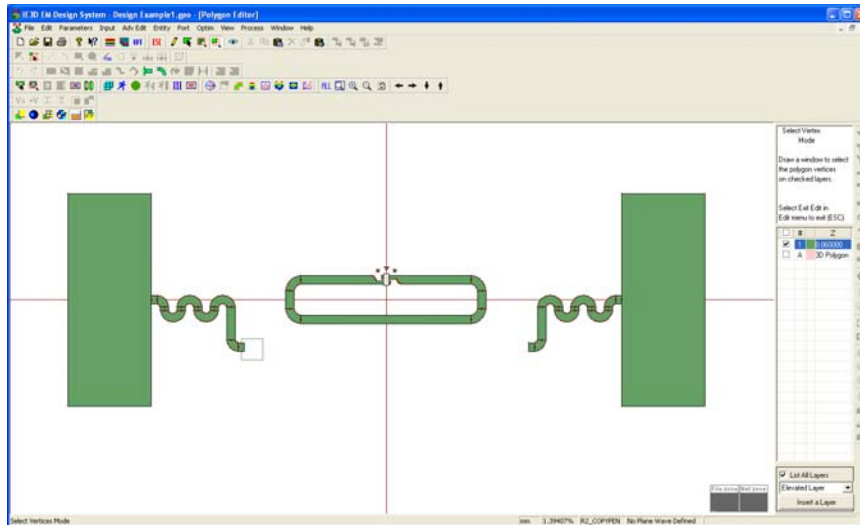
Press the left mouse button and drag a rectangle around the opposite geometries that are shown

Select **Edit --- Move Objects** SHFT-M

Enter **X-offset = 0 and Y-offset = -3.5**



Select **OK** (Move Object Offset to Original)



Select **Edit --- Select Vertices** ALT-S

Select **The bottom right most two vertices on the left side meandering.**

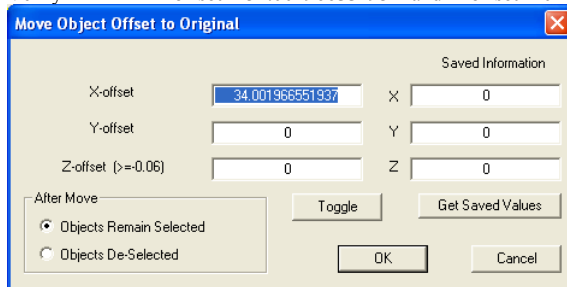
Press the right mouse button and drag a rectangle around the geometries as shown

Select **Edit --- Move Object**

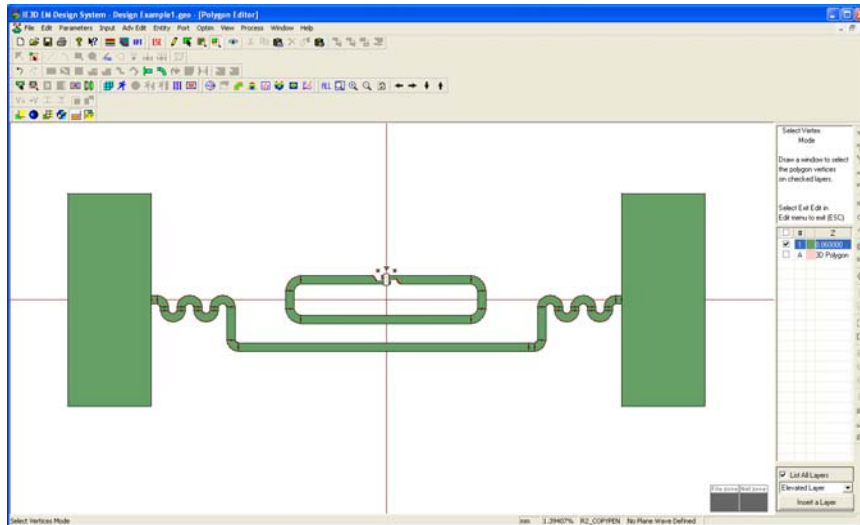
Move **The selected objects to their right side meandering corresponding vertices**

Object will snap to the opposite vertices

Verify **X-offset = 34.001966551937 and Y-offset = 0**



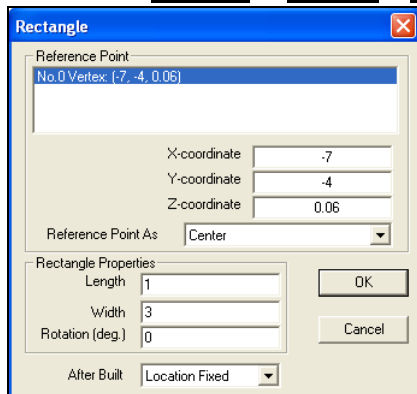
Select **OK** (Move Object Offset to Original)



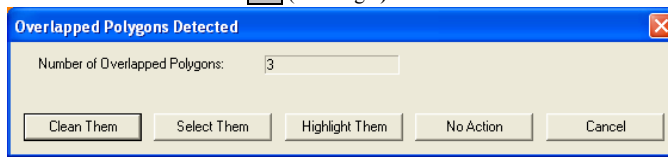
Loop Coupling Points

Couple the dipole to the loop

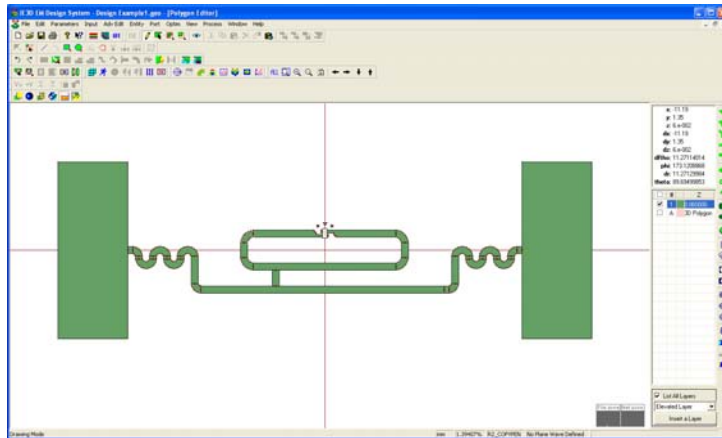
Select **Entity** then **Rectangle**
Enter **Length = 1** --- **Width = 3** --- **X-Position = -7** --- **Y-Position = -4**



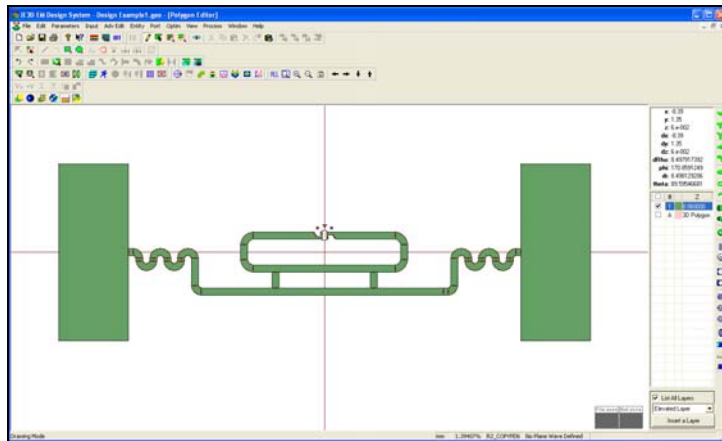
Select **OK** (Rectangle)



Select **Clean Them**



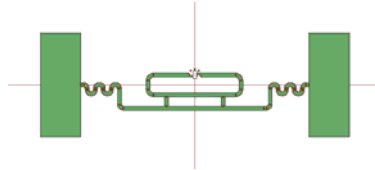
Select Entity then Rectangle
 Enter Length = 1 --- Width = 4 --- X-Position = 7 --- Y-Position = -4
 Select OK (Rectangle)
 Select Clean Them



Select File --- Save CTR-S

Appendix D
RFID Tag Design, Finite Dielectrics

Appendix E
RFID Tag Design, Optimizer



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Rev. 100615, Part No. 246066