Project Report

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Course Name: Smart Electronic System Design Paradigm

Instructor: Mr. Kishor Narang

Title: Design of a solution for energy monitoring and harmonic measurement up till 2.5 kHz i.e. 50th harmonic of AC sinusoid.

Contents

In this design project we have followed a 10 step design approach narrated below.

Level-1: Problem definition

Our current problem is appliance identification, leading towards fine grained disaggregation of our aggregated electricity bill using non-intrusive load monitoring (or NILM). Using this approach we are trying to itemize the load composition of buildings essentially using single point sensing of electrical parameters.

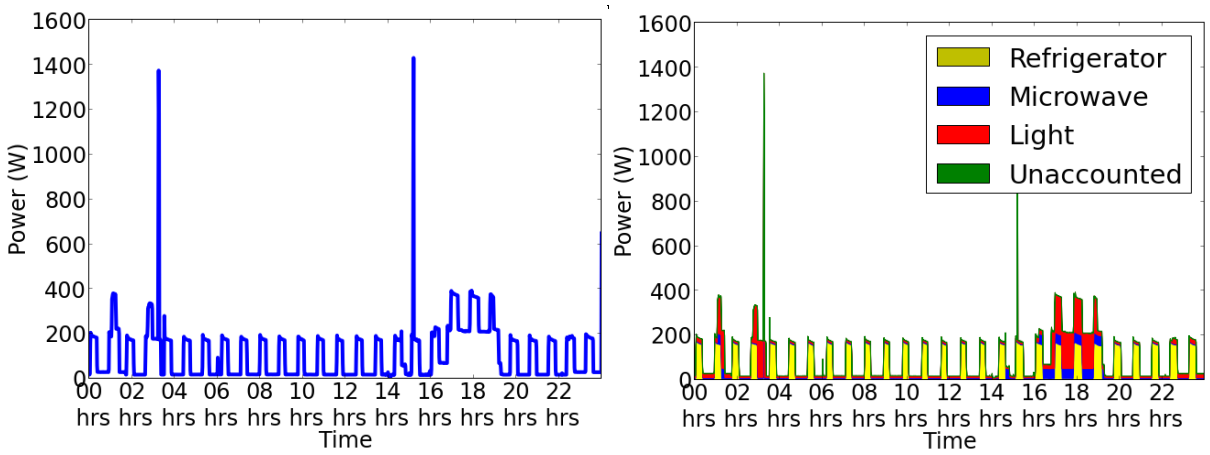


Figure-1 shows NILM as process where Figure-1(a) shows the aggregated power waveform captured using smart meter and Figure-1(b) shows the disaggregated breakdown of power in to constituent appliances.

As a technique NILM was proposed by G.W. Hart [1] three decades before, using power consumed by appliance as a feature to identify appliances. Since then several research groups across the globe have proposed multiple electrical parameters that can be used for appliance disaggregation but due to presence of complex loads, having time varying power consumption this problem is yet unsolved (shown in Figure-2).

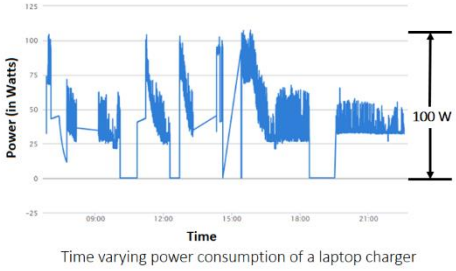


Figure-2

In our current project we are proposing use of power line Harmonics for appliance identification. This method requires a high frequency analog sensing and data acquisition system to capture power line harmonics from DC-2.5 kHz (i.e. 50^{th} harmonic of AC power line). As the problem statement is verified, next step in design methodology leads to background research.

Level-2: Background Research

Power line harmonic analysis is well studied in literature mostly by community dealing with power quality and related issues, and some commercial off the shelf (COTS) are available which can sense

power line harmonics. At this stage we did a thorough background study on available harmonic analyzers, respective features and communication interfaces. A detailed comparison of commercial power and harmonic analyzers from Fluke, MECO, Extech (Flir) is done. Few popular harmonic analyzers are discussed below along with their limitations [5, 6, 7, 8, 9, 10 and 11].

Fluke 435 Series II Power Quality and Energy Analyzer [Cost: Rs.5,85,000]

- 4 channel input (3 phase + neutral) for both voltage and current
- Resolution: 16 bit ADC on 8 channels
- Max sampling speed: 200 kS/s
- Scope for 4 voltage waveforms, 4 current waveforms, Vrms, Vfund. Arms, A fund, V @ cursor, A @ cursor, phase angles
- Measures Volts/amps/hertz Vrms phase to phase, Vrms phase to neutral, Vpeak, Hz
- Harmonics dc, 1 to 50, up to 9th harmonic for 400 Hz
- Harmonics Volts, THD, Harmonic Amps, K factor Amps, Harmonic Watts, THd Watts, K factor Watts, interharmonics
- Power and energy Vrms, Arms, Wfull, Wfund., VAfull, VAfund., VAharmonics, var, PF, CosQ, Efficiency factor

Figure-3

MECO PHA5850 Power and Harmonic Analyzer [Cost: NA]

- Analysis for 3P4W, 3P3W, 1P2W, 1P3W
- True RMS value (V123 and l123)
- Active Power (W, KW, MW, GW)
- Apparent and Reactive Power (KVA, KVAR)
- Power Factor (PF), Phase Angle (ϕ)
- Energy (WH, KWH. KVARH, PFH)
- Harmonic Analysis to the 99th Order
- Display up to 50 Harmonics

Figure-4

Extech 382096 3-Phase Power & Harmonics Analyzer [Cost: Rs.2,00,000]

- 4 channel input (3 phase + neutral) for both voltage and current
- Clamp-on measurements
- Harmonics display (1-99th order)
- Peak Values (1024 samples/period)
- Total Harmonic Distortion (THD-F), True RMS power, Active Power (kW), Apparent Power (kVA), Reactive Power (kVAR) and Power Factor, kWH and kVARh energy measurements
- Optically isolated RS-232 interface

Limitations of commercially available power line harmonic analyzers

Some of the commercial harmonic analyzers have all the required features like Fluke 435 Series II but they are priced around Rs. 5 Lakh which defeats the whole purpose of single point sensing. While others which are cheaper don't offer complete range of harmonic measurement and communication interfaces. So in either of the case there is need to build one power and harmonic analyzer which can facilitate the harmonic measurements up to 50 kHz.

Level-3: Specific Requirements

At this stage once we have a clear picture of what all parameters to be analyzed and about required communication interfaces, we have drafted our requirements below.

Features, specifications and requirements of sensing system.

- Analysis for 3P4W, 3P3W, 1P2W, 1P3W [4 wires : 3 phases and neutral]
- True RMS value (V123 and I123)
- Active Power (W, KW, MW, GW)
- Apparent and Reactive Power (KVA, KVAR)
- Power Factor (PF), Phase Angle (ϕ)
- Energy (WH, KWH. KVARH, PFH)
- Harmonic Analysis to the 99th Order
- Display up to 50^{th} Harmonics (i.e. up to 2.5 kHz)
- Display all these electrical parameters
- Provide local storage to dump data locally
- Serial interface (both USB and RS485) for communication

Add on features

- Debug interfaces
- Test points
- Pointer LED's
- Switches
- Header to add other features, communication interfaces

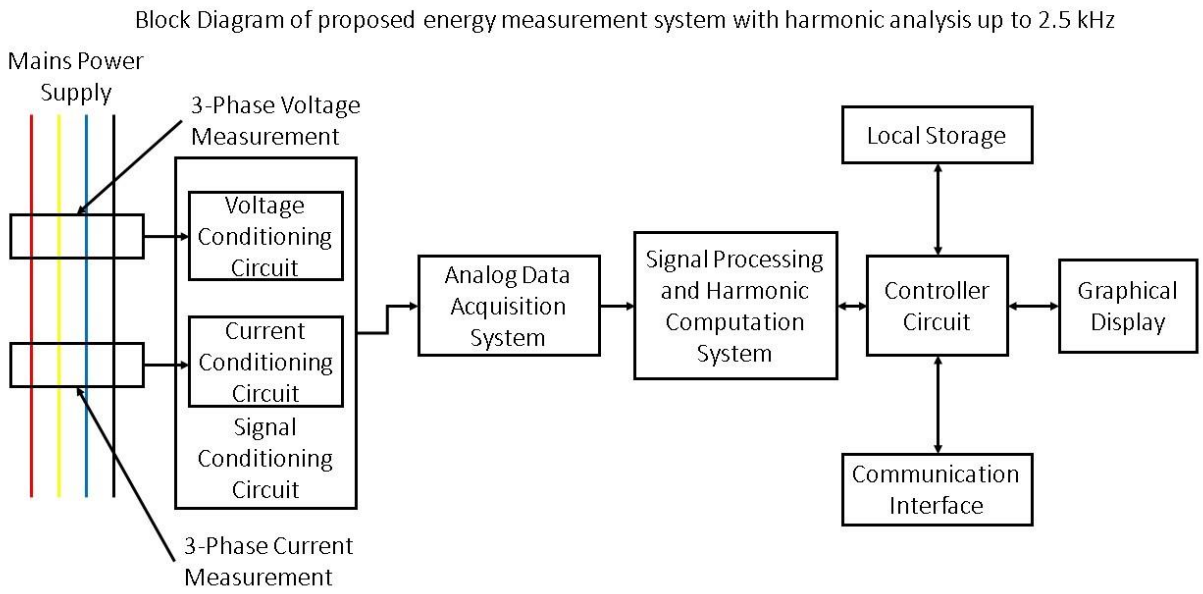


Figure-5 shows a detailed block diagram of all the required blocks and their physical interconnections.

Once we have specified the requirements of our design we can head on towards our next and most crucial stage i.e. to brainstorm and find an optimal solution for our design requirements.

Level-4: Choose an optimal solution

At this stage we prepared list of available design choices for power line harmonic measurements and finally selected one design which can best fit in our requirements.

Case-1: Design an analog sensing system using current transformers and voltage probes, for sensing 3 phase voltage and current, interfaced with a high speed data acquisition system (like NI DAQ). After analog to digital conversion this data is provided over serial interface. For signal processing and harmonic analysis computation has to be done locally on a different machine.

Case-2: Design a harmonic analyzer using an energy and harmonic measurement IC with built in DSP core for signal processing and harmonic analysis. The output from this IC has to be taken over any high speed bus using a microcontroller and post-acquisition this data can be displayed on a graphic LCD or can be stored locally.

Based on these two choices, we will now consider limitations of both of these designs.

Case-1 having CTs and voltage probes directly connected to analog DAQ is a simple and straightforward method for sensing electrical parameters but the post-acquisition processing will be quite complex as we

have to implement DSP algorithms on a secondary machine which will compute harmonics and rest of the electrical parameters and finally communicate them over serial interface.

Case-2 seems to be rather more complex in terms of hardware involved but as most of the required features are implemented in hardware the software part/ controller section will be simple. In this design all the computation and signal processing is done in hardware which reduces design complexity significantly. The IC used for energy and harmonic measurement will deliver processed electrical parameters over high speed serial bus, which can be fetched using a microcontroller. Post-acquisition these parameters are stored locally or communicated using standard bus protocols like USB and RS-485.

Finally while selecting optimal components and ICs lot of parameters have to be kept in mind before finalizing the BOM, few of them are mentioned below.

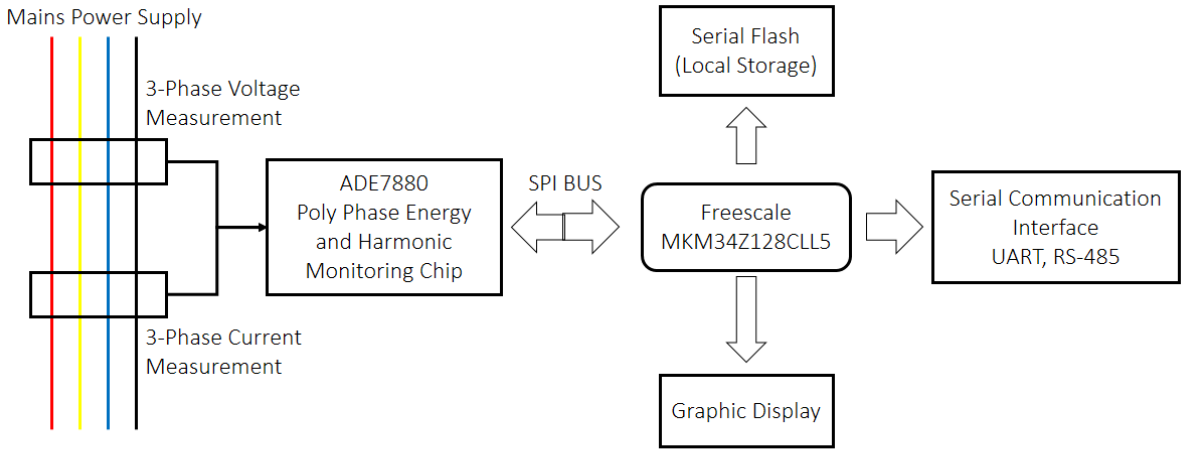
- Precision/ Resolution/ Dynamic range of IC in case it is an Analog IC
- Input and output range of voltages
- Power supply requirements
- Communication interfaces available
- No. of general purpose input's and output's
- Packages of components and IC's
- Thermal dissipation of components and IC's
- Overall cost of BOM

Based around these design choices and features we have selected following components and design add-ons.

- ADE-7880 polyphase energy metering and harmonics measurement IC [Analog Devices]
- Freescale MKM34Z128C ARM cortex M0+ controller (specifically meant for AMR applications)
- Dedicated signal conditioning circuits on all the phases and neutral (i.e. Vphase-1, Vphase-2, Vphase-3, Vneutral and Iphase-1, Iphase-2, Iphase-3, Ineutral) and test points to monitor voltage at different nodes.
- Support for serial communication over USB using FT232RL chip
- RS-485 differential bus interface using MAX485 chip
- Local storage using serial SPI flash.
- Graphic display to display all the measured parameters on board, this can also be used to display waveforms in future.

NB: Complete details of all the ICs and components is given at last in appendix section to maintain flow of design approach.

A detailed block diagram of overall circuit is shown below.



Block Diagram For Energy Measurement System With Harmonic Analysis Up To 2.5 Khz

Level-5: Develop and prototype the solution

This is the most comprehensive stage of our design which includes designing a schematic (in Orcad capture CIS), revising and optimizing schematic while considering all the possible loopbacks and test cases which are required to make this design work. Post-schematic generation next task is to do a final review of the schematic and generate net list from the schematic.

Details of major revisions of schematics featuring all updates, modifications and optimization.

- Version 1.8
  - First version of the schematic is having ADE-7880 and signal conditioning circuits as per evaluation kit of ADE-7880 from analog devices.
  - Drawback: The design was scattered across 10 sheets and was bit difficult to relate at this stage.
- Version 2.0
  - Few redundant sections like high speed isolators and buffers are removed to reduce the design complexity of our first prototype. Although we plan to use isolation in communication interface.
  - Drawback: The design was scattered across 6 sheets now but was still difficult to relate.
- Version 2.2
  - Complete schematic having ADE-7880 with all the signal conditioning circuits is brought to a single design sheet.
  - Headers are left for Interfacing with microcontroller.
  - Drawback: Power Supply section and other communication interfaces are yet to be exposed.
- Version 2.5
  - Added schematic for MKM34Z128CLL5 ARM Cortex M0+ from Freescale to this design and communication circuit over USB (isolated from MCU section using opto-couplers) and RS-485.

- 128x64 graphic display is added to display energy and harmonics data. This display can also be used for showing actual waveforms similar to DSO.
- Added power supply section.
- Local storage support using serial flash is also added over SPI interface.

- Version 2.6
  - Extra jumpers and test points are removed to reduce design complexity as well as susceptibility to EMI and RFI.
- Version 2.7
  - Added LED's to display status of ongoing pulses at CF1, CF2 and CF3 and mapped some extra LED's to GPIO's of MCU for debugging purpose.
  - Added some switches to provide control for graphic LCD.
- Version 2.8
  - Modified opto-couplers section, removed external-clock input feature
- Version 2.9
  - Modified the complete signal conditioning circuit for voltage sensing.
  - Mapped header for MCU interface directly to the MCU chip.
  - CF1, CF2, CF3, IRQ0, IRQ1, PM0, PM1 are also connected to GPIO's of microcontroller.
  - Improved power supply section added decoupling capacitors to filter noise.
  - Connected AGND and DGND using a ferrite bead to provide DC coupling.
  - Connected AVDD and DVDD using a 10 ohm resistor.
  - Added headers for voltage and current sensing analog front end.
  - Added separate power source for isolators.
  - Added test points to CF1, CF2, CF3, IRQ0, IRQ1, PM0, PM1.

Major Improvements: At this stage we are close to send the design for fabrication once the net list is generated and verified.

- Version 3.0

Just one additionally copy of design before sending for net list generation and layout part.

NB: Currently the layout of the design is being prepared, this will be led by fabrication of PCB's, component placement and heading towards testing stage.

Level-6: Test the solution

Although design hasn't yet reached this stage but in this the board will be tested first at hardware level for each block (AFE, MCU and rest of peripherals) and then later on at firmware level. Firmware level will be again implemented in block wise manner.

Level-7: Match the requirements (Case-1: if design requirements are met)

This is a bit mature stage of design where the design will be deployed and real time harmonic data is collected, with ground truth labels for each and every appliance. Once we have such database we will match this with a commercial harmonic analyzer to benchmark quality of our data.

Level-8 and Level-9: Match the requir ements (Case-2: if design requirements aren't met)→ Reiterate the design, prototype, testing and matching phase (NB: Required if the design requirements aren't matched)

In case post analysis of harmonics data reveal that this design is not giving accurate measurements then steps 4, 5 and 6 have to be exercised again. This step may involve multiple calibration, testing and measurement cycle till the design specifications aren't met.

Level-10: Deploy the final system and communicate results

If design performs as per requirements at level-7 then we are close to our design goal and we can deploy the system in real time and collect appliance level harmonic data along with power consumption traces for longer duration and over a wide set of appliances.

Learnings from this project

This project was useful in lot many ways but few highlights are mentioned below

1. How to perform background research with existing solutions. This not only provide knowledge of technologies available around the design statement but also provides you a thought for required features and add-ons in your design.
2. How to speculate and conceptualize design requirements in an optimized manner.
3. How to choose from multiple possible solutions for the same problem.
4. How to leverage resources available in market to deliver the best solution.
5. How to select components precisely, making a trade-off between design requirements and BOM cost.
6. How to design an effective schematic with required interconnections.
7. How to do placement of components based on their function.
8. How to match technical requirements of design with relative simple methods to reduce BOM cost.

Specifications-1: ADE7880 (Analog Devices) 3-Phase Energy Metering and Harmonic Measurement IC with Add-on Support for Power Quality Measurement

Features

- Supports International Electro Technical Commission standards, European Nation Standards and American National Standards Institute's standards.

IEC 62053-21: Static energy meters for active energy (Class 0 and 1)

IEC 62053-22: Static energy meters for active energy (Class 0, 2S and 0, 5S)

IEC 62053-23: Static energy meters for reactive energy (Class 2 and 3)

EN 50471-1: Electromagnetic Compatibility - emission standard for wire-line telecommunication networks

EN 50471-3: Electromagnetic Compatibility - emission standard for wire-line telecommunication networks

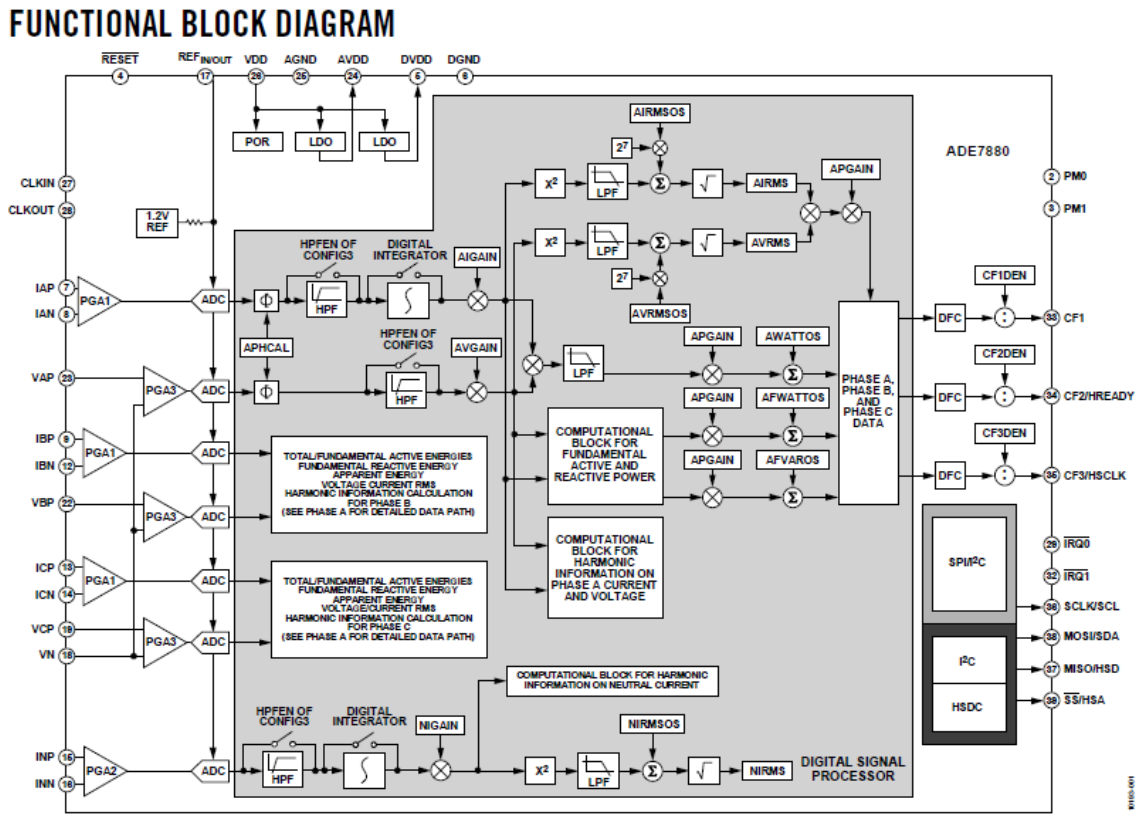
ANSI C12.20: American National Standard for Electricity Meters - accuracy and performance

- Supports Class-1, Class-2 accuracy
- Supports 3 phase 3 wire and 3 phase 4 wire (delta, wye) topology.
- Supports measurements of RMS, active, reactive, apparent power, power factor, THD, harmonic distortion of all phases and neutral.
- Less than 1% error in harmonics.
- Supplies total (fundamental and harmonics) active and apparent energy on each phase with less than 0.1% error in reactive and active energy up to dynamic range of 1000-1 and 0.2% error up to 5000-1.
- Supports battery supply for missing neutral pin.
- Internal reference of 1.2V (drift 20 PPM).
- 40-pin lead frame chip scale package.

Description/ Features

- 3-phase energy metering IC
- Serial Interface (SPI and I2C)
- 3 pulse outputs (CF1, CF2, CF3)
- In-built second order sigma-delta ADC
- In-built digital integrator
- In-built signal processing circuits to perform total (fundamental active and apparent energy measurement, RMS calculations, fundamental only active and reactive measurements)
- Additionally computes RMS of harmonics
- Supports measurement of total harmonic distortion of all phases voltages and currents
- Fixed DSP core to perform signal processing
- Supports 3 and 4 wire (wye and delta) type 3 phase measurements
- Provides system calibration for each phase, RMS offset correction, phase calibration and gain calibration
- CF1, CF2, CF3 provide wide choice of power information i.e. total active power, apparent power, sum of current RMS values, fundamental active and reactive power
- Waveform sample registers allow access to all ADC's
- It also supports power quality measurements like short duration transients, angles between phase voltages and currents
- HSDC (high speed data capture port) in parallel with I2C to provide access to ADC's
- Interrupt pins IRQ0 and IRQ1 to indicate events
- 3 low power modes to ensure energy accumulation while tampering
- Pin compatible with ADE-7854, ADE-7858, ADE-7868, ADE-7878.

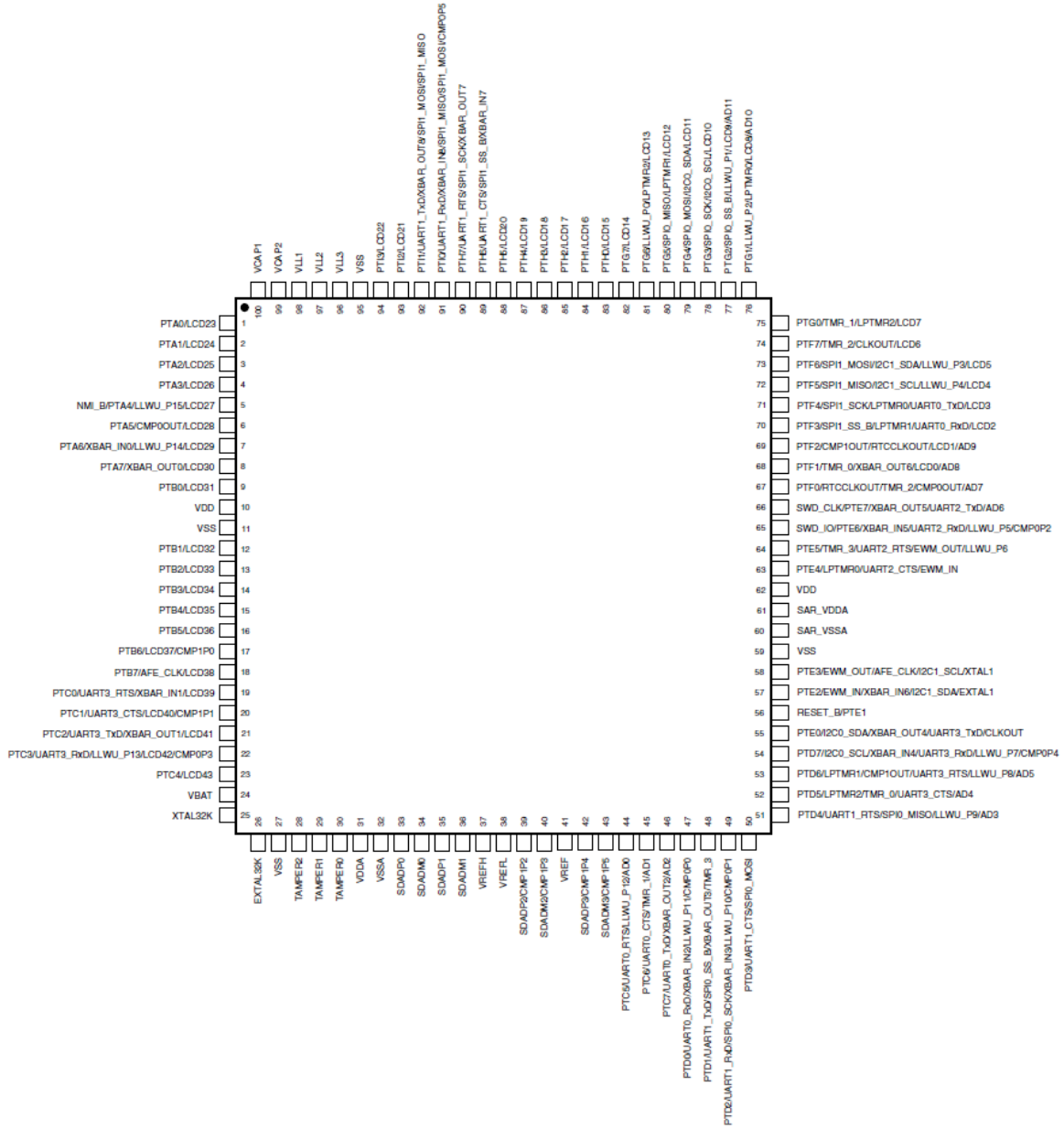
Block Diagram



Specifications-2: Freescale MKM34Z128CLL5 ARM Cortex M0+ controller

- Core: ARM Cortex M0+
- Data bus width: 32-bit
- Maximum clock frequency: 50 MHz
- Program memory size: 128 Kb
- Data RAM size: 16 kB
- A/D bit size: 24-bit sigma-delta ADC with PGA, 12 channel 16-bit SAR ADC
- Operating supply voltage: 1.71 V to 3.61 V
- Max. operating temperature: +85˚C
- Package: LQFP 100
- Data RAM type: RAM
- Data ROM size: 128 kB
- Data ROM Type: Flash
- Interface Type: 2-I2C, 2-SPI, 4-UART
- On chip DAC: with DAC
- LCD Segment driver (up to 288)
- High accuracy RTC (+-% PPM)

- Two internal clock reference:
    - 32 kHz and 2 MHz



100-pin LQFP Pinout Diagram

Specifications-3: FTDI FT232RL (USB Host IC)

Overview [12]

- Single chip USB to serial data interface
- Entire USB protocol on chip
- Data transfer rates from 300 baud to 300 Mega baud
- Clock output signals for driving external MCU
- FIFO transmit and receive buffers for high data throughput
- 1024 bit EEPROM for storing device descriptors
- Integrated +3.3V level converter for USB I/O
- Package: SSOP-28, QFP-32

Specifications-4: Winbond W25Q64FV (Serial Flash IC)

Overview [15]

- 8 M Byte Serial Flash Memory
- Communication Interface:
    - Standard SPI: CLK, /CS, DI, DO, /WP, /HOLD
    - Dual SPI: CLK, /CS, IO0, IO1, /WP, /HOLD
    - Quad SPI: CLK, /CS, IO0, IO1, IO2, IO3
    - QPI: CLK, /CS, IO0, IO1, IO2, IO3
- Voltage Operation: 2.7V to 3.6V
- 32,768 programmable pages of 256 byte each
- SPI clock frequencies up to 104 MHz
- 24 bit addressing
- 50MB/s data rate
- 100,000 erase/ program cycles
- More than 20 year data retention
- Package: SOIC-8
- Allows true execute in place (XIP)

References

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2. Sutherland, Peter E. "Harmonic measurements in industrial power systems." Industry Applications, IEEE Transactions on 31.1 (1995): 175-183.
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4. Ma, Haili, and Adly A. Girgis. "Identification and tracking of harmonic sources in a power system using a Kalman filter." Power Delivery, IEEE Transactions on 11.3 (1996): 1659-1665.
5. http://www.mecoinst.com/meco-product-details/Power-and-Harmonics-Analyser.aspx
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7. http://www.fluke.com/fluke/inen/Power-Quality-Tools/Logging-Power-Meters/Fluke-435-Series-II.htm?PID=73939
8. http://www.flir.com/uploadedFiles/Extech/US_Datasheets/Clamp-On_Meters/Speciality_Clamp_Meters/382095_382096_data_en.pdf
9. http://powersight.com/?gclid=CNKv_bj1nsICFVIpjgody2oA_Q
10. http://www.bosworthinstrument.com/382095info.html
11. https://www.hioki.com/products/power_current_sensor/power_meters/683
12. http://www.ftdichip.com/Support/Documents/DataSheets/ICs/DS_FT232R.pdf
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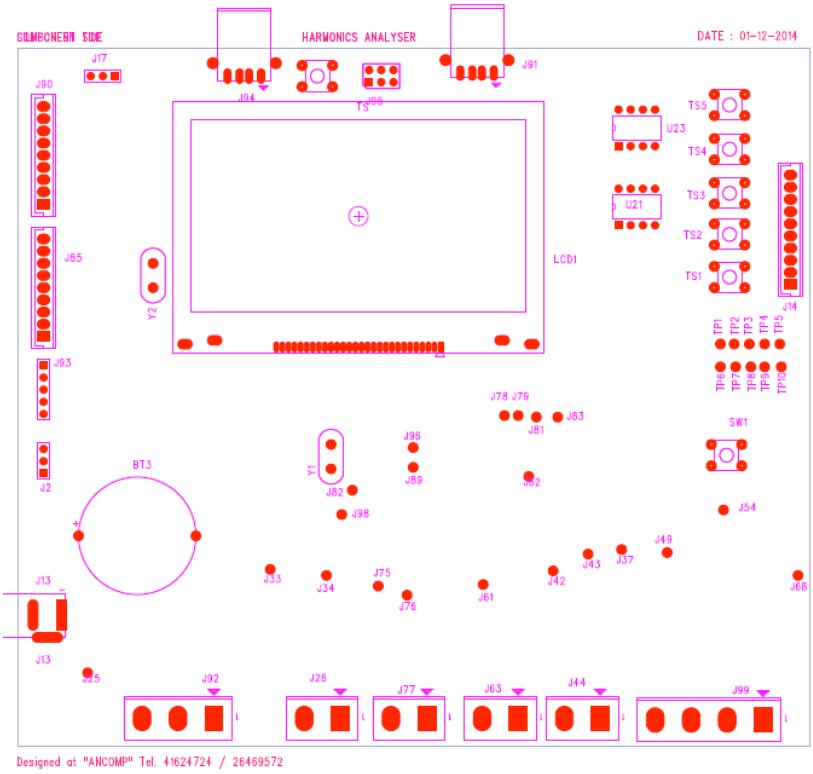
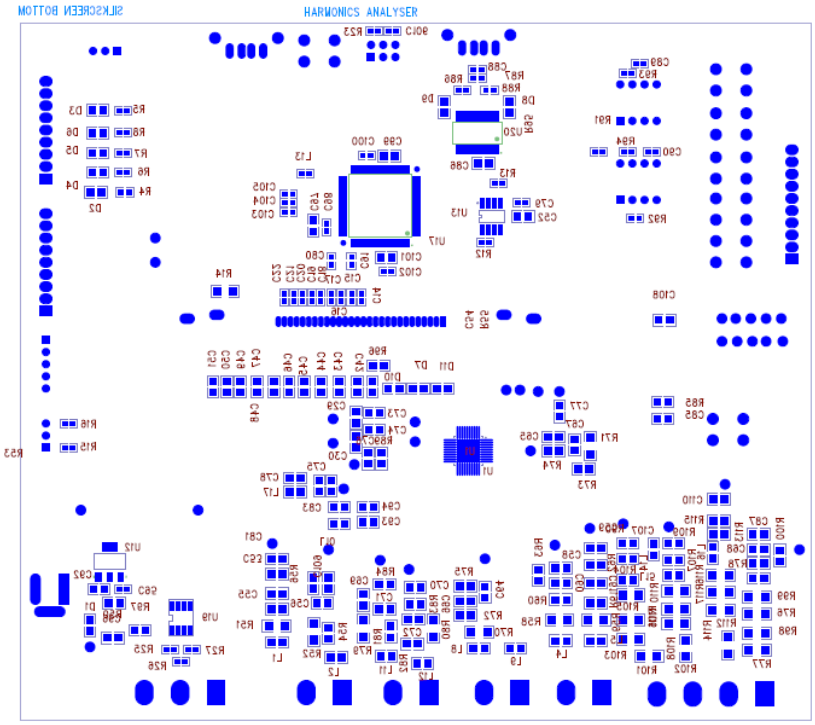
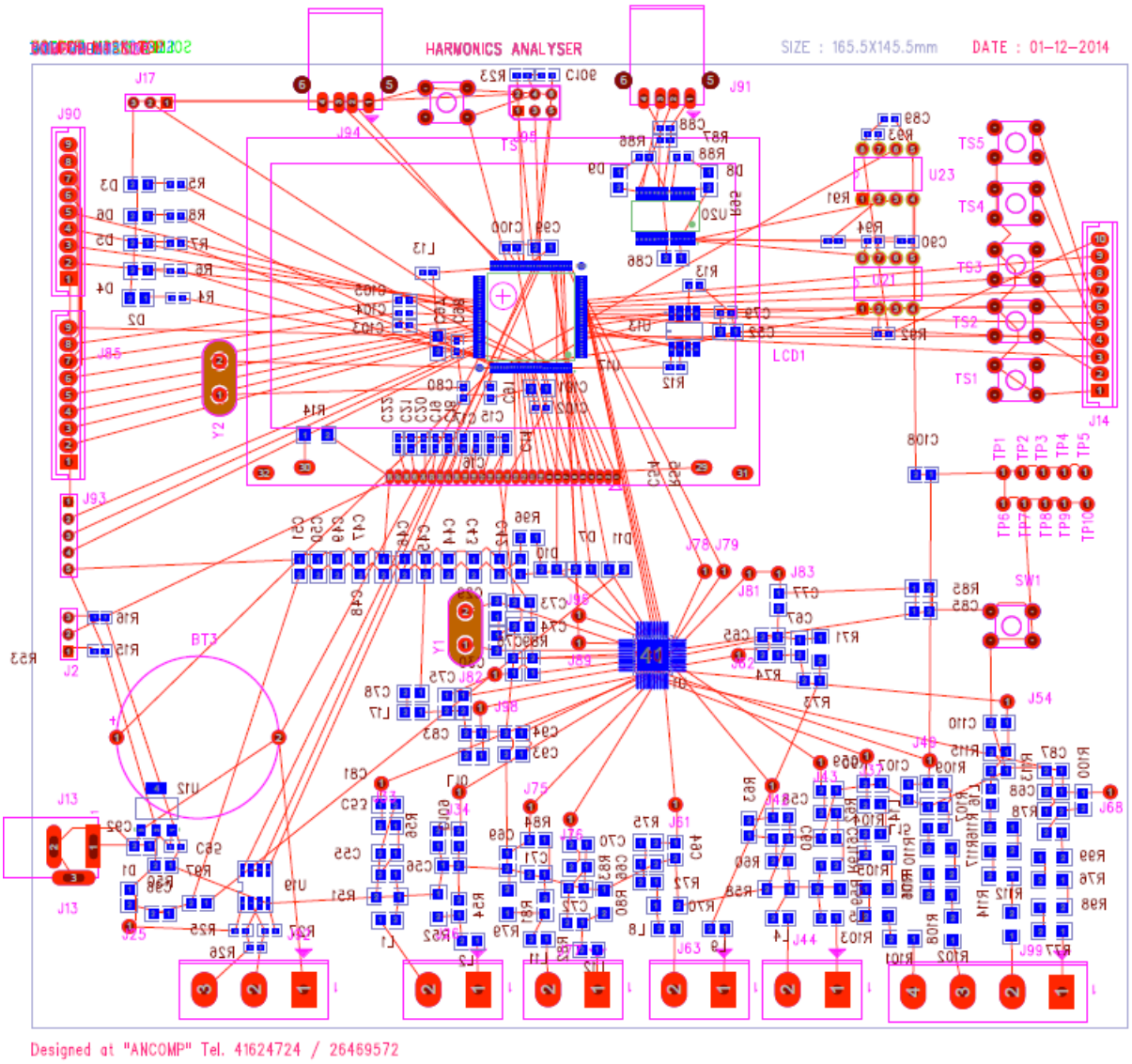
15. http://www.nexflash.com/NR/rdonlyres/05A6F2FD-83D2-4748-8394-65909AC2A8E3/0/W25Q64FV.pdf

Placement Map for Current Design (Schematic Revision 3.0)





Routing Map for both layers



Net list of this design taken from schematic (Rev 3.0), prepared by Mr. Sanjeev (Ancomp Solutions) is attached separately [due to size constraints].

Bill of Materials from schematic (Rev 3.0)

Item Number	Quantity	Value	Description	Part Number	Part Reference	PCB Footprint
1	1	BATTERY			BT3	CR2450
2	1	1uF			C14	0603
3	1	1uF			C15	0603
4	1	1uF			C16	0603
5	1	100nF			C17	0603
6	1	100nF			C18	0603
7	1	100nF			C19	0603
8	1	100nF			C20	0603
9	1	100nF			C21	0603
10	1	100nF			C22	0603
11	1	20PF			C29	0805
12	1	20PF			C30	0805
13	1	0.1uF			C42	
14	1	0.1uF			C43	
15	1	0.1uF			C44	
16	1	0.1uF			C45	
17	1	0.1uF			C46	
18	1	0.1uF			C47	
19	1	0.1uF			C48	
20	1	0.1uF			C49	
21	1	0.1uF			C50	
22	1	0.1uF			C51	
23	1	2.2uF			C52	0805
24	1	220pF			C53	
25	1	220pF			C54	
26	1	220pF			C55	
27	1	220pF			C56	
28	1	220pF			C58	
29	1	220pF			C59	
30	1	220pF			C60	
31	1	220pF			C61	
32	1	220pF			C64	
33	1	220pF			C65	
34	1	220pF			C66	
35	1	220pF			C67	
36	1	20nF			C68	
37	1	220pF			C69	
38	1	220pF			C70	
39	1	220pF			C71	

40	1	220pF	C72	
41	1	0.1uF	C73	
42	1	10uF	C74	
43	1	0.22uF	C75	
44	1	4.7uF	C76	
45	1	0.22uF	C77	
46	1	4.7uF	C78	
47	1	100nF	C79	0603
48	1	22pF	C80	0603
49	1	0.1uF	C81	
50	1	4.7uF	C83	
51	1	10uF	C85	
52	1	1uF	C86	0805
53	1	20nF	C87	
54	1	0.1uF	C88	0603
55	1	0.1uF	C89	0603
56	1	0.1uF	C90	0603
57	1	22pF	C91	0603
58	1	2.2uF/16V	C92	0805
59	1	20nF	C93	
60	1	20nF	C94	
61	1	0.1	C95	0603
62	1	22uF	C96	0805
63	1	2.2uF	C97	0805
64	1	100nF	C98	0603
65	1	2.2uF	C99	0805
66	1	100nF	C100	0603
67	1	2.2uF	C101	0805
68	1	100nF	C102	0603
69	1	0.1uF	C103	0603
70	1	0.1uF	C104	0603
71	1	0.1uF	C105	0603
72	1	0.01uF	C106	0603
73	1	20nF	C107	
74	1	20nF	C108	
75	1	20nF	C109	
76	1	20nF	C110	
77	1	LED	D1	
78	1	LED	D2	0805
79	1	LED	D3	0805
80	1	LED	D4	0805
81	1	LED	D5	0805
82	1	LED	D6	0805

83	1	LED	D7	
84	1	RX LED	D8	0805
85	1	TX LED	D9	0805
86	1	LED	D10	
87	1	LED	D11	
88	1	LCD conn.	J1	box conn
89	1	jumper3-pin	J2	
90	1	5V DC JACK	J13	PDCJ01-01
91	1	Keypad conn	J14	10 PIN BOX_HEADER
92	1	NMI_HEADER	J17	SIL_HEADER
93	1	LCD conn	J22	BOX_CONNECTOR
94	1	HEADER 1	J25	
95	1	HEADER 2	J26	PHOENIX(5MM)
96	1	INN	J33	
97	1	INP	J34	
98	1	VN	J37	
99	1	IAN	J42	
100	1	IAP	J43	
101	1	HEADER 2	J44	PHOENIX(5MM)
102	1	VAP	J49	
103	1	VBP	J54	
104	1	IBN	J61	
105	1	IBP	J62	
106	1	HEADER 2	J63	PHOENIX(5MM)
107	1	VCP	J68	
108	1	ICN	J75	
109	1	ICP	J76	
110	1	HEADER 2	J77	PHOENIX(5MM)
111	1	PM0	J78	
112	1	PM1	J79	
113	1	VDD	J81	
114	1	AVDD	J82	
115	1	DVDD	J83	
116	1	Sigma Delta 0,1	J85	SIL header
117	1	~IRQ1	J89	
118	1	Sigma Delta 2,3	J90	SIL Header
119	1	Data Communication Conn,	J91	Type-A USB-female conn
120	1	54ACT8990/LCC	J92	PHOENIX(5MM)
121	1	Tamper header	J93	SIl header
122	1	I2C Connector	J94	Type-A USB-female conn

123	1	DUBUGGER_CONN.	J95	DUAL INLINE 6PIN
124	1	~IRQ0	J96	
125	1	REFIN	J98	
126	1	HEADER 4	J99	PHOENIX(5MM)
127	1	1500	L1	
128	1	1500	L2	
129	1	1500	L4	
130	1	1500	L5	
131	1	1500	L8	
132	1	1500	L9	
133	1	68E @ 100MHz	L10	
134	1	1500	L11	
135	1	1500	L12	
136	1	1KE/100 MHz	L13	0603
137	1	68E @ 100MHz	L14	
138	1	68E @ 100MHz	L15	
139	1	68E @ 100MHz	L16	
140	1	68E @ 100MHz	L17	
141	1	LCDTM12864A8CCWG WA	LCD1	same as in EDS
142	1	220E	R4	0603
143	1	220E	R5	0603
144	1	220E	R6	0603
145	1	220E	R7	0603
146	1	220E	R8	0603
147	1	10K	R12	0603
148	1	10K	R13	0603
149	1	100E	R14	1206
150	1	10K	R15	0603
151	1	10K	R16	0603
152	1	10K	R23	0603
153	1	680E	R25	0603
154	1	120E	R26	0603
155	1	680E	R27	0603
156	1	680	R50	
157	1	TBD1206	R51	
158	1	TBD1206	R52	
159	1	100	R53	
160	1	100	R54	
161	1	1k	R55	
162	1	1k	R56	
163	1	TBD1206	R58	
164	1	TBD1206	R59	

165	1	100	R60	
166	1	100	R61	
167	1	1k	R62	
168	1	1k	R63	
169	1	TBD1206	R70	
170	1	TBD1206	R71	
171	1	100	R72	
172	1	100	R73	
173	1	1k	R74	
174	1	1k	R75	
175	1	220k	R76	
176	1	220k	R77	
177	1	2.2k	R78	
178	1	TBD1206	R79	
179	1	TBD1206	R80	
180	1	100	R81	
181	1	100	R82	
182	1	1k	R83	
183	1	1k	R84	
184	1	10K	R85	
185	1	1K	R86	0603
186	1	1K	R87	0603
187	1	4.7K	R88	0603
188	1	10	R89	
189	1	2.2k	R90	
190	1	4.7K	R91	0603
191	1	4.7K	R92	0603
192	1	10K	R93	0603
193	1	10K	R94	0603
194	1	680	R95	
195	1	680	R96	
196	1	680	R97	
197	1	220k	R98	
198	1	220k	R99	
199	1	1k	R100	
200	1	220k	R101	
201	1	220k	R102	
202	1	220k	R103	
203	1	1k	R104	
204	1	220k	R105	
205	1	220k	R106	
206	1	2.2k	R107	
207	1	220k	R108	

208	1	1k	R109	
209	1	220k	R110	
210	1	220k	R111	
211	1	220k	R112	<1204>
212	1	2.2k	R113	
213	1	220k	R114	<1204>
214	1	1k	R115	
215	1	220k	R116	
216	1	220k	R117	<1204>
217	1	SW_TC_SPST	SW1	
218	1	SW PUSHBUTTON	TACTILE SWITCH	
219	1	SW PUSHBUTTON	TACTILE SWITCH1	
220	1	SW PUSHBUTTON	TACTILE SWITCH2	
221	1	SW PUSHBUTTON	TACTILE SWITCH3	
222	1	SW PUSHBUTTON	TACTILE SWITCH4	
223	1	SW PUSHBUTTON	TACTILE SWITCH5	
224	1	DGND	TP1	
225	1	DGND	TP2	
226	1	DGND	TP3	
227	1	DGND	TP4	
228	1	DGND	TP5	
229	1	AGND	TP6	
230	1	AGND	TP7	
231	1	AGND	TP8	
232	1	AGND	TP9	
233	1	AGND	TP10	
234	1	Value	U1	CP_40_10
235	1	1117 SOT223	U12	SOT223
236	1	W25Q64FV	U13	SOIC-8
237	1	Photon	U17	100 LQFP
238	1	MAX-485	U19	S08
239	1	FT232RL(DEBUG)	U20	SSOP28
240	1	ACNW261L	U21	DIP 8
241	1	ACNW261L	U23	DIP 8
242	1	16.384MHz	Y1	
243	1	32.768KHz	Y2	CRYSTAL

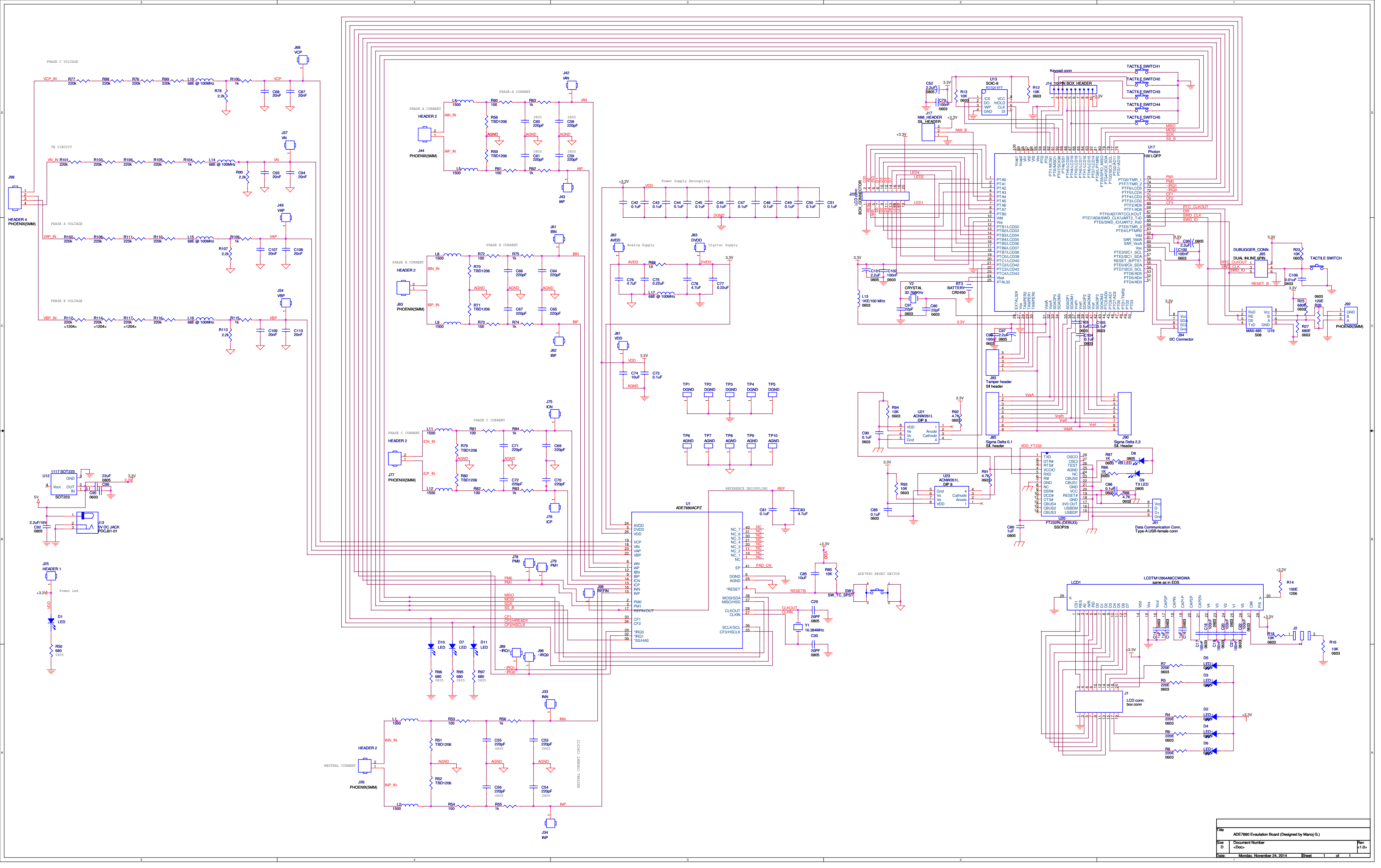
Rough Algorithm for Firmware of Harmonic Analyzer (to be loaded in MKM34Z128CLL5)

- Initialize RTOS environment
- Initialize LCD
    - Display an initialization message
- Start debug/test environment (will be serviced on all initializations)
    - Display a message on LCD or an LED blink on successful initialization
    - Otherwise display an error/debug message
    - Each call of this function will show unique error code/debug message
- Initialize SPI communication
    - Call for debug/test environment
- Initialize ADE-7880
    - Call for debug/test environment
    - Define calibration parameters and gain for all current and voltage channels
        - Call for debug/test environment
- Initialize W25Q64FV flash
    - Call for debug/test environment
- Initialize external interrupts for interrupts from ADE-7880
    - Call for debug/test environment
- Infinite Loop Statement
    - Fetch data from registers
        - Call for debug/test environment (will be serviced with each fetch statement, subject to code complexity)
        - Data for each of the registers is fetch sequentially
            - Real Power
            - Apparent Power
            - RMS of Voltage and Current
            - Harmonic Parameters
            - Power Factor (optional) and Phase angle (optional)
        - Store data in local storage or communicate over USB bus
            - Call for debug/test environment
            - Additionally do a sanity check if data is stored properly or not (once)
    - Display computed values for respective electrical parameters on Graphic LCD
        - Refresh LCD after every reading (will depend on sampling rate/ acquisition rate of MCU)
    - Display status of calibrated frequency (CF1, CF2, CF3) parameters on LED's
    - Check if all the calibration parameters and gain of PGA's is properly configured. (optional and will be done occasionally)
    - Store the data first in to SPI flash if power down button is pressed before shutting down.

Conclusion of the report

Previously we have defined component selection and schematic capture part of our design, here we will conclude our report with final steps required to complete this design and a flow diagram.

1. Post fabrication of PCB for harmonic analyzer, component placement will be done.
2. Electrical circuit check has to be done for PCB (measuring voltages at different nodes and test points). This is to ensure that every section is getting appropriate signals.
3. Run a basic test code on MCU to confirm its functionality.
4. Run a test code on MCU to fetch data from ADE-7880 and match this data with measured amplitude of signals at test points.
5. Based on satisfaction with results obtained from previous test, next step is to implement firmware in a step wise manner as explained previously.
6. In case if step-4 is not giving satisfactory results AFE and signal conditioning circuit has to be optimized to improve results or the firmware section has to be optimized.
7. Once the step-5 is completed both harmonic data and power traces are collected, and is compared with a commercial harmonic analyzer to bench mark performance of our design.
8. Post assurance of results obtained from Step-5 we will deploy this system in a buildings to collect harmonic data and power consumption traces over a wide set of appliances and multiple test settings.


PHASE C VOLTAGE
VN CIRCUIT
PHASE A VOLTAGE
PHASE B VOLTAGE
PHASE-A CURRENT
PHASE B CURRENT
PHASE C CURRENT
NEUTRAL CURRENT
Power Supply Decoupling
Analog Supply
Digital Supply
REFERENCE DECOUPLING
ADE7880 RESET SWITCH
U1
ADE7880ACPZ
U17
Photon
LCDTM12864A8CCWGWA
Power Led
TACTILE SWITCH
Title
ADE7880 Evaluation Board (Designed by Manoj G.)
Size
D
Document Number
<Doc>
Rev
<1.0>
Date:
Monday, November 24, 2014
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