# HW#2: Design a Digital Stopwatch with Start/ Stop and Reset Functions

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## Course: Smart Electronics System Design Paradigm

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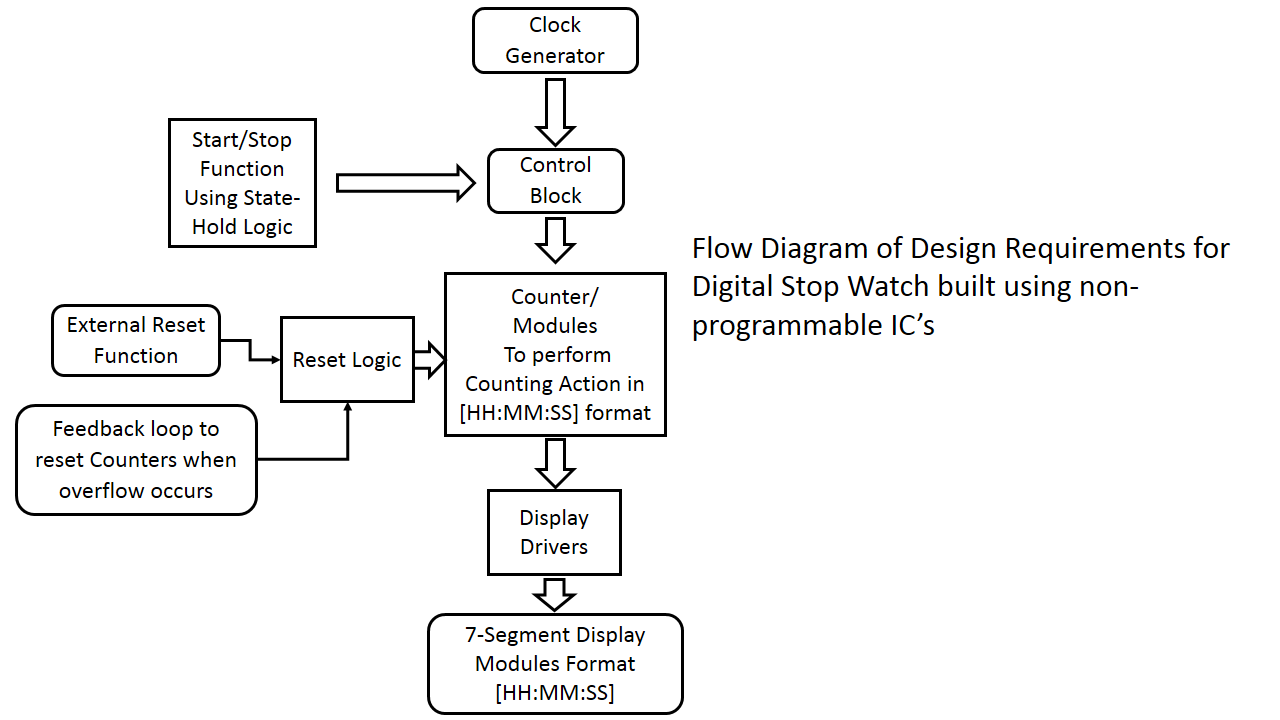
**Problem Definition:** Goal of this design project is to design a digital stopwatch using non-programmable ICs and should demonstrate full functionality of a digital stop watch, this design is given to have a thorough understanding of design principles and make note of facts which have to be taken care of while designing electronic systems e.g. handling switch de-bouncing in hardware, design toggle switches having state hold feature.

**Steps required for implementation:**

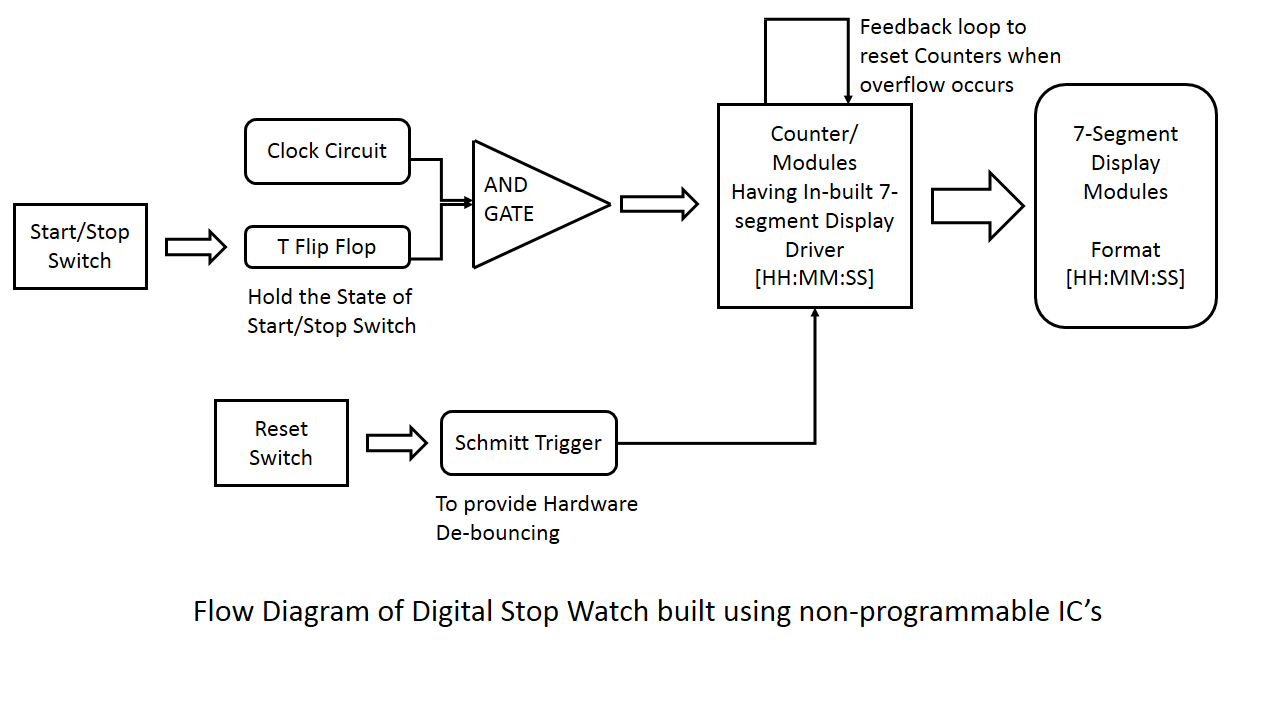
NB: Please not that individual block performing these functions and description of ICs involved is being discussed in proceeding sections.

* A clock generator is required to provide a precision square wave clock output at the rate of 1Hz, in order to drive digital stop watch. The output clock rate is dependent upon required precision of stop watch i.e. in some commercial designs of stop watch meant for bacteria decay time precision of millisecond or microsecond is required.
* Next level of this design includes a counter circuit is required which will perform the task of counting the clock sequence as in hour minute second format. These counters have to be implemented essentially using digital counter ICs instead of using microcontrollers, as the current design is supposed to be implemented using a hardcoded logic instead of relying upon programmable ICs.
* These counter blocks will perform the count sequence in HH:MM:SS format having an initial value of 00:00:00 and final value of 23:59:59 after this in next second counters will reset on to 00:00:00 again starting the new time sequence.
* The count sequence generated by these counter blocks has to be fed in to display drivers which will drive the 7-segment displays. Purpose of this is to provide control signals to display drivers to show count sequence on displays.
* Apart from this count🡪drive🡪display action we have 3 more functions which will control this digital stop watch i.e. Start, Stop and Reset.
* Start action has to be independent of clock triggering but yet to be synchronous with clock signal. In order to comply with off the shelf products we have to use a normal push button. But these buttons do not maintain their state and some digital logic is required to hold the current state.
* Stop function is just the conjugate of Start, hence can be implemented using same digital logic.
* Reset function is bit more complex to implement as in this case we have to reset all counter blocks using on-chip reset pin, but as all resent pins of counters are already being utilized to perform overflow function i.e. to resent when count sequence is 59 or 23. So we have to implement some logic to have joint reset function work in parallel with this logic. This is similar to ORing function of any logic.

**Block Diagram of Required Design Logic:**



**Flow Chart of Design Followed:**

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**Block wise description of all section is given below:**

1. **Clock Generating Block (NE555 Timer)**

NE-555 is driven in astable multivibrator mode governed by design equations as stated below. This block is used to generate 1Hz clock to drive out stop watch circuit. The clock fed in to first counter circuit is provided through an AND gate controlled a switch to START and STOP the stop watch. A T-Flip Flop is used to toggle polarity of this switch which controls the CLOCK feeding. This whole step of including T-FF is to avoid any glitches in the switching action. So in this way clock will be provided to stop watch when output from T Flip Flop is high.

Circuit Diagram for NE-555 Timer IC in astable mode is shown below.



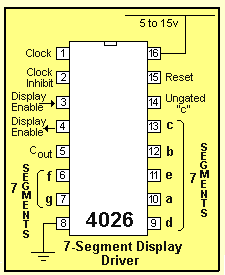


Figure: IC NE555 in Astable mode.

1. **Counter circuit IC4026**

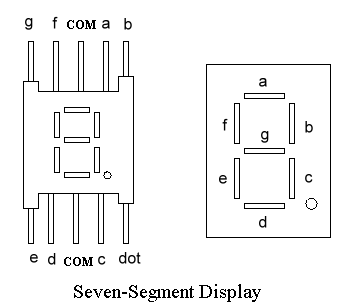
This block consists of six decade counters used with a purpose of doing the counting action in HH:MM:SS having 24 hourly display pattern. This also consists of IC4082 quad input AND gate to do the counter reset based on sequence match e.g. resetting seconds counter after 59 and hours counter after 24. The first counter in this block is driven by 1Hz clock from NE555 timer IC. This block is also having a common RESET function in order to reset all the counters with a same push button. This function is implemented by feeding overflow reset and RESET through a dual input OR gate in to Pin No. 15 of all the counters.

The labelled Pin diagram of CD4026 is shown below.



1. **7 Segment Modules**

Six 7-segment modules are used to display stop watch action in HH:MM:SS format. Having 7 control signals for 7 LEDs and all the LEDs are connected with 100 ohm series resistor to limit the current being fed in to these LED segments.

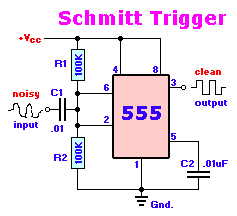


1. **Schmitt Trigger Based RESET Function**

Schmitt Trigger based Reset is used to avoid any glitches in the reset action and to provide hardware de-bouncing.

The circuit is closed whenever the normally open switch is momentary closed. When the switch is released, the contacts separate and open the circuit. The contacts are designed to be springy, so that the switch will return to its open state immediately upon being released. The same springy characteristic of the contacts that enables the switch to function in this way creates a new problem - when the switch is released, the contacts have a tendency to bounce and make a series of very short open / closed pulses called switch bounce or “chatter”. This problem can be very pronounced when using the momentary pushbutton switch as a digital logic input in a circuit. The result can be a very erratic or seemingly random functioning of the switch. “Switch de-bouncing” is the term for the technique to correct and compensate for mechanical switch bounce. There are both software and hardware methods to accomplish this. Here hardware de-bouncing has been used.

This circuit actually takes an input signal and maintains the output for a certain time period and then goes back to low state.



1. **Power Supply**

Power supply to all pins and also un-invoked pins is fed through standard signal inputs which are mounted using a standard BERG connector to +5V and GND. Good quality SMPS based supply with low ripple rate and reliable load/line regulation can be used for this circuit.

1. **ICs**

* IC CD4026: Decade Counter IC is used for counter action. Another important fact is that it also contains inbuilt BCD to 7-segment driver for controlling 7-segment displays.

External inputs given to this counter are: clock from clock circuit (containing a timer, T flip flop, AND gate, switch), Reset through OR gate, ground and +5V supply. Output of this counter is connected to the seven segment display modules.

* IC 7408: This is quad dual-input AND gate IC being used for controlling START/STOP function of this stop watch.
* NE555: This is used for Schmitt trigger as well as for generating clock for counter circuit. This is used to implement hardware de-bouncing while doing reset function as explained above.
* IC 4027: This is a JK FF being used to implement T-FF for controlling START/STOP switch. This is required to maintain the state of Start/Stop function.
* IC 74HC32N: This IC is a dual-input OR gate IC used to control provide dual reset function to counter ICs. One is through overflow due to counters and second is due to manual resets.
* IC 4092N: This IC is used to do the overflow action whenever a minute counter reaches 59 or hour counter reaches 24 this will make a reset.

**NB: All these ICs are available in local markets.**

1. **Schematic:**

Detailed schematic is attached at last.

1. **Issues and Problems faced**
   1. Initially in testing phase, most of the counter ICs were not behaving reliably when high frequency clock was applied. Also the reset function of most of ICs were not behaving properly. This was due to bouncing of switch and lack of state-hold circuit in start and stop function. After rectifying these two issues by adding a T-type flip flop next to start/stop switch to hold state of switch and also by addition of a Schmitt trigger section to implement hardware de-bouncing while doing the reset action. This whole circuit performed in a stable manner.
   2. While implementing external reset function the reset pins from all counters have to be clubbed together for implementation but while doing this the existing overflow function implemented using these reset pins will conflict with external reset action. To avoid this Oring logic was required to allow simultaneous operation of both of these reset and overflow functions.
   3. To reduce logical/wiring complexity of this design Counter IC4026 is used having inbuilt BCD to 7-Segment display drivers so external driver IC’s are not required.
2. **Alternative Approach**

Currently this design is implemented using non-programmable ICs and due to that this seems to be quite complex. Similar design can be implemented using any low cost microcontroller to do this counting and other functions (Start/Stop and Reset). This design will be far simpler in terms of board design and also in terms of debugging. But this design will require six external bcd-7segment driver ICs (BC7447) to drive six 7-segment displays.

1. **Future work or Possible Improvements**

I am not sure if some further improvement is possible apart from an efficient SMPS based power supply to power this up. I have tried to cover all design aspects which are best known to my knowledge.