Manoj S

Design Verification Engineer
manojshanmugam1729@gmail.com | 9443125626 | Trichy-621005
Linkedin | **GitHub**

Objective

Design Verification Engineer with hands-on experience in UVM testbench development and debugging. Skilled in SystemVerilog and RTL design with a strong focus on functional coverage and Assertions. Passionate about building robust and scalable testbenches. Eager to contribute to future-forward projects while continuously learning and adapting to the evolving verification techniques.

Education

Saranathan College of Engineering — Trichy
Electronics and Communication Engineering B.E — 2021 – 2025
CGPA: 7.56

S.V.M — Trichy
Higher Secondary Certificate (HSC) — 2019 – 2021
Percentage: 84.4%

Sri Akilandersawari Vidhyalaya CBSE — Trichy
Secondary School Leaving Certificate (SSLC) — 2010 – 2019
Percentage: 79.6%

Projects

Mod-14 up_down Counter Design and Verification *SystemVerilog, UVM*

- Designed SystemVerilog and UVM testbench with constrained random testing and coverage.
- Developed UVM components (driver, monitor, scoreboard, reference model) with synchronization.
- Verified RTL correctness and achieved full coverage on key scenarios.
- **Tools used:** Synopsys VCS, Synopsys Verdi

Router 1x3 Design and Verification *Verilog,UVM*

- Designed a Verilog-based packet 1x3 router with FIFO buffers, FSM control, and parity error detection.
- Developed UVM testbench covering FIFO full/empty states, soft reset, and error handling scenarios.
- Optimized synchronization for multi-channel data routing with minimal latency.
- Verified Using Fuctioal Coverage and Assertions.
- **Tools used:** Xilinx ISE, UVM ,ModelSim ,Verdi.

Experience

Trainee | ASIC Design and Verification Engineer — Jan 2025 - Present
Maven Silicon Softech Pvt Ltd.

- Pursuing professional training in RTL design and verification.
- Gaining hands-on experience with Verilog ,SystemVerilog and UVM methodologies.
- Training with industry standard tools including Synopsys VCS and Siemens Questa.

Skills

Programming Languages:	SystemVerilog, Verilog, C
Framework:	UVM
Tools:	Xilinx ISE, Synopsys VCS, Siemens Questa, Verdi

Certifications

Programming in Advanced C — T4TEQ Software Solutions

Honors & Awards

Smart India Hackathon (SIH) 2024 Achieved college level selection for the esteemed Smart India Hackathon.

Strengths

- Fast learner with no quitter attitude I solve until it's solved.
- I grow by building constant coding and practical application help me master new technologies faster.

Declaration

Date: 07-08-2025
Place: Bangalore

I hereby declare that the information furnished above is true and correct to the best of my knowledge and belief.

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