

Standard Cell Library Design of 2:1 Mux Using 45nm Technology

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Abstract

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Abstract:

Rapid technique development aimed at significantly reducing power consumption or dissipation is required for low-power VLSI designs. We suggest creating a unique multiplexer design to satisfy the rising need for low-power multiplexer cells to alleviate the threshold loss issue. The number of MOS transistors employed in this novel method is greatly reduced, which significantly reduces the threshold loss issues. To develop an ultra-low power multiplexer for the suggested circuit, we use CMOS design methods. Because of how little static power they dissipate, CMOS techniques are chosen. The suggested CMOS multiplexer employs fewer transistors than a traditional multiplexer, which normally requires 12 transistors and uses more power. As a result, compared to the conventional counterpart, speed is enhanced and power consumption is decreased. The circuit that is suggested in this study uses an XOR-based multiplexer architecture and uses less power than a dynamic multiplexer. The performance of the design is evaluated in terms of speed and latency in this study.

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