

HY428 – Lecture 2

ARM Timers, Clocks, Interrupts

Features

- Incorporates the ARM7TDMI® ARM® Thumb® Processor
 - High-performance 32-bit RISC Architecture
 - High-density 16-bit Instruction Set
 - Leader in MIPS/Watt
 - EmbeddedICE™ In-circuit Emulation, Debug Communication Channel Support
- Internal High-speed Flash
 - 512 Kbytes (AT91SAM7S512) Organized in Two Contiguous Banks of 1024 Pages of 256 Bytes (Dual Plane)
 - 256 kbytes(AT91SAM7S256) Organized in 1024 Pages of 256 Bytes (Single Plane)
 - 128 Kbytes (AT91SAM7S128) Organized in 512 Pages of 256 Bytes (Single Plane)
 - 64 Kbytes (AT91SAM7S64) Organized in 512 Pages of 128 Bytes (Single Plane)
 - 32 Kbytes (AT91SAM7S321/32) Organized in 256 Pages of 128 Bytes (Single Plane)
 - Single Cycle Access at Up to 30 MHz in Worst Case Conditions
 - Prefetch Buffer Optimizing Thumb Instruction Execution at Maximum Speed
 - Page Programming Time: 6 ms, Including Page Auto-erase, Full Erase Time: 15 ms
 - 10,000 Write Cycles, 10-year Data Retention Capability, Sector Lock Capabilities, Flash Security Bit
 - Fast Flash Programming Interface for High Volume Production
- Internal High-speed SRAM, Single-cycle Access at Maximum Speed
 - 64 kbytes (AT91SAM7S512/256)
 - 32 kbytes (AT91SAM7S128)
 - 16 kbytes (AT91SAM7S64)
 - 8 kbytes (AT91SAM7S321/32)
- Memory Controller (MC)
 - Embedded Flash Controller, Abort Status and Misalignment Detection
- Reset Controller (RSTC)
 - Based on Power-on Reset and Low-power Factory-calibrated Brown-out Detector
 - Provides External Reset Signal Shaping and Reset Source Status
- Clock Generator (CKGR)
 - Low-power RC Oscillator, 3 to 20 MHz On-chip Oscillator and one PLL
- Power Management Controller (PMC)
 - Software Power Optimization Capabilities, Including Slow Clock Mode (Down to 500 Hz) and Idle Mode
 - Three Programmable External Clock Signals
- Advanced Interrupt Controller (AIC)
 - Individually Maskable, Eight-level Priority, Vectored Interrupt Sources
 - Two (AT91SAM7S512/256/128/64/321) or One (AT91SAM7S32) External Interrupt Source(s) and One Fast Interrupt Source, Spurious Interrupt Protected
- Debug Unit (DBGU)
 - 2-wire UART and Support for Debug Communication Channel interrupt, Programmable ICE Access Prevention
- Periodic Interval Timer (PIT)
 - 20-bit Programmable Counter plus 12-bit Interval Counter
- Windowed Watchdog (WDT)
 - 12-bit key-protected Programmable Counter
 - Provides Reset or Interrupt Signals to the System
 - Counter May Be Stopped While the Processor is in Debug State or in Idle Mode



AT91 ARM Thumb-based Microcontrollers

AT91SAM7S512
AT91SAM7S256
AT91SAM7S128
AT91SAM7S64
AT91SAM7S321
AT91SAM7S32

Preliminary

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System Controller Block Diagram (AT91SAM7S512/256/128/64/321)

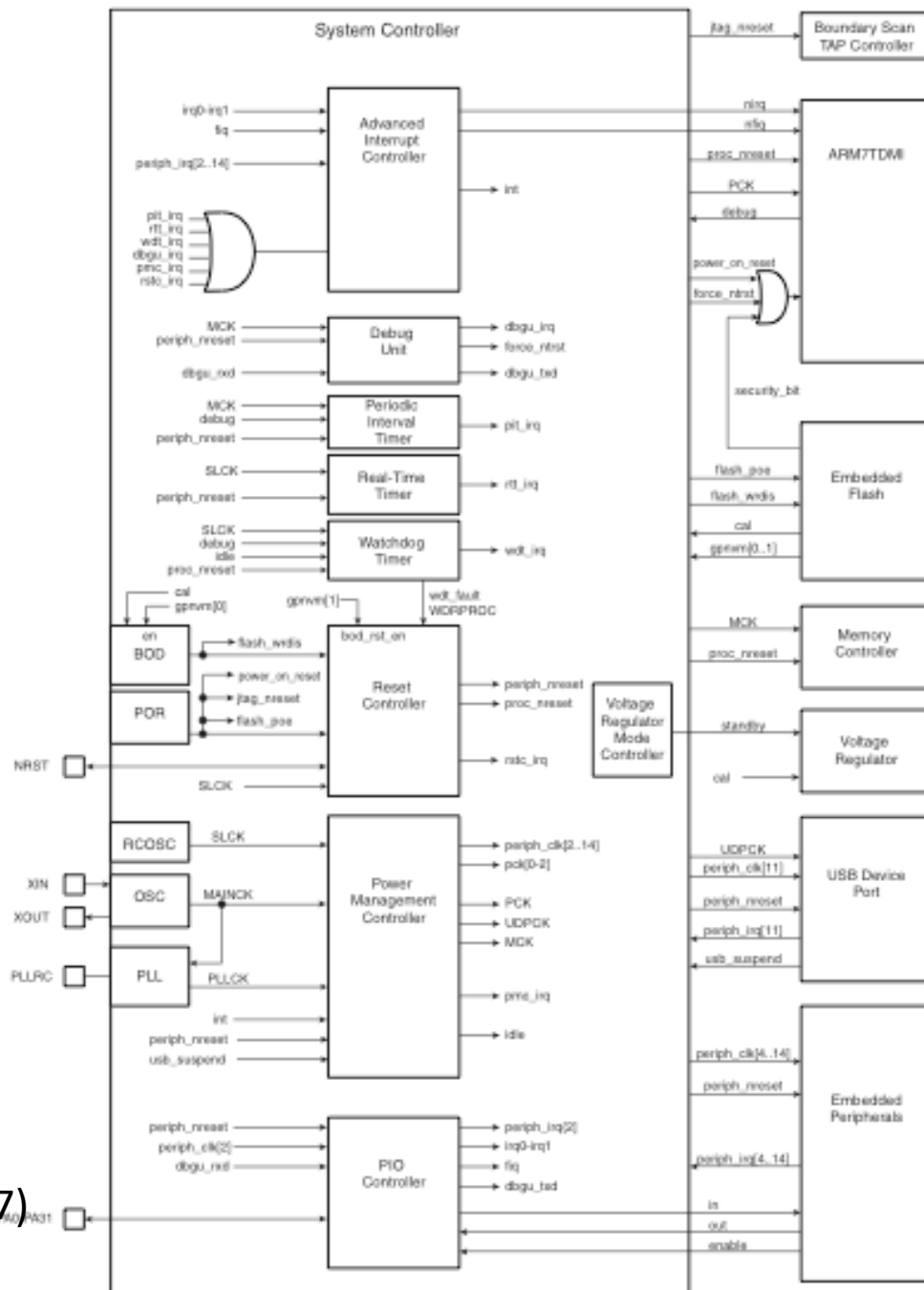
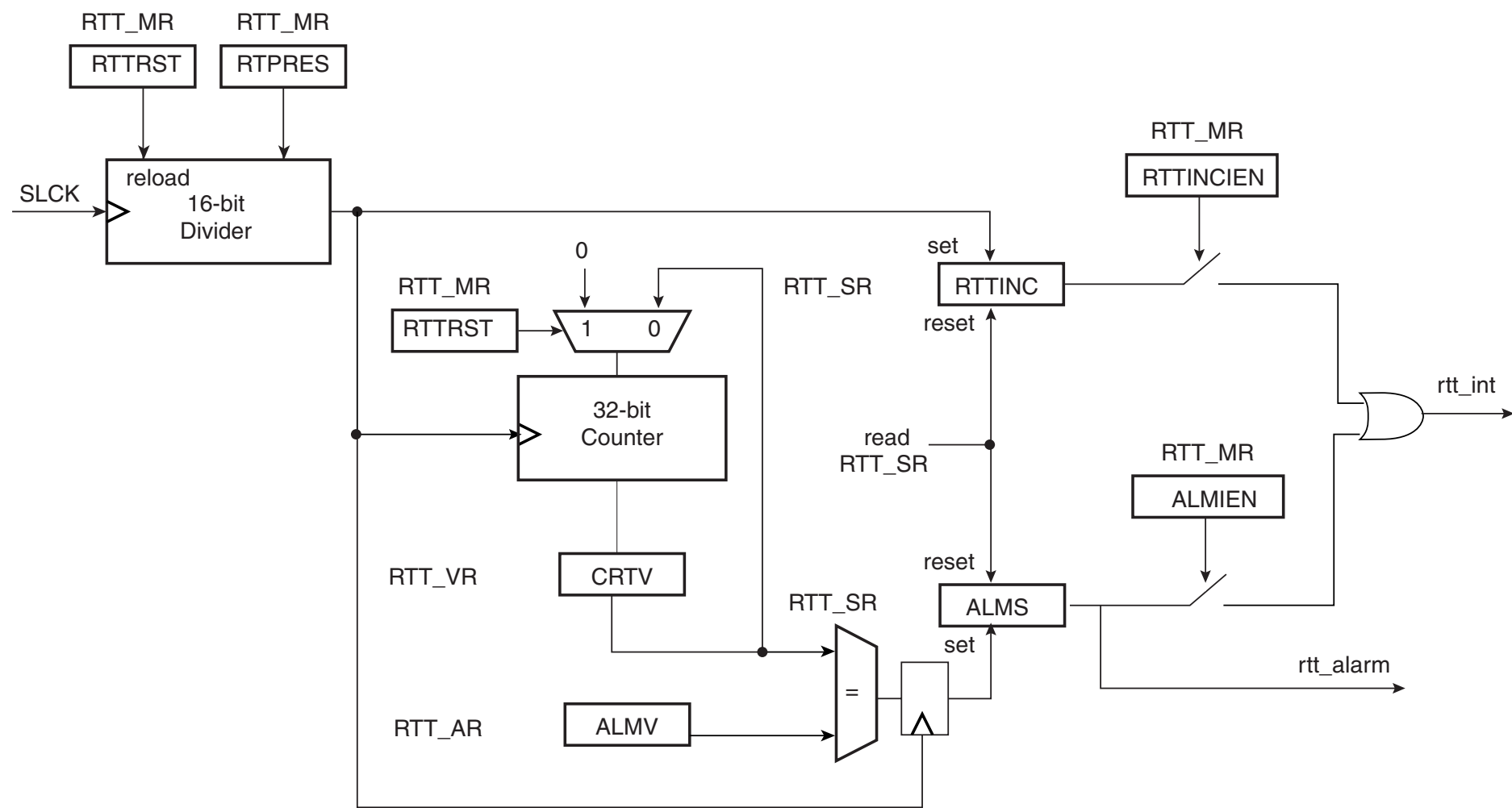


Figure 14-1. Real-time Timer



14.4 Real-time Timer (RTT) User Interface

Table 14-1. Real-time Timer (RTT) Register Mapping

| Offset | Register | Name | Access | Reset Value |
|--------|-----------------|--------|------------|-------------|
| 0x00 | Mode Register | RTT_MR | Read/Write | 0x0000_8000 |
| 0x04 | Alarm Register | RTT_AR | Read/Write | 0xFFFF_FFFF |
| 0x08 | Value Register | RTT_VR | Read-only | 0x0000_0000 |
| 0x0C | Status Register | RTT_SR | Read-only | 0x0000_0000 |

14.4.1 Real-time Timer Mode Register

Register Name: RTT_MR

Access Type: Read/Write

| | | | | | | | |
|--------|----|----|----|----|--------|-----------|--------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| – | – | – | – | – | – | – | – |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| – | – | – | – | – | RTTRST | RTTINCIEN | ALMIEN |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RTPRES | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RTPRES | | | | | | | |

- **RTPRES: Real-time Timer Prescaler Value**

Defines the number of SLCK periods required to increment the real-time timer. RTPRES is defined as follows:

RTPRES = 0: The Prescaler Period is equal to 2^{16}

RTPRES \neq 0: The Prescaler Period is equal to RTPRES.

- **ALMIEN: Alarm Interrupt Enable**

0 = The bit ALMS in RTT_SR has no effect on interrupt.

1 = The bit ALMS in RTT_SR asserts interrupt.

- **RTTINCIEN: Real-time Timer Increment Interrupt Enable**

0 = The bit RTTINC in RTT_SR has no effect on interrupt.

1 = The bit RTTINC in RTT_SR asserts interrupt.

- **RTTRST: Real-time Timer Restart**

1 = Reloads and restarts the clock divider with the new programmed value. This also resets the 32-bit counter.

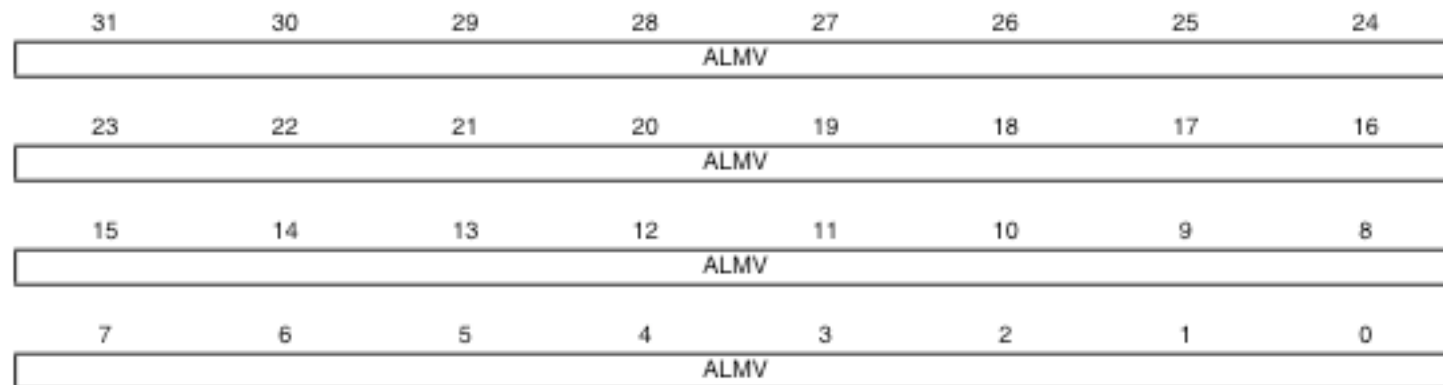
System Controller Mapping

| | | |
|---|----------|-----------------------------|
| 0xFFFF F000 | AIC | 512 Bytes/ 128 registers |
| 0xFFFF F1FF 0xFFFF F200 | DBGU | 512 Bytes/ 128 registers |
| 0xFFFF F3FF 0xFFFF F400 | PICU | 512 Bytes/ 128 registers |
| 0xFFFF F5FF 0xFFFF F600 | Reserved | |
| 0xFFFF FBFF 0xFFFF FC00 | PMC | 256 Bytes/ 64 registers |
| 0xFFFF FCFF 0xFFFF FD00 0xFFFF FD0F | RSTC | 16 Bytes/ 4 registers |
| | Reserved | |
| 0xFFFF FD20 0xFFFF FC2F | RTT | 16 Bytes/ 4 registers |
| 0xFFFF FD30 | PIT | 16 Bytes/ 4 registers |
| 0xFFFF FC3F 0xFFFF FD40 | WDT | 16 Bytes/ 4 registers |
| 0xFFFF FD4F | Reserved | |
| 0xFFFF FD60 0xFFFF FC6F | VREG | 4 Bytes/ 1 register |
| 0xFFFF FD70 | Reserved | |
| 0xFFFF FEFF 0xFFFF FF00 | MC | 256 Bytes/ 64 registers |
| 0xFFFF FFFF | | |

14.4.2 Real-time Timer Alarm Register

Register Name: RTT_AR

Access Type: Read/Write



- **ALMV: Alarm Value**

Defines the alarm value (ALMV+1) compared with the Real-time Timer.

14.4.3 Real-time Timer Value Register

Register Name: RTT_VR

Access Type: Read-only

| | | | | | | | |
|------|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CRTV | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CRTV | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CRTV | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRTV | | | | | | | |

- **CRTV: Current Real-time Value**

Returns the current value of the Real-time Timer.

14.4.4 Real-time Timer Status Register

Register Name: RTT_SR

Access Type: Read-only

| | | | | | | | |
|----|----|----|----|----|----|--------|------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| – | – | – | – | – | – | – | – |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| – | – | – | – | – | – | – | – |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| – | – | – | – | – | – | – | – |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| – | – | – | – | – | – | RTTINC | ALMS |

- **ALMS: Real-time Alarm Status**

0 = The Real-time Alarm has not occurred since the last read of RTT_SR.

1 = The Real-time Alarm occurred since the last read of RTT_SR.

- **RTTINC: Real-time Timer Increment**

0 = The Real-time Timer has not been incremented since the last read of the RTT_SR.

1 = The Real-time Timer has been incremented since the last read of the RTT_SR.

Next

- Advanced Interrupt Controller (AIC)