



The ARM Architecture

■ Introduction to ARM Ltd

Programmers Model

Instruction Set

System Design

Development Tools

- **Founded in November 1990**
 - Spun out of Acorn Computers
- **Designs the ARM range of RISC processor cores**
- **Licenses ARM core designs to semiconductor partners who fabricate and sell to their customers.**
 - ARM does not fabricate silicon itself
- **Also develop technologies to assist with the design-in of the ARM architecture**
 - Software tools, boards, debug hardware, application software, bus architectures, peripherals etc







- **ARM provides hard and soft views to licencees**
 - RTL and synthesis flows
 - GDSII layout
- **Licencees have the right to use hard or soft views of the IP**
 - soft views include gate level netlists
 - hard views are DSMs
- **OEMs must use hard views**
 - to protect ARM IP

Introduction to ARM Ltd

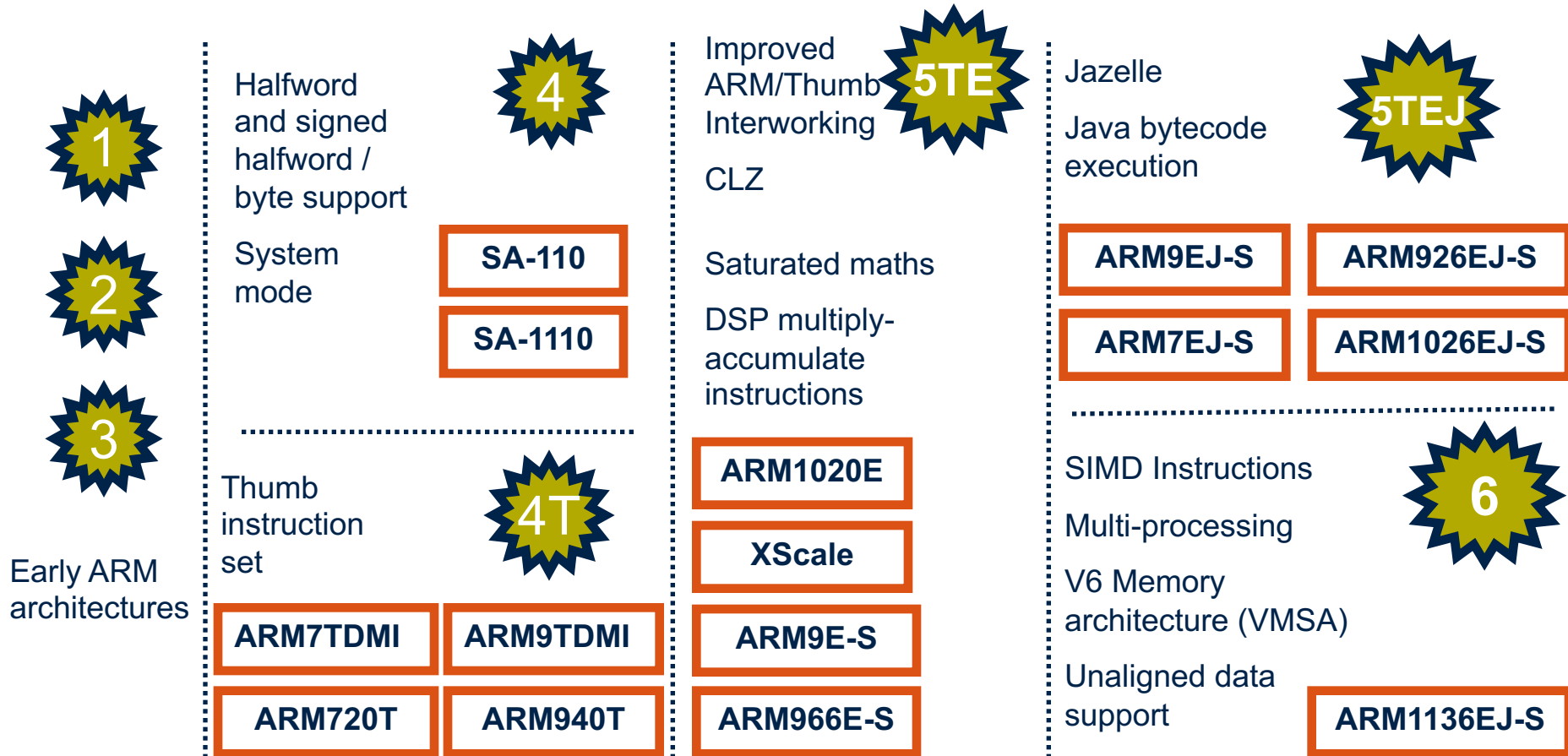
■ **Programmers Model**

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- The ARM is a 32-bit architecture.
- When used in relation to the ARM:
 - **Byte** means 8 bits
 - **Halfword** means 16 bits (two bytes)
 - **Word** means 32 bits (four bytes)
- Most ARM's implement two instruction sets
 - 32-bit ARM Instruction Set
 - 16-bit Thumb Instruction Set
- Jazelle cores can also execute Java bytecode



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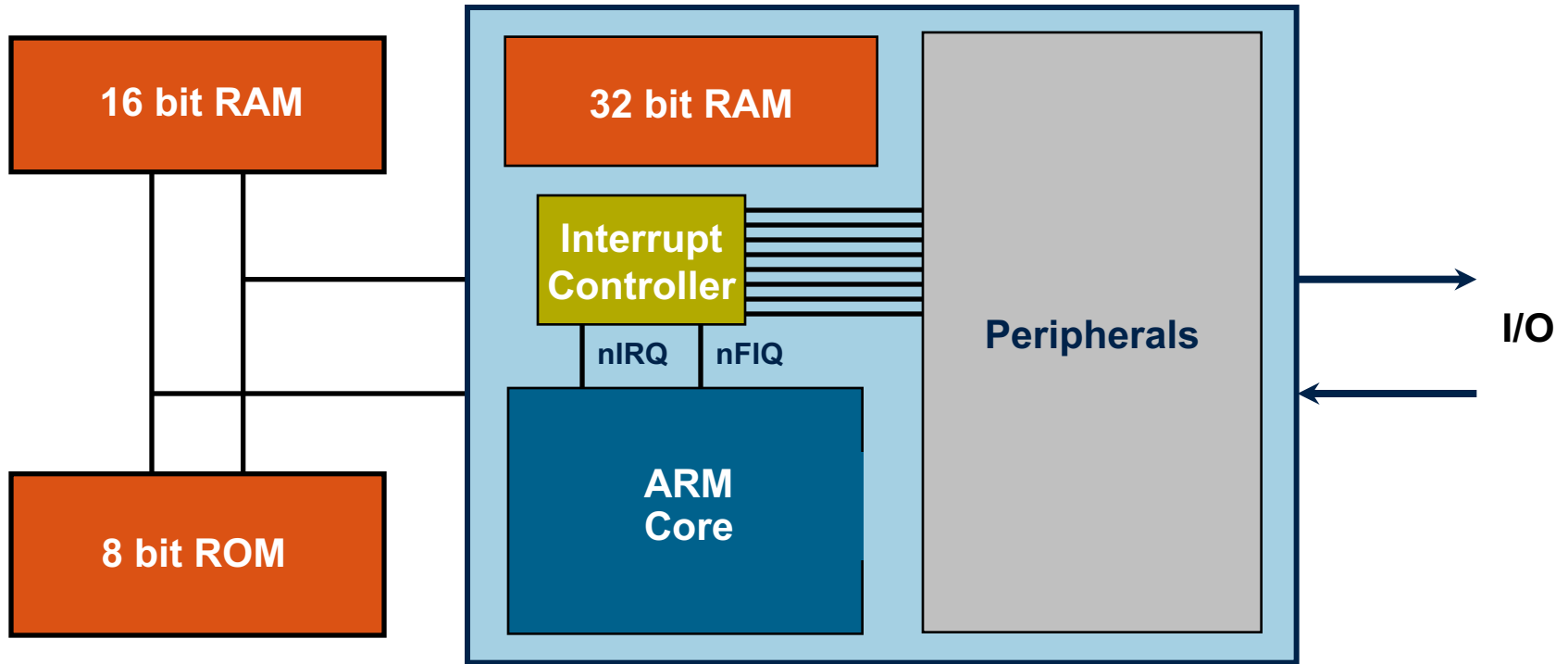
Introduction

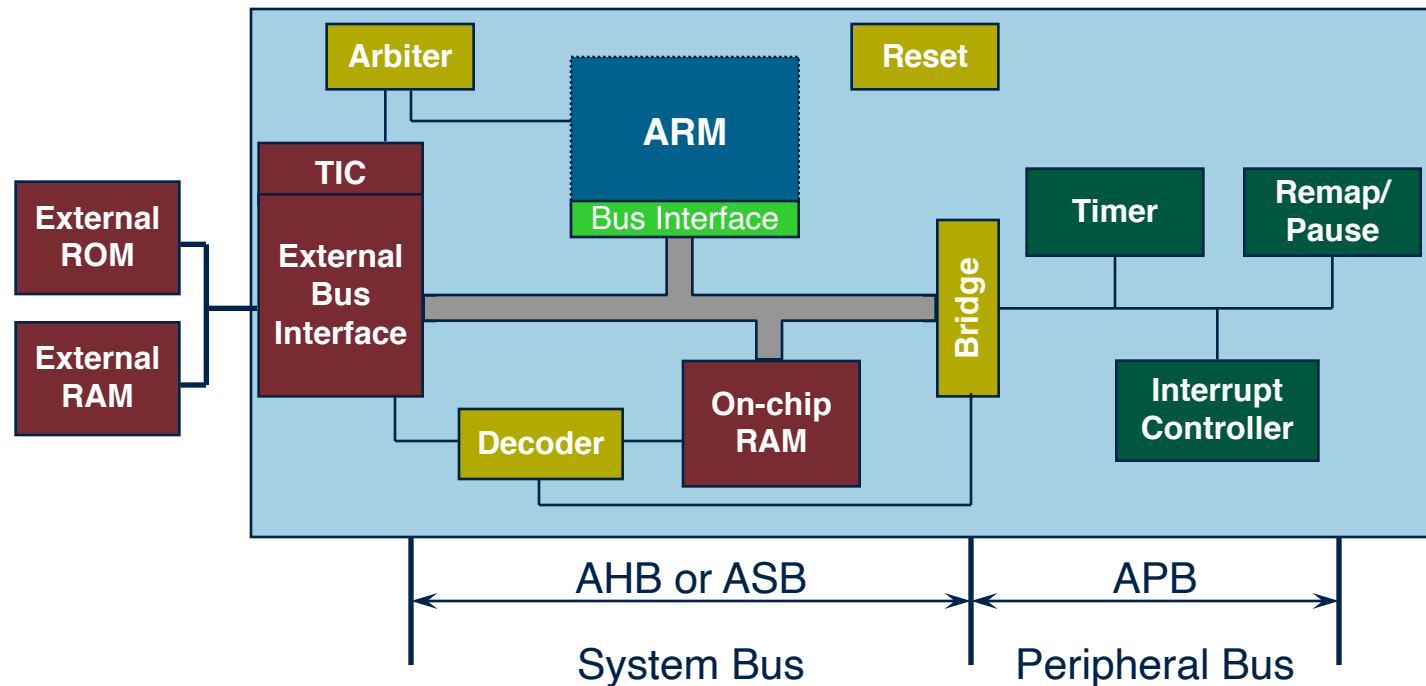
Programmers Model

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■ **System Design**

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■ AMBA

- Advanced Microcontroller Bus Architecture

■ ADK

- Complete AMBA Design Kit

■ ACT

- AMBA Compliance Testbench

■ PrimeCell

- ARM's AMBA compliant peripherals

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■ **Development Tools**

Compilation Tools

ARM Developer Suite (ADS) –
Compilers (C/C++ ARM & Thumb),
Linker & Utilities



RealView Compilation Tools (RVCT)

Debug Tools

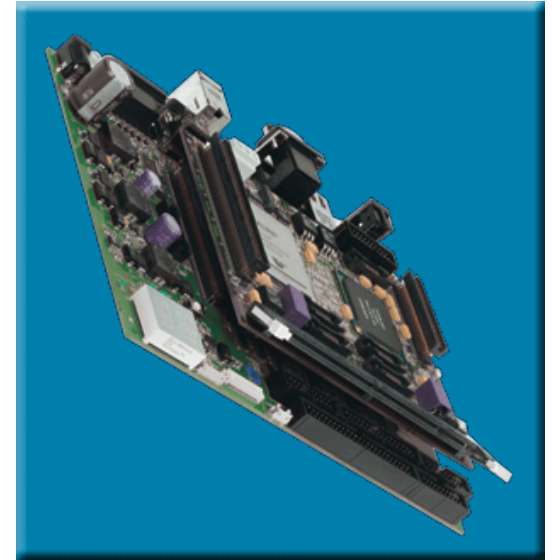
AXD (part of ADS)
Trace Debug Tools
Multi-ICE
Multi-Trace



RealView Debugger (RVD)
RealView ICE (RVI)
RealView Trace (RVT)

Platforms

ARMulator (part of ADS)
Integrator™ Family



RealView ARMulator ISS (RVISS)

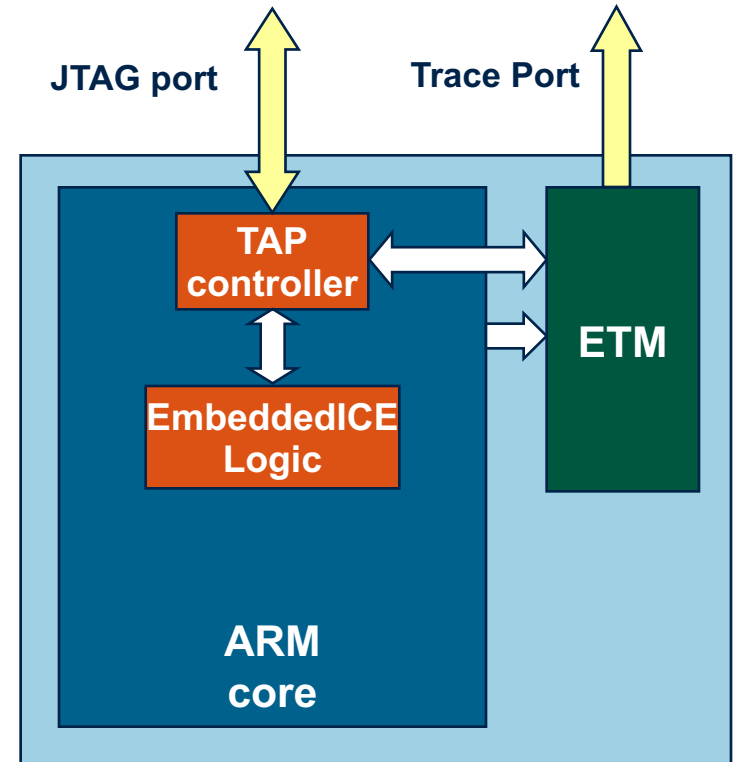
Debugger (+ optional trace tools)



Ethernet



- **EmbeddedICE Logic**
 - Provides breakpoints and processor/system access
- **JTAG interface (ICE)**
 - Converts debugger commands to JTAG signals
- **Embedded trace Macrocell (ETM)**
 - Compresses real-time instruction and data access trace
 - Contains ICE features (trigger & filter logic)
- **Trace port analyzer (TPA)**
 - Captures trace in a deep buffer



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