Digital Logic Design

Problem Set 10

Due Date: 1400/10/14

1- Implement an ALU with two 8 bit signed inputs A and B and with 4 different operation modes mentioned below. (100 points)

0- $(A \ <<< \ 3) \ + \ (B \ >>> \ 2)$

1- $\mathrm{B} + 2\mathrm{A}$

2- $-B$

3- $|3\mathrm{B} - \mathrm{A}|$

Each of the four operations should be implemented in a distinct module using dataflow coding. Then in a top module file, the modules should be connected to each other in a proper way. The final output should also be coded using dataflow.

(Note: "<<<" and ">>>" mean arithmetic shift to left and arithmetic shift to right, respectively.)

Note 1: You should at least provide two Verilog files for each question: one for the module, and one for the testbench. There should be enough test cases in your testbenches to test modules for different input and output values.

Note 2: This project must be done individually; thus, in case of any similarities between the codes provided by the students, all of those will receive a "-50".

Note 3: Upload your codes as one zip file. Each question must be placed in a separate folder inside the zip file.

Note 4: Please name your files as below:

{Your_Last_Name}.{Your_First_Name}.{Student_Number}.{Module_Name}.v

{Your_Last_Name}.{Your_First_Name}.{Student_Number}.{Module_Name}.Testbench.v

Example: Cruise.Tom.98777777.Main.Testbench.v

Note 5: Provide a report in pdf format alongside with project files. Report should be at least 3 pages, proving that your design actually works. It should contain schematics, several screenshots from simulation waves and your descriptions.

Good Luck!

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Do not hesitate to ask your question

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