**SEMICONDUCTORS AND THEIR METAL CONTACTS**

**A SUMMER INTERN REPORT**

*Submitted by*

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*in partial fulfillment of Summer Internship for the award of the degree*

**BACHELOR OF TECHNOLOGY**

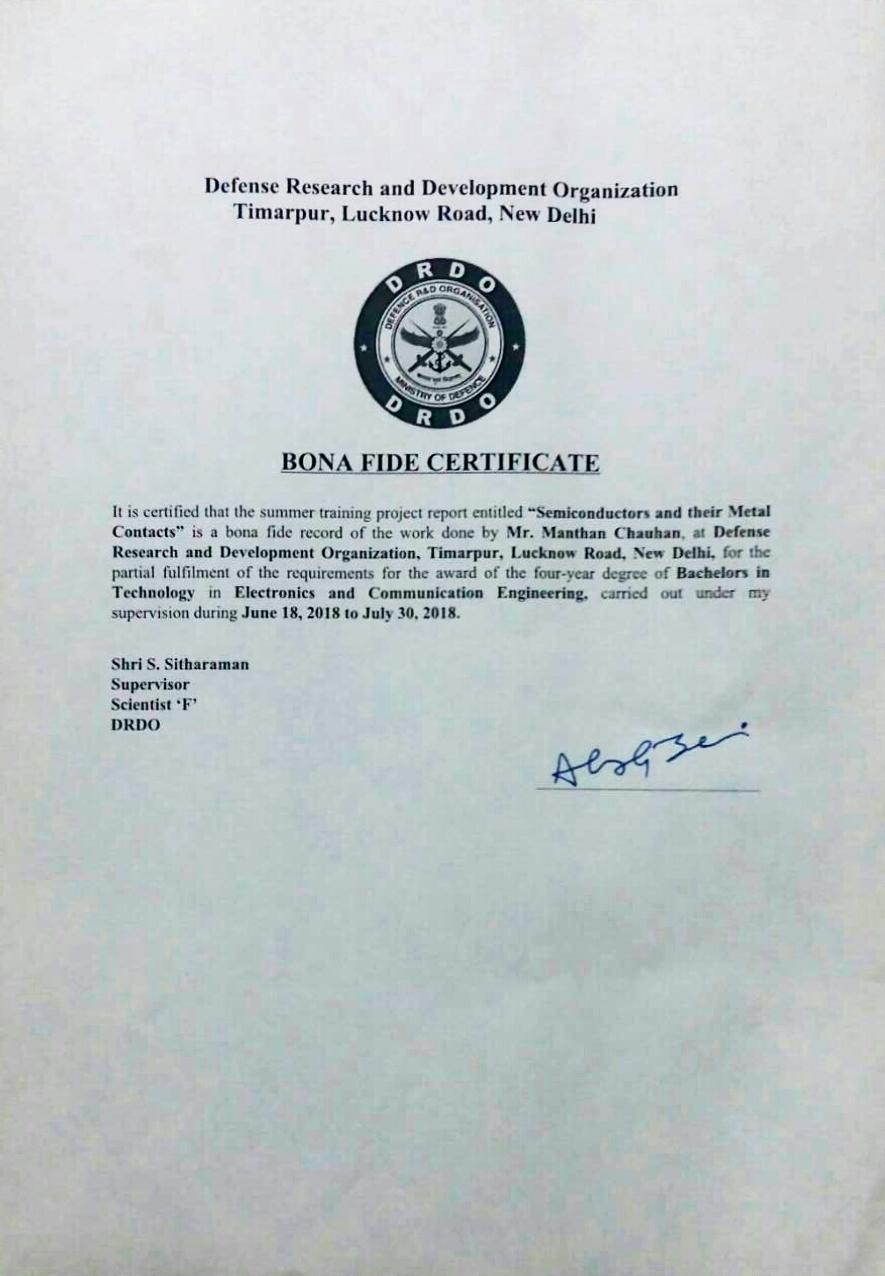
**IN**

**ELECTRONICS AND COMMUNICATION ENGINEERING**

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**Maharaja Agrasen Institute of Technology**

**Rohini, New Delhi**

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**Maharaja Agrasen Institute of Technology**

*To Whom It May Concern,*

I, **Manthan Chauhan,** Enrollment Number **02614802816,** a student of **Bachelors of Technology (ECE), a class of 2016 – 20, Maharaja Agrasen Institute of Technology, Delhi** hereby declare that the summer training project report entitled **“Semiconductors and their Metal Contacts”** is an original work and the same has not been submitted to any other institute for the award of any other degree.

Date: 28 / 7 / 2018

Place: Delhi

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***of***

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**About the Company (DRDO)**

**Defense Research & Development Organization (DRDO)** was formed in **1958** from the amalgamation of the then already functioning **Technical Development Establishment (TDEs)** of the **Indian Army** and the **Directorate of Technical Development & Production (DTDP)** with the **Defense Science Organization (DSO).** DRDO was then a small organization with 10 establishments or laboratories. Over the years, it has grown multi-directionally in terms of the variety of subject disciplines, number of laboratories, achievements and stature.

Today, DRDO is a network of **more than 50 laboratories** which are deeply engaged in developing defense technologies covering various disciplines, like aeronautics, armaments, electronics, combat vehicles, engineering systems, instrumentation, missiles, advanced computing and simulation, special materials, naval systems, life sciences, training, information systems and agriculture. Presently, the Organization is backed by over 5000 scientists and about 25,000 other scientific, technical and supporting personnel. Several major projects for the development of missiles, armaments, light combat aircrafts, radars, electronic warfare systems etc. are on hand and significant achievements have already been made in several such technologies.

Defense Research & Development Organization (DRDO) works under **Department of Defense Research and Development of Ministry of Defense**. DRDO dedicatedly working towards enhancing self-reliance in Defense Systems and undertakes design & development leading to production of world class weapon systems and equipment in accordance with the expressed needs and the qualitative requirements laid down by the three services.

DRDO is working in various areas of military technology which include aeronautics, armaments, combat vehicles, electronics, instrumentation engineering systems, missiles, materials, naval systems, advanced computing, simulation and life sciences. DRDO while striving to meet the Cutting-edge weapon technology requirements provides ample spinoff benefits to the society at large thereby contributing to the nation building.

**Solid State Physics Laboratory (SSPL),** one of the establishments under the **Defense R&D Organization (DRDO), Ministry of Defense,** was **established in 1962** with the broad objective of developing an R&D base in the field of Solid State Materials, Devices and Sub-systems. The Laboratory has a vision to be the center of excellence in the development of Solid State Materials, Devices and has a Mission to develop and characterize high purity materials and solid-state devices and to enhance infrastructure, technology for meeting the futuristic challenges.

The major activities at SSPL include development of semi-conductor materials, solid state devices, electronic components/sub-systems and investigation of solid state materials/devices. Over the years, the Laboratory has developed core competence in the following areas: -

**Design & Development of**

* GaAs based Microwave devices and circuits
* IR – devices
* Ferrite components
* SAW devices & sensors
* MEMs components
* Materials Development & Characterization

**Vision & Mission**

**Vision**

Make India prosperous by establishing world class science and technology base and provide our Defense Services decisive edge by equipping them with internationally competitive systems and solutions.

**Mission**

* Design, develop and lead to production state-of-the-art sensors, weapon systems, platforms and allied equipment for our Defense Services.
* Provide technological solutions to the Services to optimize combat effectiveness and to promote well-being of the troops.
* Develop infrastructure and committed quality manpower and build strong indigenous technology base.

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**Chapter 1: What are Semiconductors?**

Semiconductors or metalloids as the name suggests are those materials whose conductivity lies between that of conductors and insulators. The conductivity of semiconductors lies between 10 S/cm and 103 S/cm. The number of free electrons in a semiconductor lies between 107 and 1028 electrons / m3. Silicon and Germanium are two of the most valuable semiconductor materials.

To completely understand semiconductor materials, it is important to understand the Band Theory of Solids.

**1.1 Band Theory of Solids**

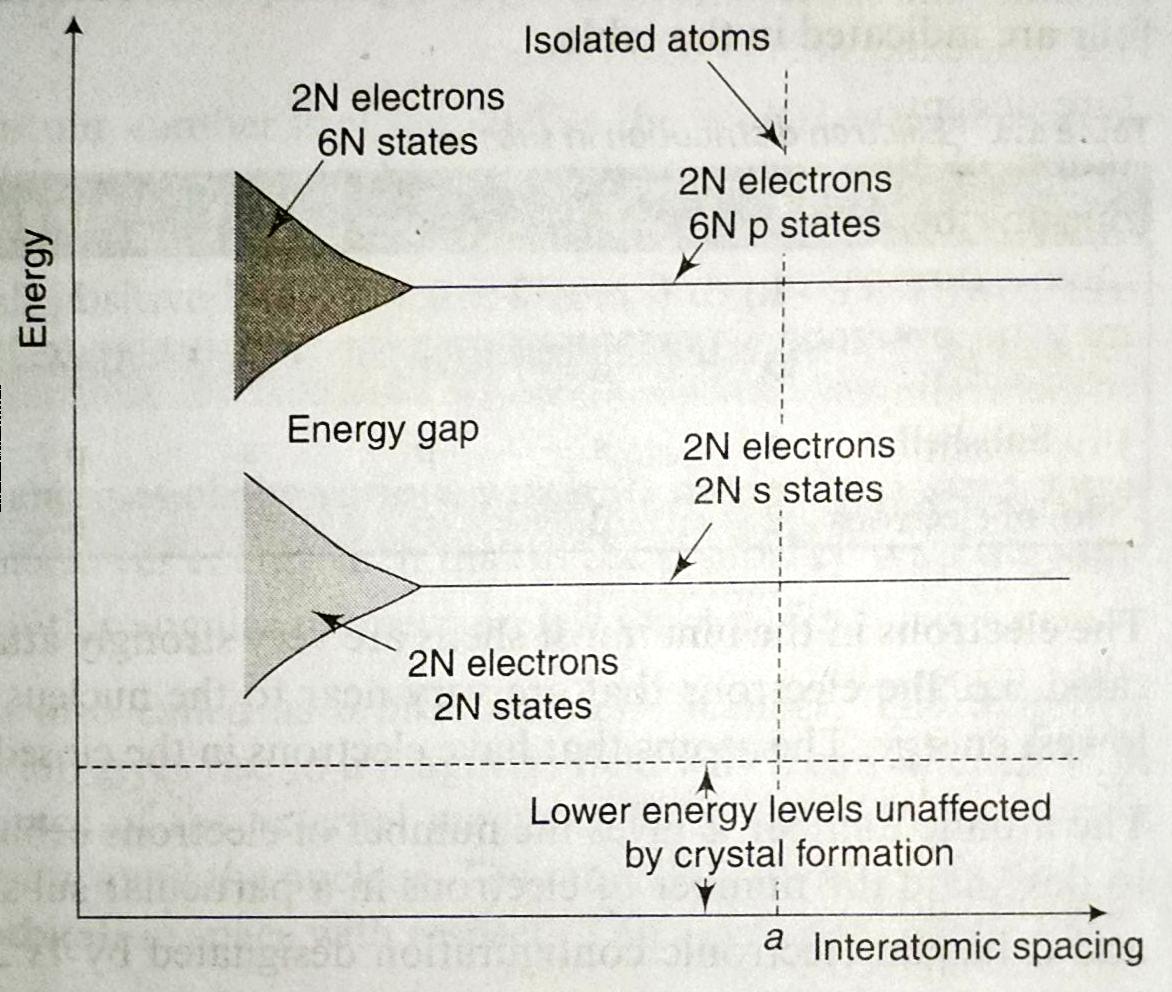
Crystalline structure in common semiconductors. All the semiconductors are naturally solids. For a gaseous state element, the energy levels are same as that for a single atom because the individual elements in gaseous state are well apart and has negligible influence on each other. However, in a crystal, the atoms are so close to each other that the resulting energy levels are modified due to interaction between the atoms. When atoms form crystals, the energy levels of inner–shell electrons are not appreciably affected, however, the energy levels of outer- shell electrons are considerably altered.

Figure 1: Formation of energy bands in solids

To understand the formation of energy bands in a crystal, consider a silicon crystal made up of N atoms. We shall also assume that the interatomic spacing can also be varied without affecting the crystal structure of the solid. For a large crystal spacing ‘a’ in the figure shown (figure 1), the interaction between the atoms is negligible, and the overall energy levels are same as that of an individual atom. Hence, the crystal consists of outermost subshells 3s and 3p containing 2N electrons each.

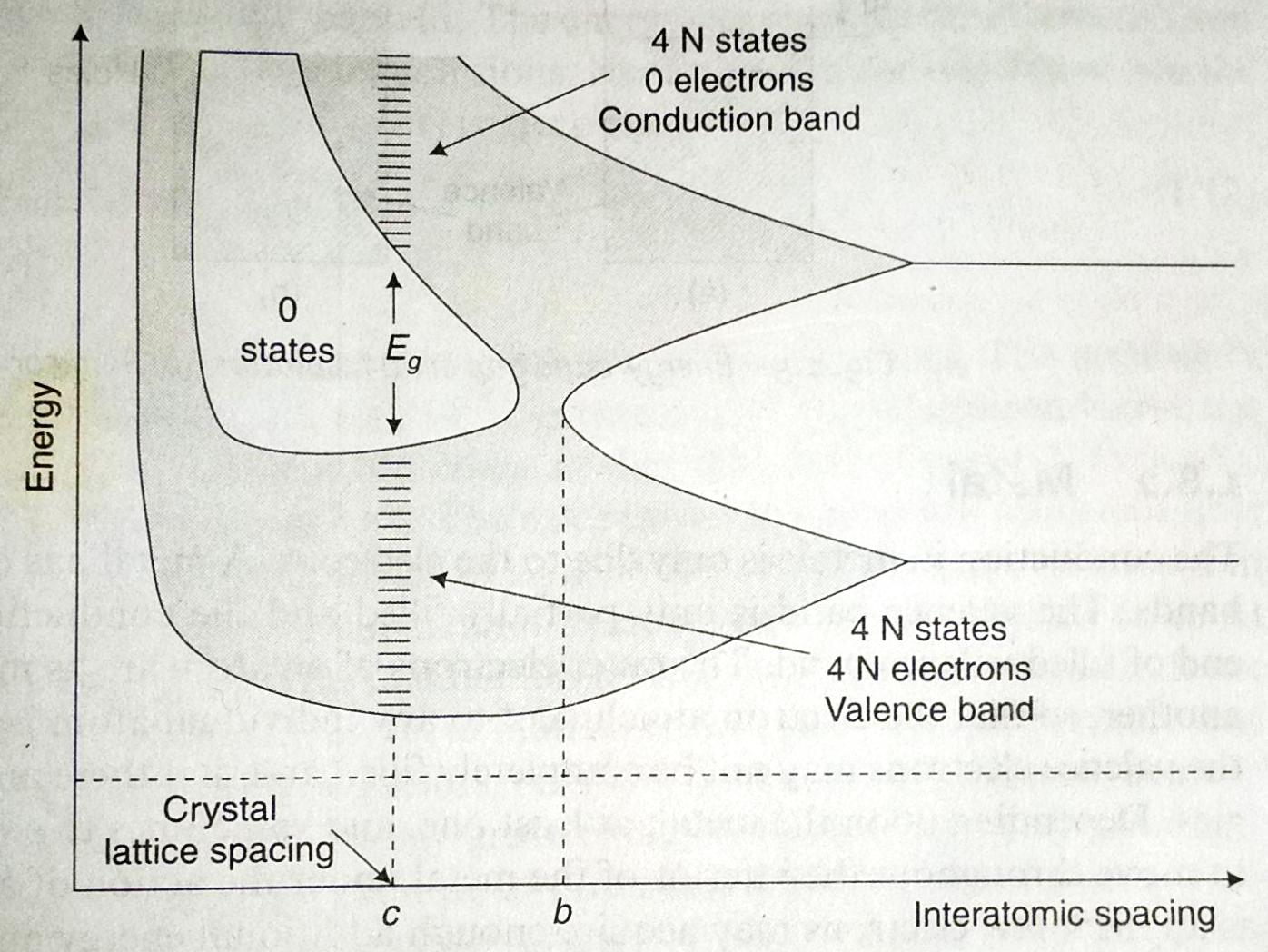
If the interatomic spacing is decreased, the interatomic interaction will increase. Due to this the energy states spread out to form a band of energy. This band is called *energy band*. An energy gap exists between the two energy bands and this energy gap is called *forbidden energy gap*. As no electron exists in this region.

Figure 2: Energy bands structure in solids

The forbidden energy gap decreases as the interatomic spacing is reduced and becomes zero at some interatomic spacing ‘b’. Under such circumstances 6N p states merge with 2N s states giving a total of 8N states. Half of these 8N states are occupied by available 4N electrons. These electrons now belong to neither the s subshell nor the p subshell but to the crystal as a whole.

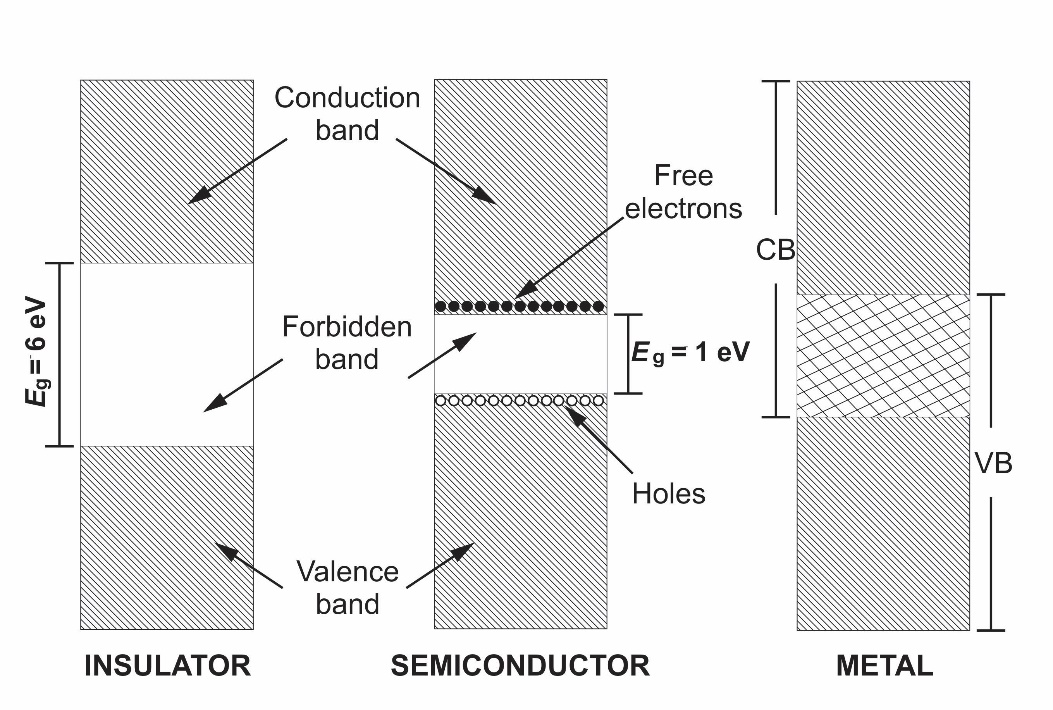
At the typic interatomic spacing ‘c’, the lower energy band contains 4N states filled by all the 4N electrons. This lower energy band is called *valence band*. The upper energy band contains 4N empty states and is called *conduction band*. The energy bands are separated by *forbidden energy gap*. Electrons if any in the conduction band, contribute to the conduction of electric current through the crystal. At typical interatomic spacing ‘c’ energy band structure can be simplified as shown.

Figure 3: Simplified structure of energy bands in solids

The most practical semiconductors silicon and germanium, have value of Eg 1.21 eV and 0.785 eV, respectively, at 0-degree Kelvin. Energies of this magnitude cannot be acquired at low temperatures.

Thus, at low temperatures the valence band remains full and the conduction band remains empty, thus, semiconductors are insulators at low temperature. As temperature increases electrons in valence band acquire sufficient energy and jump to the conduction band. The conductivity of semiconductors increases with temperatures, this ability to control the concentration of charge carriers makes semiconductors of great technological importance.

**1.2 Classification of Semiconductors**

Semiconductors are classified as *intrinsic* and *extrinsic* semiconductors.

**Intrinsic semiconductor:** A pure semiconductor is called an intrinsic semiconductor. At room temperature some of the electrons of valence band may acquire sufficient energy and jump to conduction band to form free electrons. Under the influence of electric field, these electrons give rise to a small electric current. A missing electron in valence band leaves a vacant space names as a *hole.* Holes also take part in conduction. Following table shows properties of common semiconductors.

**Extrinsic semiconductor:** Due to poor conduction at room temperature intrinsic semiconductors are not of much use. Conductivity of intrinsic semiconductor is increased by adding a small amount of impurity, this process of adding impurities is called *doping* and the impure semiconductor is called extrinsic. The amount of impurity is as small as 1 to 2 atoms of impurity per 106 atoms of intrinsic semiconductor.

Depending on the type of impurity added, extrinsic semiconductors can be classified as N-type or P-type.

**N-type semiconductor:** A small amount of pentavalent impurities such as phosphorus are added to the pure semiconductor to get a N-type semiconductor. When pure silicon is doped with phosphorus, each phosphorus atom makes covalent bonds with its adjacent four silicon atoms. Thus, four valence electrons of phosphorus make covalent bonds with adjacent silicon atoms and one valence electron is left free.

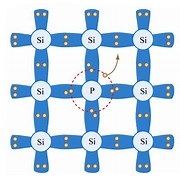
****This free electron can be easily excited from valence band to conduction band. On giving one electron, the donor becomes fixed positive ion. In N-type semiconductors the number of electrons far exceeds the number of holes, therefore for N-type semiconductors, electrons are majority carriers and holes are minority carriers.

Figure 4: Structure of N – type Silicon

**P-type semiconductor:** A small amount of trivalent impurity is added to pure semiconductor to obtain P-type semiconductor. When pure semiconductor like silicon is doped with a trivalent impurity like boron, the three valence electrons of boron form three covalent bonds with adjacent silicon atoms leaving one bond incomplete which gives rise to a hole and a negatively charged fixed ion. This hole is free and can take part in conduction.

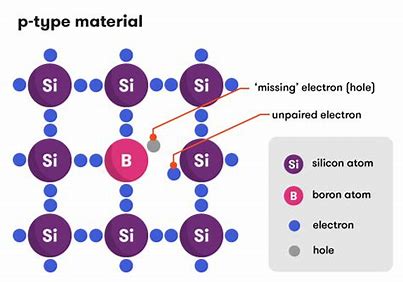
As the number of holes is very much greater that number of electrons, for P-type semiconductors, holes are majority carriers and electrons are minority carriers.

Figure 5: Structure of P-type silicon

**1.3 Energy Distribution of Electrons**

The energy distribution of electrons in a system with thermal equilibrium can be represented as

Where is the number of electrons per cubic meter whose energies lie in the interval , and is the density of electrons in the given energy interval.

The energy density can be represented as,

Where, is the density of energy states in conduction band and called *Fermi-Dirac function*, is the probability that a quantum energy state with energy ‘E’ is occupied by an electron. N(E) can be represented as,

Where, is a constant defined by

**Fermi-Dirac function:** As already said, the Fermi-Dirac function specifies the probability that an energy state ‘E’ will be occupied by an electron. From quantum physics,

Where represents the Fermi level for the crystal.

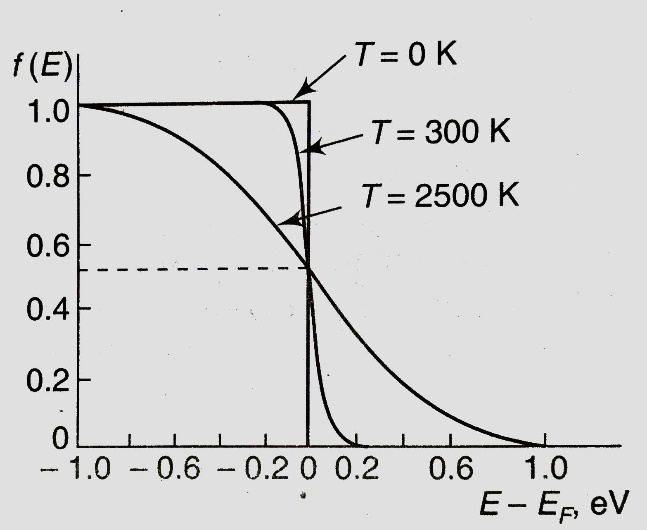
The Fermi level is the energy state with 50% probability of being filled if no forbidden band exists, irrespective of the temperature.

Figure 6: Plot of fermi dirac function

**Carrier concentration in intrinsic semiconductor:** using the equations all of the above equations,

For an intrinsic semiconductor,

Concentration of electrons in conduction band,

Where

Concentration of holes in valence band,

Where

**Fermi level in intrinsic semiconductor:** In case of an intrinsic semiconductor, number of holes is equal to number of electrons. Hence,

Substituting the expressions for and and solving for Fermi level we get,

For an intrinsic semiconductor,

If effective masses of electrons and holes are equal, then

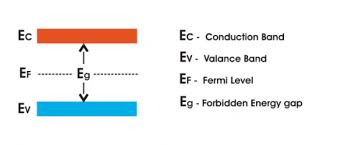
Energy band diagram of intrinsic semiconductors can be represented as,

Figure 7: Intrinsic semiconductor

**Fermi level in extrinsic semiconductor:** In case of an N-type semiconductor, due to large number of donated electrons, if is the donor concentration,

Substituting the expression for and solving for Fermi level we get,

For a N-type semiconductor,

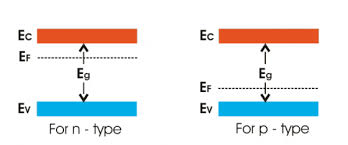
Similarly, for a P-type semiconductor,

Figure 8: extrinsic semiconductor

**Movement of with temperature:** As temperature increases a greater number of electron-hole pairs are formed. At very high temperature, the concentration of thermally generated electrons and holes will be far greater than the concentration of donor electrons or acceptor holes. In such a case,

Thus, the semiconductor becomes essentially intrinsic and returns to the center of the forbidden band. Thus, with increase in temperature, moves towards the center of the forbidden band.

**Chapter 2: Metal-Semiconductor Junctions**

Metal-Semiconductor junctions are very common in all the semiconductor devices. Depending on the doping concentration, materials and the characteristics of the interface, the metal-semiconductor junctions can act as either an ohmic contact or a Schottky barrier. Following sections will provide a close analysis of the metal-semiconductor junctions.

**2.1 Structure of Metal-Semiconductor Junction**

A metal-semiconductor junction consists of a metal in contact with a semiconductor. The structure of a typical metal-semiconductor junction in as shown,For a N-type semiconductor, the active junction is the interface between the semiconductor and the metal which acts as anode. The other interface is an ohmic contact. Whereas, for a P-type semiconductor, the active junction is the one between semiconductor and cathode.

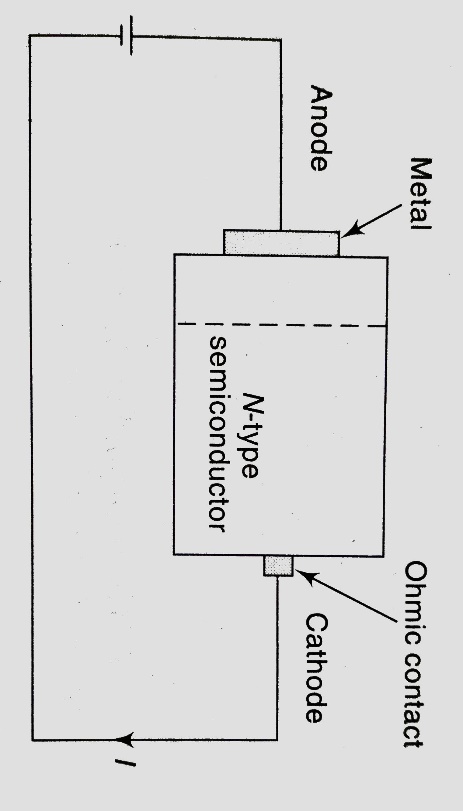
While the other junction is an ohmic contact. Active junction is the one which has some potential drop. There is no potential drop at ohmic contacts. The energy band diagram of the metal-semiconductor junction will help to differentiate between Schottky barriers and ohmic contacts.

Figure 9: Metal- semiconductor junctions

**2.2 Energy Band Diagram**

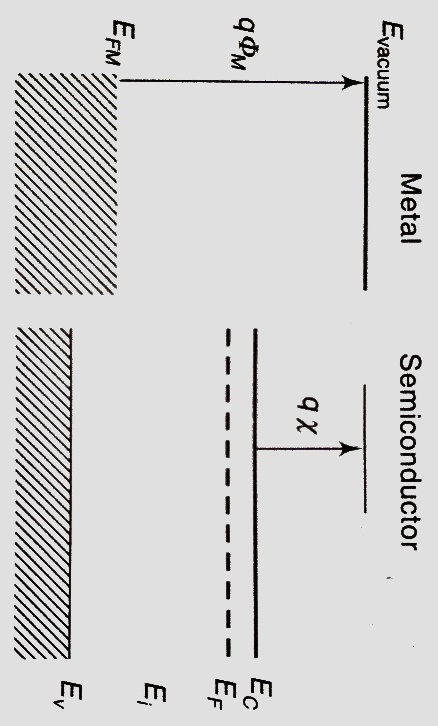
The energy band diagram of a metal-semiconductor junction helps in identifying whether it is a Schottky barrier or ohmic contact. The energy bands of metals and semiconductors are as shown. The energy levels are aligned at same vaccum level. Here, is the metal work function and, is the electron affinity for the semiconductor.

Figure 10: energy band diagram before the establishment of thermal equilibrium

Let us say, the metal and the semiconductor are joined but the thermodynamic equilibrium is yet to be established. At this position, the metal-semiconductor junction can be represented as shown in the figure.

 Let us define the *barrier height* as the potential difference between metal fermi level and the band edge where majority carriers exist.

Figure 11: energy band diagram with barrier height

For a N-type semiconductor,

For a P-type semiconductor,

If the metal fermi level lies between the conduction band and valence band edges, the junction is considered to be a Schottky barrier. Otherwise, the junction will be considered as an ohmic contact *( is negative)*.

That is, for an ohmic contact, for a N-type semiconductor  
or, for a P-type semiconductor

Let us define another parameter , the built-in potential as the difference between metal fermi level and the fermi level of the semiconductor.

For a N-type semiconductor,

Substituting ,

For a P-type semiconductor,

Substituting ,

**2.3 Thermal Equilibrium**

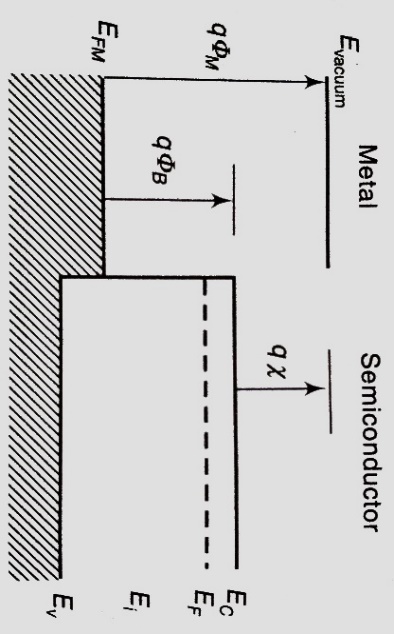
When metal and semiconductor have been just brought in contact, the fermi level is different on the two sides. The average energy of electrons and holes in a specimen is directly related to the fermi level of the specimen.

Figure 12: energy band diagram before thermal equilibrium

Hence when metal and semiconductor are brought in contact, the average energy of electrons and holes are different on the two sides.

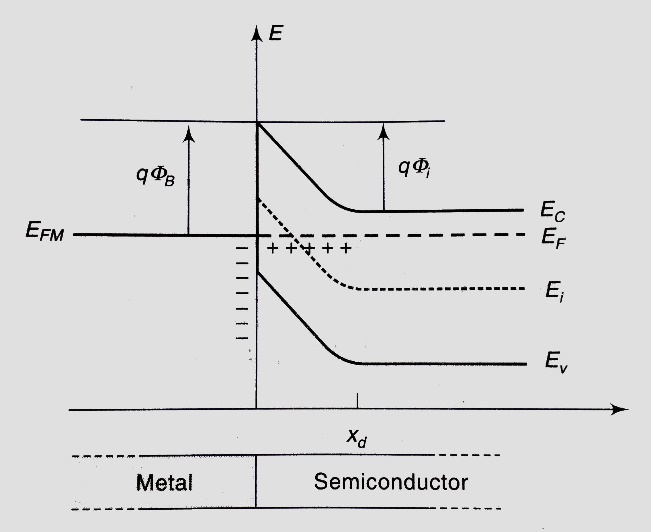
This causes a transfer of charge carriers and energy between the two sides until the fermi levels on the two sides get equalized. In the junction shown in figure 12, the average energy of electrons in the semiconductor is more than the average energy of electrons in the metal.

Figure 13: Metal semiconductor junction after thermal equilibrium

Thus, electrons flow from semiconductor to metal and holes flow from metal to semiconductor. This flow of charges continues until the average energy of charge carriers equals on both the sides. Thus, fermi level becomes constant throughout the sample.

As a result of flow of electrons from semiconductor to metal, a depletion region of width *xd*, with uncompensated positive charge is formed.

In metal, the flow of electrons forms a negative charge layer. This results in an electric field and hence the band edges are lowered in the semiconductor. Due to the electric field in the depletion region the energy bands in semiconductor are bent. As we know,

And,

And,

Hence at the junction,

Also, as discussed before,

Since,

Thus, we can say,

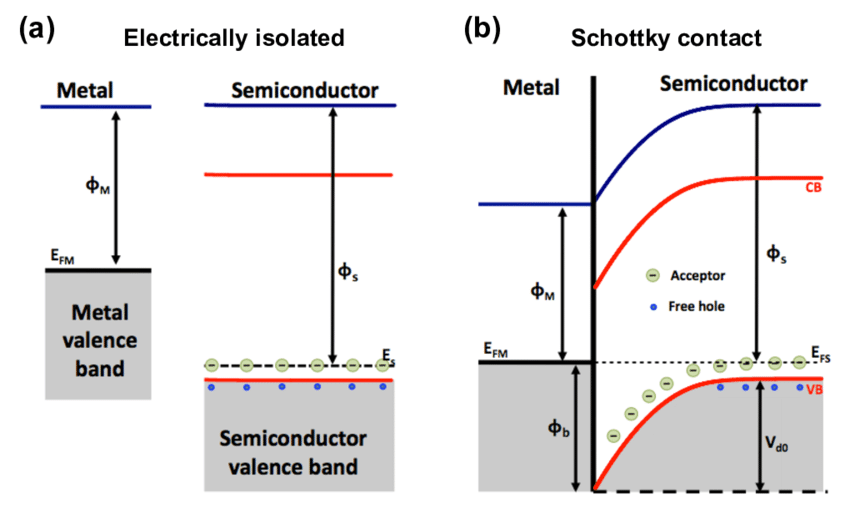
The Schottky barrier between a metal and a P-type semiconductor is as shown,

Figure 14: Metal-semiconductor junction in P-type semiconductor

**2.4 Schottky Junction under Forward Bias and Reverse Bias**

When an external bias is applied, the metal-to-semiconductor barrier remains unchanged, whereas, the semiconductor-to-metal barrier either increases or decreases.

**Forward Bias:**

In a forward biased Schottky junction the external bias is applied in such a way that it opposes built-in potential. Since the region with highest resistivity is the depletion region, most voltage drop is across depletion region. The fermi levels are no longer lined up but are shifted with respect to each other and the depletion region is narrowed.

As the metal is positively biased with respect to the N-type semiconductor, the fermi level of metal is lowered due to the application of the positive bias. Thus, there is a net difference between the fermi level on both sides. Thus, there is current from N-type semiconductor to metal through the junction. Energy band diagram of metal to N-type semiconductor Schottky barrier with external bias , is as shown in the adjoining figure.

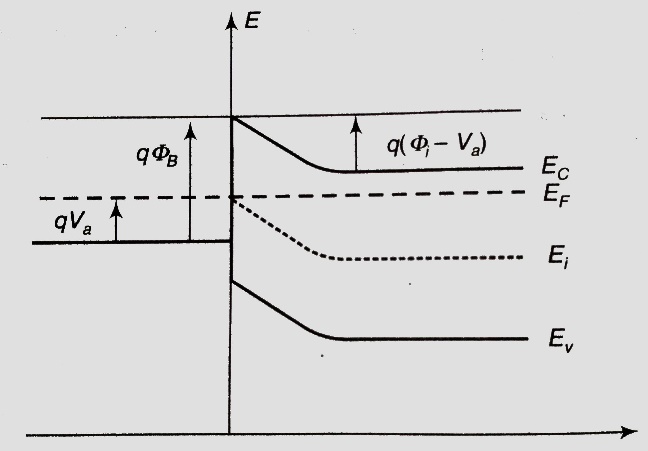


Figure 15: Schottky junction in forward bias

**Reverse Bias:**

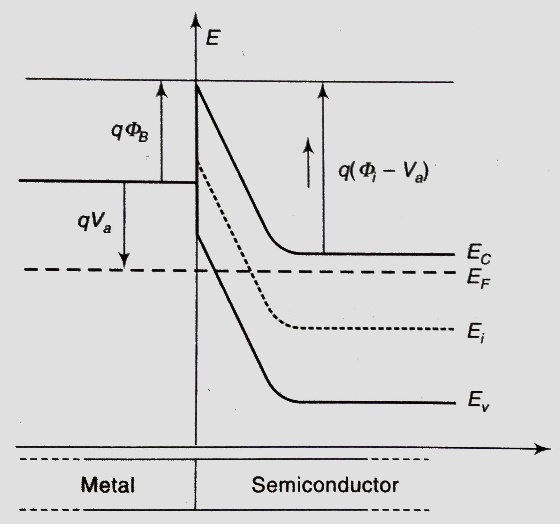
If the applied external bias supports the built-in potential, the Schottky junction is said to be reverse biased. This again causes relative shift between the fermi level on the two sides of the junction. In reverse bias, the depletion region becomes wider.

Figure 16: Schottky junction under reversed bias

If metal is connected to negative bias with respect to the N-type semiconductor, the junction is said to be reverse biased.

The fermi level of the metal is increased which repels the electrons in the semiconductor even more. Due to this, the depletion region becomes wider and the potential barrier is raised. However, the barrier on the metal side remains unchanged and limits the flow of electrons.

A few electrons in metal acquire sufficient thermal energy to overcome the potential barrier, this results in a small current, this phenomenon is called *thermionic emission*.

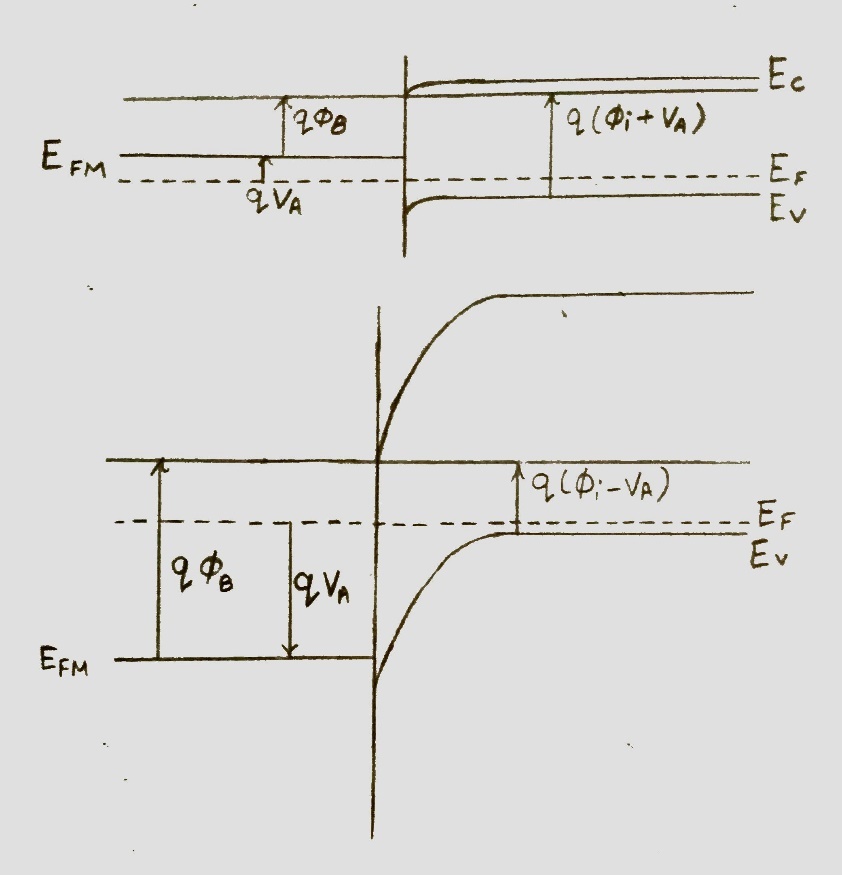
**Junction between metal and P-type semiconductor under forward bias:**

Figure 17: Schottky junction under forward bias

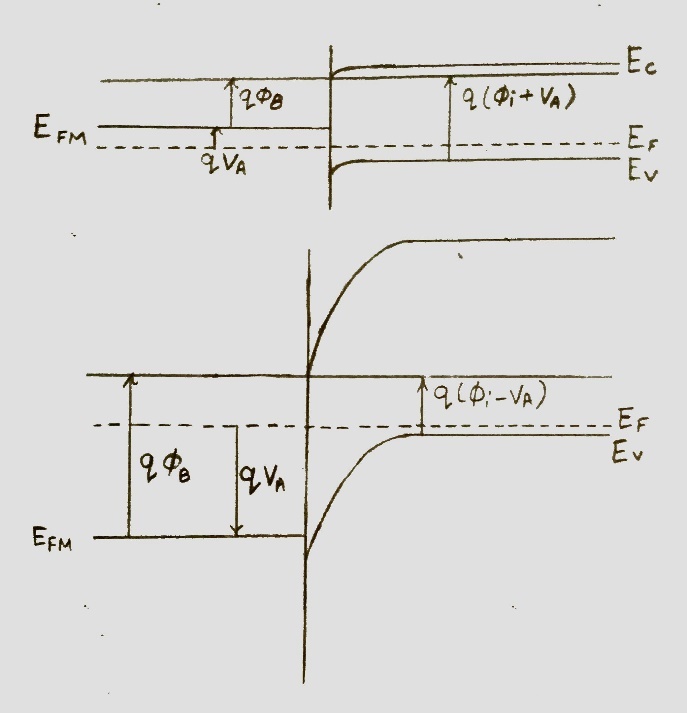
**Junction between metal and P-type semiconductor under reverse bias:**

Figure 18: Schottky junction under reversed bias

**2.5 Schottky Diode:**

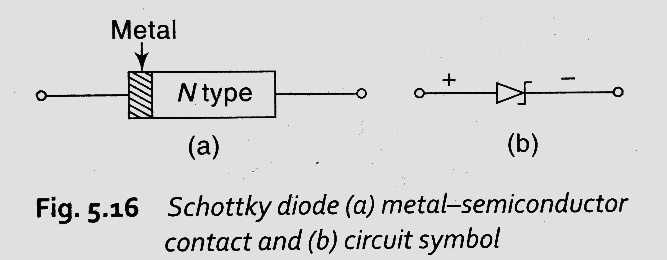
Schottky barrier diode is the extension of an old semiconductor device called point contact diode. In point contact diode, the metal semiconductor junction was a point but in Schottky barrier diode, the metal semiconductor junction is a surface. The Schottky diode is formed when a metal, like aluminum, is brought in contact with a moderately doped N-type semiconductor. It is a unipolar device because it has electrons as majority charge carriers on both sides of the junction.

Figure 19: symbol of Schottky diode

The advantage of Schottky barrier diode is that, there is no significant current form metal to semiconductor in reverse bias. Thus, the delay present in p-n junction diode due to hole-electron recombination time is absent here. Due to the large area between metal and semiconductor, forward resistance is lower, and so is noise, as compared to point contact diode.

The forward current is dominated by electron flow from semiconductor to metal, and the reverse current is mainly due to electron flow from metal to semiconductor. As there is very little minority injection form metal to semiconductor, Schottky diodes are called majority carrier devices.

Schottky barrier diode is also referred as hot carrier diode because when it is forward biased, conduction electrons on N side gain sufficient energy to cross the barrier. These electrons plunge into metal with so much energy, they are called hot carriers.

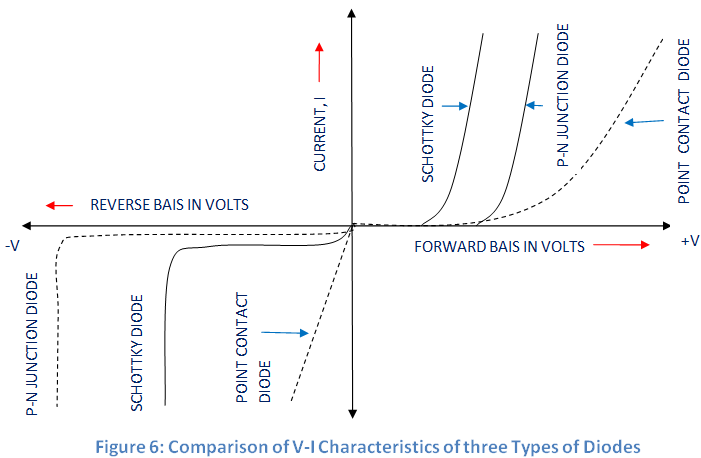
The *V-I* characteristics of a Schottky barrier diode and p-n junction diode are as shown,

Figure 20: V-I characteristics

**2.6 Key specifications of Schottky diode:**

1. **Forward voltage drop:** The voltage drop across the diode in forward bias condition is called forward voltage drop. The forward voltage drop of a diode varies according to the current being carried. Forward voltage drop is also known as turn-on voltage. Typically, turn-on voltage is around 0.2V.
2. **Capacitance:** Like any other diode, junction of Schottky diodes story electric charge and act as parallel plate capacitor. Normally, junction areas of Schottky diodes are smaller as compared to *PN* junction diode. As the capacitance of Schottky diode is dependent on its depletion width, capacitance must be specified at a particular voltage. Typical value of capacitance for Schottky diodes is several picofarads.
3. **Reverse recovery time:** It is the time taken to switch a diode from its forward conducting state to its reverse non-conducting state. The charge that flows through the junction during this time is called *reverse recovery charge.* In Schottky diodes, unlike *PN* junction diode, there is no majority carrier recombination. The reverse recovery time in Schottky diodes is only due to slight capacitive loading. Hence, reverse recovery time for Schottky diodes is as low as 100 ps to several nanoseconds. For *PN* junction diodes reverse recovery time varies from several microseconds to hundreds of nanoseconds.
4. **Working temperature:** The maximum working temperature of Schottky diodes lies between 125 to 175 ͦ C. Which is less than the working temperature of *PN* junction diodes. Due to high reverse leakage current, high temperature lead to thermal instability.
5. **Reverse leakage current:**  As seen in the V-I characteristics of Schottky diode, Schottky diodes have a high reverse leakage current. This leakage current increases significantly with increase in temperature.

Figure 21: Schottky diode

**2.7 Some Applications of Schottky Diode:**

1. **RF mixer and detector diode:** Because of its high switching speed and low noise Schottky barrier diode has many applications in radio frequencies. Schottky barrier diodes are used in high performance diode ring mixers. Low turn on voltage, high frequency capability and low capacitance of Schottky barrier diodes make them ideal for RF detectors.
2. **Power rectifier:** Due to lower forward voltage drop, Schottky barrier diodes are also used in high power rectifiers, as less power is wasted than if ordinary *PN* junction diodes were used. This also means that less heat needs to be dissipated, and smaller heat sinks may be incorporated in the design, leading to less cost and compact designs.
3. **Solar cell applications:** Solar cells are typically connected to rechargeable batteries. To avoid the reverse charge applied by the battery a diode is required in series with solar cells. Any voltage drop across the diode will result in reduced efficiency. Therefore, a diode with low voltage drop is required. The low voltage drop of Schottky diode is particularly useful in this situation.

**2.8 Ohmic Contacts**

An ohmic contact is another type of metal-semiconductor junction. It is formed by applying a metal to heavily doped semiconductor. In ohmic contacts, current is conducted in both directions with a small voltage drop across junction. The usage of ohmic contacts is to connect semiconductor devices to external circuit.

A proper choice of metal and semiconductor can offer a low resistance ohmic contact.  
A metal semiconductor contact is an ohmic contact if the Schottky barrier height is zero or negative. Thus, for a metal-semiconductor junction to behave as ohmic contact,

for a N-type semiconductor  
 for a P-type semiconductor

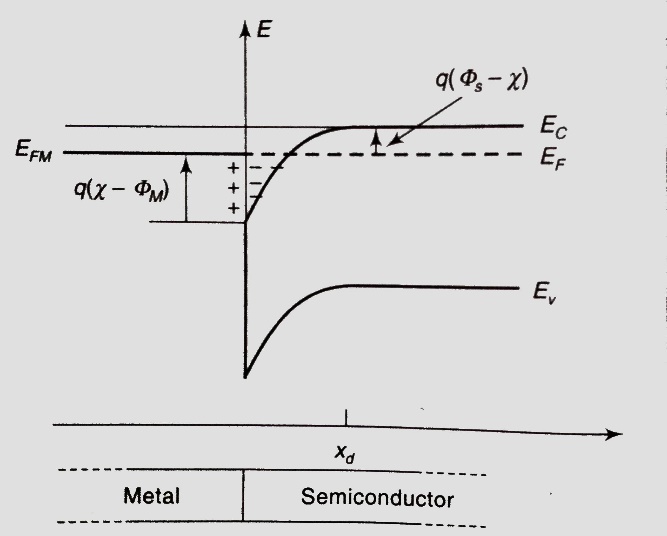
Figure 20 shows energy band diagram when , in such a case electrons flow from metal to semiconductor forming a positive surface charge layer in metal. Energy bands bend downward due to the electric field set up.

Figure 22: Energy band diagram of ohmic contact

There is no barrier to flow of electrons in both directions. The current is directly proportional to the potential across the junction.

Alternatively, contacts with thin barrier can be created by heavily doping the semiconductor through which carriers can tunnel. As doping is increased, the thickness of the barrier decreases, up-to a few Ǻ. This thickness is only about 1/50th of the wavelength of visible light. For such thin potential barriers, wave nature of electrons comes in to picture and the electrons will penetrate through the junction, increasing the tunneling current and reducing the barrier resistance. This effect is called *tunneling* of electrons.

**Chapter 3: Results**

**Device used**: BAT54SHMFH Schottky diode

**3.1 V-I Characteristics under forward bias**

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**3.2 V-I Characteristics under reversed bias**

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**3.3 Junction Capacitance under reverse bias**

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**References**

[1] S. Salivahanan and N. Suresh Kumar “Electronic Devices and Circuits”

[2] Adel S. Sedra and Kenneth C. Smith “Microelectronic Circuits”

[3] <https://en.wikipedia.org/wiki/Schottky_diode>

[4] <https://www.elprocus.com/schottky-diode-working-and-applications/>

[5] <http://www.futureelectronics.com/en/diodes/schottky-diodes.aspx>

[6] <https://en.wikipedia.org/wiki/Metal–semiconductor_junction>