Logan Manthey

Hardware Engineer - DOD Clearable - Plymouth, WI

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Education

Masters, Engineering Management, *Rose-Hulman Institute of Technology* **May 2025**
Bachelors of Science, Computer Engineering, *Rose-Hulman Institute of Technology*
Minors, Cyber Security, German

Related Courses
Advanced Microcomputers (Hardware-Software Codesign), Advanced Verilog, Embedded Systems, High-Speed Digital Design, Communication Networks, Computer Architecture I-II, Operating Systems, Digital Signal Processing, Electronic Device Modeling, Practical Security I-III, DC and AC Circuits, Object-Oriented Software Development, Engineering at Nanoscale

Relevant Work Experience

Glassboard Product Development Indianapolis, IN June 2022 - August 2023
Lead Hardware Engineering Intern
Worked on a team to develop new products from customer specifications; Designed Altium Schematics and layouts, prototyped and tested PCB assemblies, surface mount soldering, firmware and device tree development using Zephyr RTOS, wrote technical documentation, implemented and ran electronic component database for on-hand parts.

Wrote documentation on standards for Altium Designer practices and created PCB and Schematic templates. Designed A365-managed content such as device sheets and design reuse blocks. Used Electron, Javascript, and HTML to create RF hardware testing and debugging tools.

Curt G. Joa Sheboygan Falls, WI June 2021 - August 2021
Electrical Engineering Intern
Communicated across various teams including electricians, mechanical engineers, and mechanics to develop industrial automation machinery in the disposable hygiene space; worked with Allen Bradley PLC, Studio 5000 Logix, Logix Emulate, RSlinx, Factory Talk, Codesys, Cognex Machine Vision Insight explorer, and VMware ESXI for remote HMI systems; troubleshooted electrical panels, setup and tested new devices, and coordinated with project management and clients

Projects and Research

- **Open Source Evolvable Hardware Toolkit:** Worked on a team with a professor at Rose-Hulman to develop and run experiments that apply genetic evolution to FPGA bit-streams. Used Python to run the evolution and program the FPGA and to take data in from the microcontroller, which gathers fitness data about the circuit. Currently working on creating a custom board in KiCAD to gather more fitness data from the FPGA and to add more features that can allow further experiments

- **RSA Hardware Accelerator:** Used hardware-software co-design on a Xilinx Vivado Zybo Z7 development board through custom IPs made with verilog to increase the performance of the RSA algorithm. Wrote software that interacted with custom IPs through address mapping in C

- **Reduced Instruction Set Processor:** Utilized Model-Sim and Quartus Prime to design and implement multi accumulator and load-store processors in Verilog with custom assembly languages. Tested using various programs which had loops, and procedure calls, and benchmarked using various algorithms. Wrote supporting documentation in LaTeX which included an assembly language guide and overview of the hardware

- **RISC-V ROP Gadget Finder** Worked on a team to create Python scripts that disassembled compiled RISC-V 64-bit binaries and found gadgets inside of them to exploit return-oriented programming.

- **Portfolio Website:** Used HTML, CSS, and Javascript to create both a front and backend of a portfolio website and used Firebase for hosting: https://portfolio-website-ltm.web.app/

Activities and Honors

Cyber Security Club Vice President, Treasurer Rose-Hulman Institute of Technology 2021 - Present
National Collegiate Cyber Defense Competition, HACK-A-SAT

Lambda Chi Alpha - Theta-Kappa Zeta Member Rose-Hulman Institute of Technology 2023 - Present
Formula SAE, Electrical Team Rose-Hulman Institute of Technology 2020 - 2021
Dean's List Rose-Hulman Institute of Technology 2020 - 2021, 2023
FIRST Robotics Team Captain RoboRiot 3418 Programming Team Captain for 3 years 2017 - 2020