Abhishek **Bhattacharyya**

Computer Engineering · PhD Student

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Summary

I am a third year PhD student at the University of Wisconsin-Madison developing efficient hardware architectures for ultra-low power edge devices. I love to find new problems to solve. Recently, I also find myself intrigued by the challenges involved in achieving realistic quantum computing in the NISQ-era.

Education

University of Wisconsin-Madison — *Madison, WI*

PhD in Computer Engineering — *Aug 2018 - Exp. May 2023*

North Carolina State University — *Raleigh, NC*

M.S. in Computer Engineering — *Aug 2011 - Aug 2013*

Gauhati University — *Assam, India*

B.E. in Electrical Engineering — *May 2006 - May 2010*

Research Projects

Energy efficient architectures for energy-harvesting devices

Advisor: Joshua San Miguel

Intermittent Computing

- Using legacy architecture concepts like register renaming and liveness analysis to achieve reliable computation in an extremely energy-constrained environment
- Apart from low power mobile applications, these solutions can also mitigate issues in supporting machine learning inference at the edge

Fast and scalable simulation of NISQ-era Quantum Computers

Advisor: Joshua San Miguel

Quantum Computing

- Using concepts of stochastic computing to accelerate simulation of quantum circuits

Processor-Neural Engine System for digit recognition on an FPGA

Advisor: Parmesh Ramanathan

Digital Engineering Laboratory (ECE 554)

- Designed a 24-bit ISA for CPU and Neural Engine
- Weights for the neural network were loaded from an SDRAM, pre-loaded on reset through a serial interface from a terminal using PySerial API
- The input, fed to the neural engine, is an image from a VGA camera that is stored on the on-board block RAM after pre-processing in run-time
- The digital logic was written in Verilog. The design was synthesized and programmed using Quartus on an Altera FPGA Cyclone V board

Study of cache replacement policies in Gem5

Advisor: Matt Sinclair

Advanced Computer Architecture 1 (ECE/CS 752)

- Wrote micro-benchmarks to study cache replacement policies in Gem5
- Found bugs in cache replacement policies of Gem5 public repository source code and made fixes

Dead-word analysis for NoCs in Gem5+Garnet2.0

Advisor: Mark D. Hill

Advanced Computer Architecture 2 (ECE/CS 757)

- Did dead word analysis for the traffic induced by a 16-core X86 system with a two-level cache, the last-level cache being shared among the cores, and suggested ways to reduce power consumption
- Configured the on-chip interconnect using Garnet2.0 and used L1 caches with MESI protocol in Gem5 Ruby memory model

Study in classical simulation of quantum circuits based on stabilizer formalism

Advisor: Dieter van Melkebeek

Quantum Computing (CS880)

- Studied classical simulation of quantum circuits with an emphasis on techniques using stabilizer formalism
- Wrote a C++ simulator to simulate classically quantum circuits based on stabilizer frames and verified output with results from IBM's Qiskit

Packet Forwarding Engine

Advisor: Paul D. Franzon

Digital ASIC Design

- Designed a packet forwarding engine based on a 16-way trie search algorithm
- The RTL was written in Verilog
- The circuit logic was simulated in ModelSim and was synthesized using Synopsys Design Vision

Implemented Load Speculation Techniques on Simplescalar

Advisor: Eric Rotenberg

Advanced Microarchitecture

- Implemented “always stall”, “always speculate” and a hybrid approach that involved a dedicated memory dependence predictor using store sets in Simplescalar simulator
- Did performance analysis with SPEC2K benchmarks

Teaching Experience

Teaching Assistant

Madison, WI

Introduction to Computer Architecture (ECE/CS552)

Aug 2019 - Dec 2019

- Taught in a few lectures and helped students with in-class exercises
- Held discussions and office hours for questions related to course material and student projects that involved processor design using Verilog
- Graded in-class exercises, exams and projects

Teaching Assistant

Madison, WI

Advanced Computer Architecture 2 (ECE/CS757)

Jan 2020 - May 2020

- Graded paper reviews and exams

Work Experience

AMD Research

Remote

Co-op Engineer

June 2020 - Dec 2020

- Working in GPU test vehicle team on adding runtime support for next generation AMD architecture. Wrote microcode for some performance benchmark work of the front-end packet processing engine.

IBM Power Systems

Austin, TX

Staff Engineer/Scientist

Feb 2014 - July 2018

- Co-developed testbench environment for Memory Controller Unit, IBM Power 9
- Co-developed testbench environment for OpenCAPI-based Memory Buffer Unit for IBM Power 10. Worked across three teams to ensure timely delivery
- Worked on bringing up verification environment for maintenance/ bist as well as error correcting code logic

Calxeda

Austin, TX

Hardware Engineer

Aug 2013 - Dec 2013

- Worked on testbench development for Calxeda 64-bit ARM-based SOC chip for servers using System Verilog UVM
- Wrote scoreboard for Calxeda F2 Fabric Switch
- Wrote tests to verify IP blocks such eFuse, 40G PC

Courses

Fall, 2018 Advanced Computer Architecture 1, Intro to Programming Languages and Compilers
Spring, 2019 Advanced Computer Architecture 2, Intro to Operating Systems
Fall, 2019 Digital Engineering Laboratory, Intro to Quantum Computing (Audit)
Spring, 2020 Quantum Computing, Advanced Digital Image Processing

Skills

Software C++, C, Python, Qiskit, Git
Hardware Verilog, System Verilog, Quartus, ModelSim
Simulators Gem5, Garnet2.0, Thumbulator, CACTI