Unidad de Control

B82957

Restricciones:

- No vamos a interpretar los "branch" con código de operación 1

Repasemos las señales que mencionamos en los documentos anteriores:

Signal name	Effect when deasserted	Effect when asserted
RegDst	The register destination number for the Write register comes from the rt field (bits 20:16).	The register destination number for the Write register comes from the rd field (bits 15:11).
RegWrite	None.	The register on the Write register input is written with the value on the Write data input.
ALUSrc	The second ALU operand comes from the second register file output (Read data 2).	The second ALU operand is the sign-extended, lower 16 bits of the instruction.
PCSrc	The PC is replaced by the output of the adder that computes the value of PC + 4.	The PC is replaced by the output of the adder that computes the branch target.
MemRead	None.	Data memory contents designated by the address input are put on the Read data output.
MemWrite	None.	Data memory contents designated by the address input are replaced by the value on the Write data input.
MemtoReg	The value fed to the register Write data input comes from the ALU.	The value fed to the register Write data input comes from the data memory.

Como se aprecia en la imagen, la unidad de control maneja todas estas banderas y señales, sin embargo hay que tener en mente la restricción.

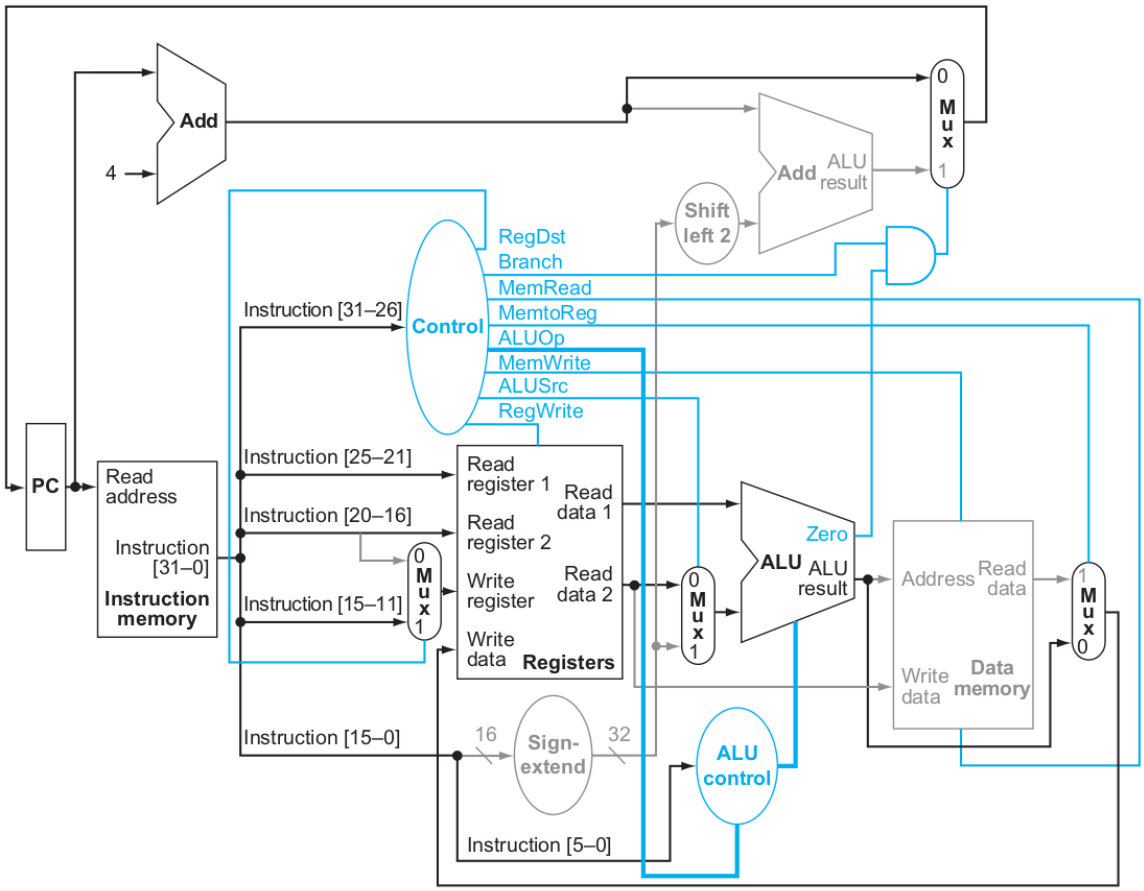

FIGURE 4.19 The datapath in operation for an R-type instruction, such as add $t1,$t2,$t3**.** The control lines, datapath units, and connections that are active are highlighted.

	EX				MEM			WB	
Instr.	**RegDst**	**ALUOp 1**	**ALUOp2**	**ALUSrc**	**Branch**	**MemRead**	**MemWrite**	**RegWrite**	**MemToReg**
R	1	1	0	0	0	0	0	1	0
lw	0	0	0	1	0	1	0	1	1
sw	X	0	0	1	0	0	1	0	X
beq	X	0	1	0	1	0	0	0	X

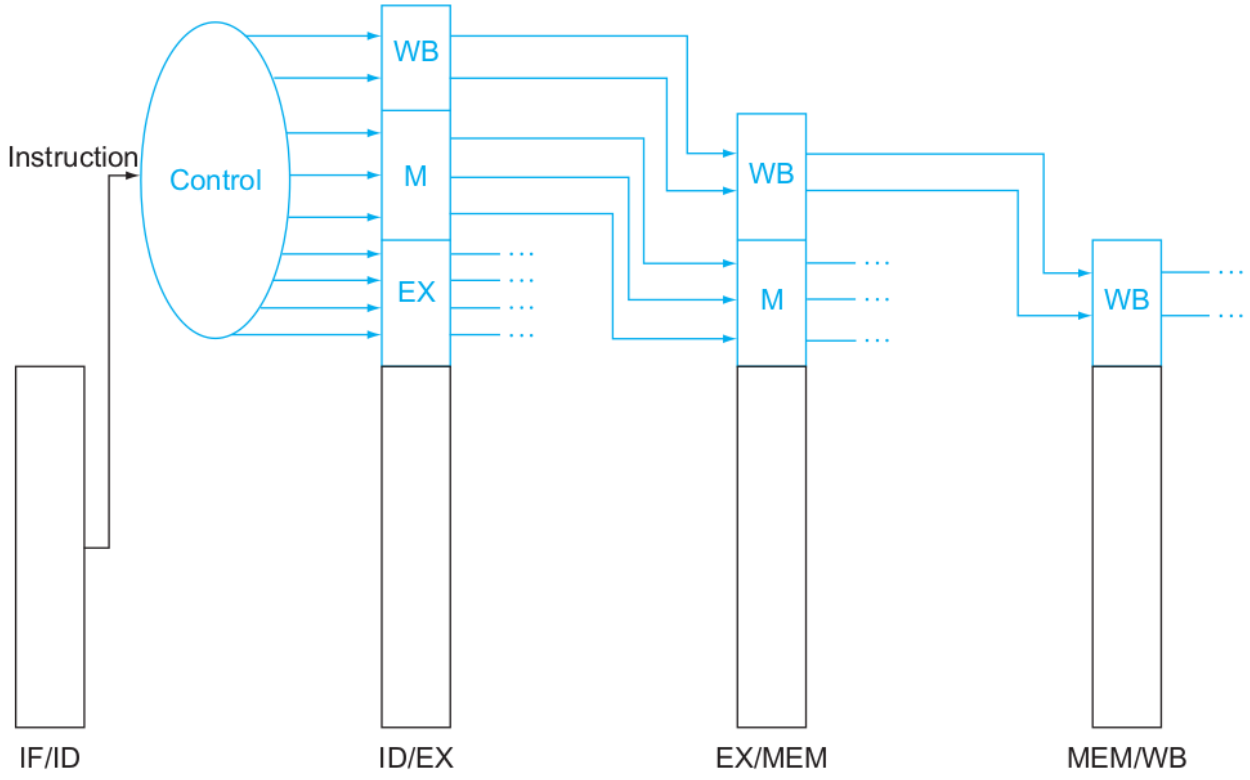

FIGURE 4.50 The control lines for the final three stages. Note that four of the nine control lines are used in the EX phase, with the remaining five control lines passed on to the EX/MEM pipeline register extended to hold the control lines; three are used during the MEM stage, and the last two are passed to MEM/WB for use in the WB stage.

Notamos que la unidad de control es simplemente, un manejador de banderas. La idea de como implementar esto es mediante un **splitter**. Obtemenos la instrucción y separamos los datos, mandando 1 bit, correspondiente al valor de la flag, a cada stage necesario

Referencias:

Computer Organization and Design: the Hardware/Software