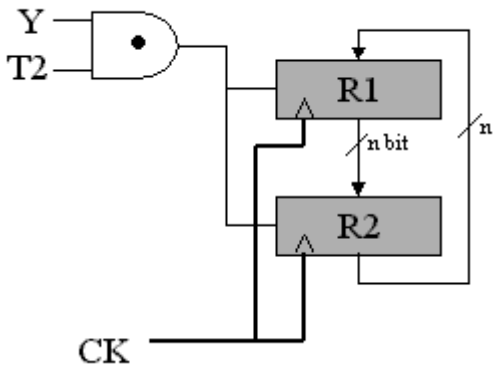
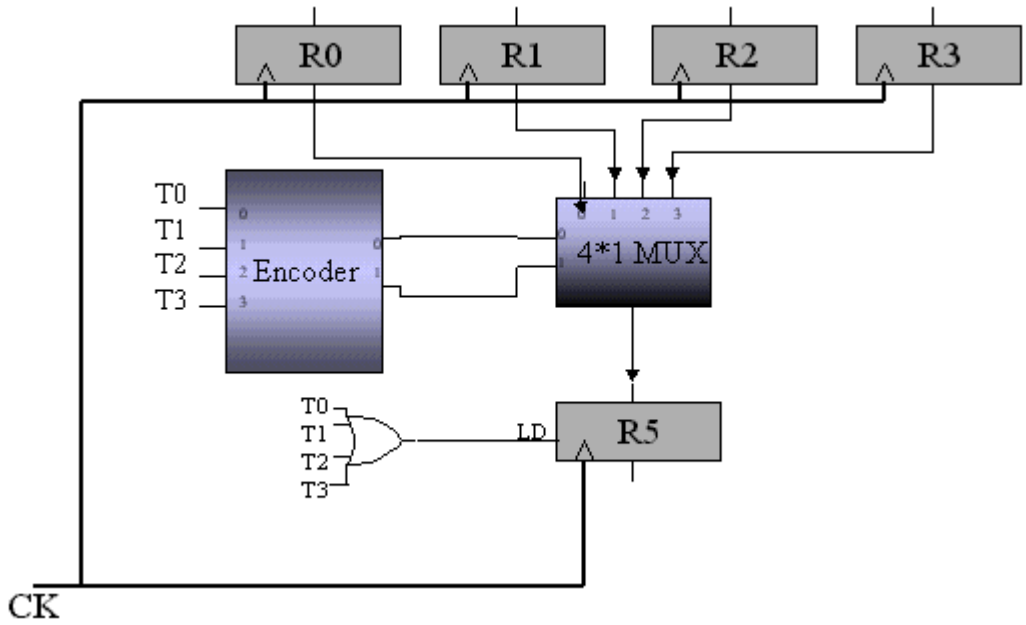
Question 4-1:



This RTL statement can happen provided that registers are of edge triggered type.[1]

Question 4-2:



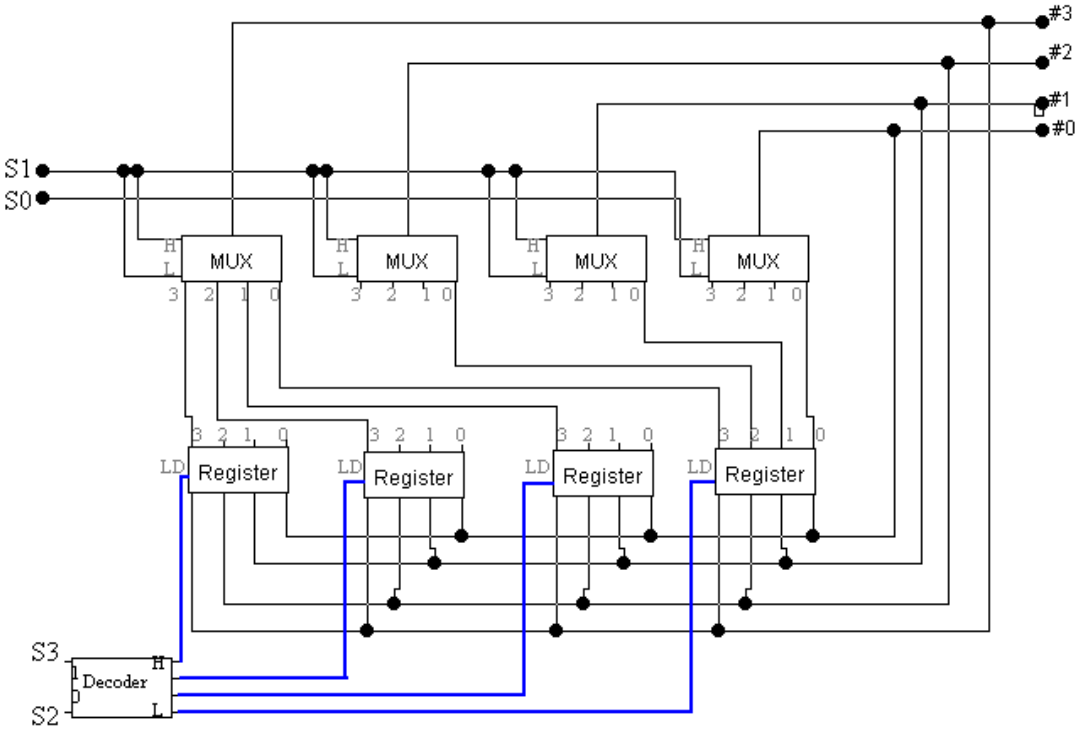
Question 4-3:

`P:  R1 ← R2`

`P'Q:  R1 ← R3`

[1] "Computer System Architecture" M. Morris Mano, page 97

Question 4-4:
In this question we use S1 S0 to select the source register (With S1 being HSB), and use S3 S2 to select among the four registers available (with S3 being the HSB).



Question 4-5:

a) IR ← M[PC]
We can't use the PC as an address to Memory, because Memory takes its address from AR Register.
We can write it as:
AR ← PC
IR ← M[AR]

b) AC ← AC + TR
There is no such access to AC except for INPR, DR and itself, so the correct form would be:
DR ← TR
AC ← AC + DR

c) DR ← DR + AC (AC doesn't change):
This would change the value of AC to AC + DR. Also the Adder and Logic Unit should save its result in AC not in DR. The correct form would be:
TR ← AC
AC ← AC + DR
DR ← AC
AC ← TR

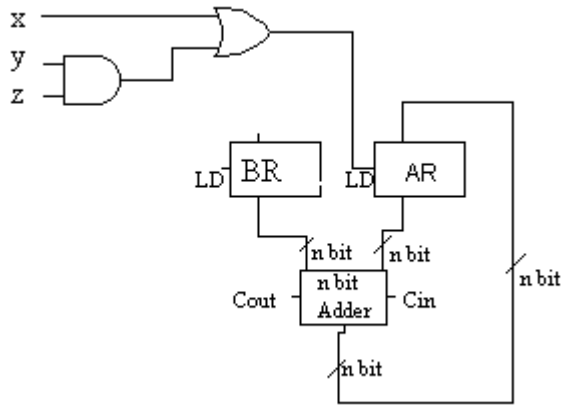
Question 4-6:

a) 4 Selection Lines.
b) 16x1 MUX's
c) 32 MUX

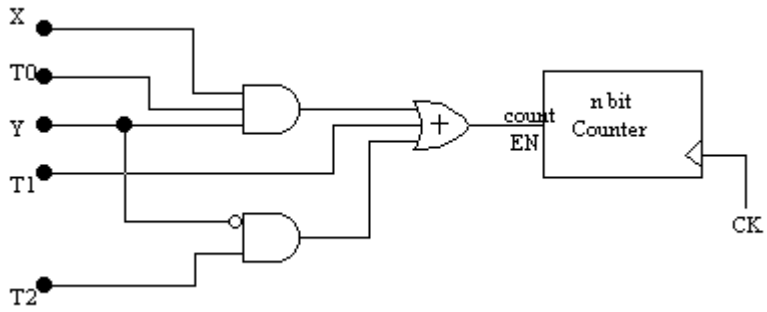
Question 4-7:

a) R2 ← M[AR]
This statement would transfer the contents of Memory word that has the address specified by AR into R2 register.
b) M[AR] ← R3:
WRITE the value in register R3 into the Memory Word that has the address specified in AR.
d) R5← M[R5]:
It will firstly READ the Memory Word specified by R5 and then transfer the value into the same register R5, this is mostly used in Indirect Addressing.

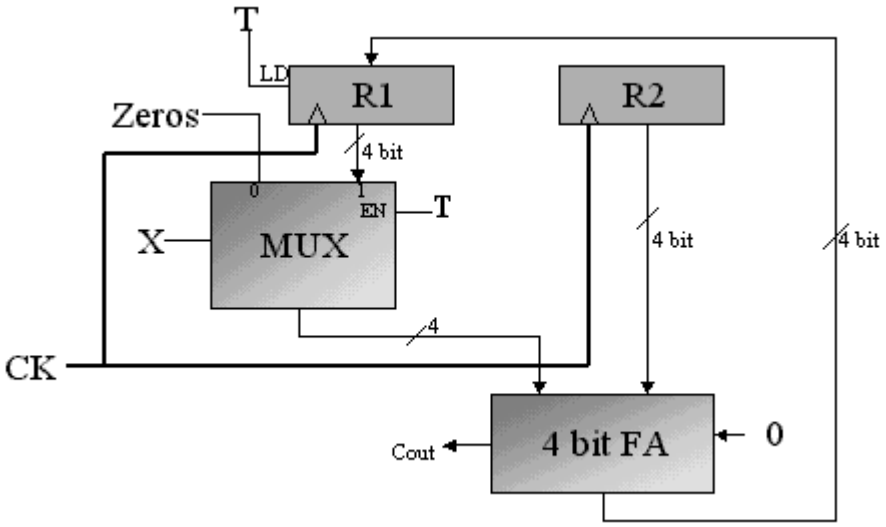
Question 4-8:



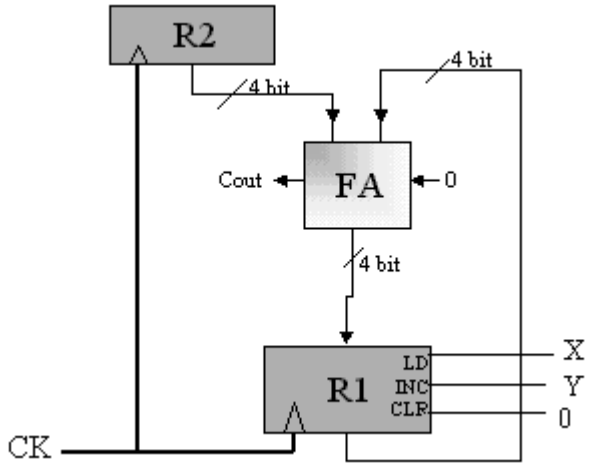
Question 4-9:



Question 4-10:



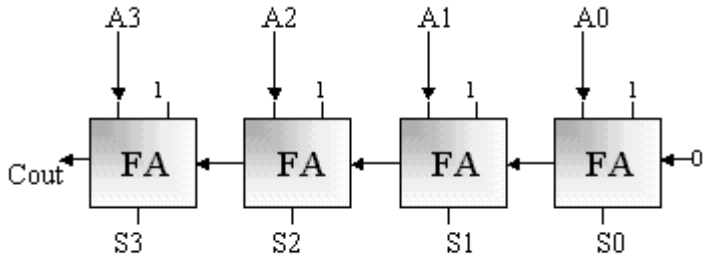
Question 4-11:



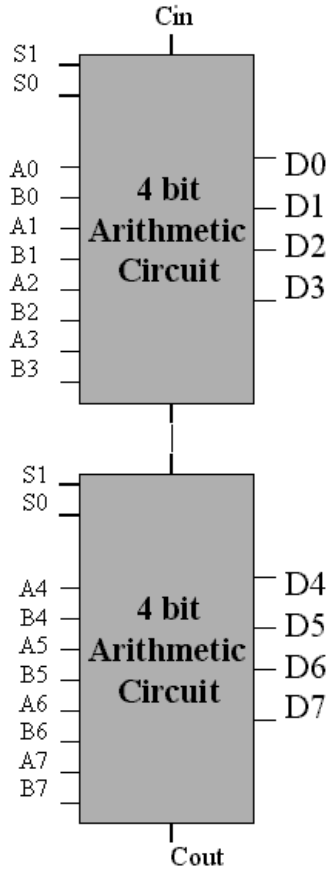
Question 4-12:

	S3	S2	S1	S0	C4	
A	1	1	0	1	0	7+6
B	0	0	0	1	1	8+9
C	0	1	0	0	1	12-8
D	1	0	1	1	0	5-10
E	1	1	1	1	0	-1

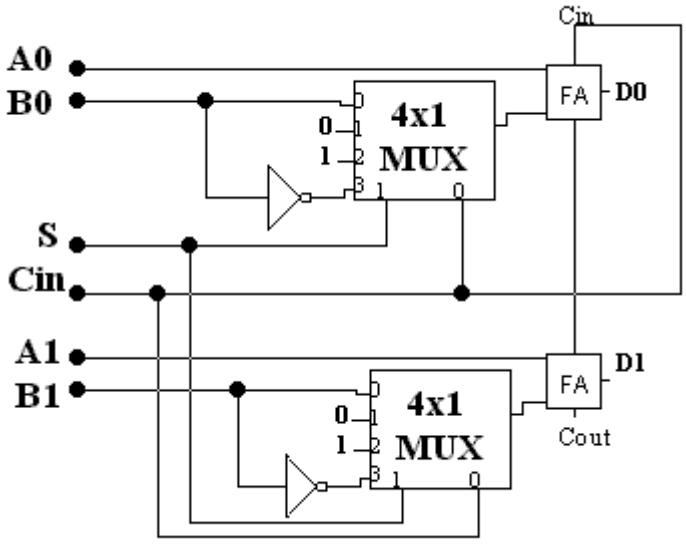
Question 4-13:



Question 4-14:



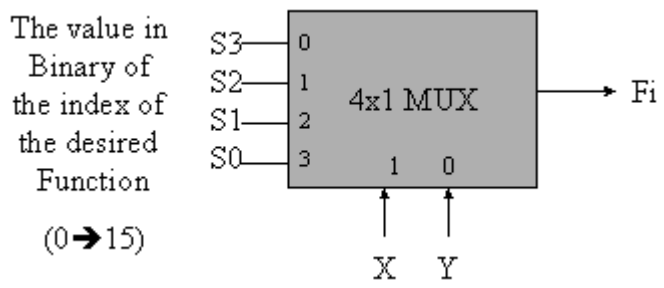
Question 4-15:



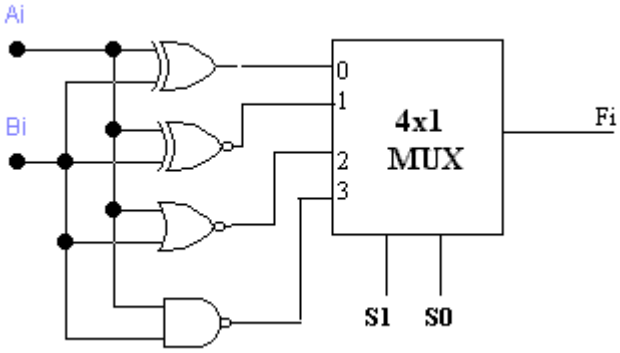
Question 4-16:

Building a combinational circuit capable of selecting and generating any of the 16 logic functions in table 4-5?

	F_i	$S_3\ S_2\ S_1\ S_0$
0	$F_0 = 0$	0000
1	$F_1 = xy$	0001
2	$F_2 = xy'$	0010
3	$F_3 = x$	0011
4	$F_4 = x'y$	0100
5	$F_5 = y$	0101
6	$F_6 = x$ XOR y	0110
7	$F_7 = x + y$	0111
8	$F_8 = (x + y)'$	1000
9	$F_9 = (x$ XOR $y)'$	1001
10	$F_{10} = y'$	1010
11	$F_{11} = x + y'$	1011
12	$F_{12} = x'$	1100
13	$F_{13} = x' + y$	1101
14	$F_{14} = (xy)'$	1110
15	$F_{15} = 1$	1111



Question 4-17:



Question 4-18:

A= 1101 1001 (Note: A^+ means the new value of Register A)

a) A^+ = 0110 1101 ➔ B=1011 0100 And the Logic Operation is **XOR**
b) A^+ = 1111 1101 ➔ B= 1111 1101, And the Logic Operation is **OR**

Question 4-19:

Initially:

AR = 11110010, BR=11111111, CR=10111001, DR=11101010

Determine the values of these registers after the execution of the following micro operations:

Micro operation	**AR**	**BR**	**CR**	**DR**
Initially	1111 0010	1111 1111	1011 1001	1110 1010
AR ← AR + BR	1111 0001	1111 1111	1011 1001	1110 1010
CR← CR AND DR, BR←BR+1	1111 0001	0000 0000	1010 1000	1110 1010
AR←AR – CR	0100 1001	0000 0000	1010 1000	1110 1010

Question 4-20:
Initially R = 1001 1100, which is –100 in Decimal.

Microoperation	R	Decimal value of R	Overflow
R ← ashr R	1100 1110	-50	No
R ← ashl R	0011 1000	+56	Yes

Question 4-21

Microoperation	R
Initially	1101 1101
R ← shl R	1011 1010
R ← cir R	0101 1101
R ← shr R	0010 1110
R ← cil R	0101 1100

Question 4-22:
What's the output H in Fig 4-12 if A is 1001, S=1, $I_R = 1$ and $I_L = 0$?
The value of H would be : $A_1\ A_2\ A_3\ I_L = 0010$

Question 4-23:
What is wrong in the following?

a. xT: AR ← (AR)', AR ← 0
   The two microoperations -Compliment and Clear - are supposed to be done @ the same time on the same register, this is wrong coz these microoperations can't be implemented on the same register @ the same time.
b. yT: R1 ← R2, R1← R3
   These microoperations make no sense; coz two values are to be loaded into the same register at the same time.
c. zT: PC ← AR, PC ← PC + 1

This statement is ambiguous; it doesn't determine what to be loaded into PC, the value of AR or incrementing PC, these are two conflicting microoperations that can't be implemented on the same register at the same time.