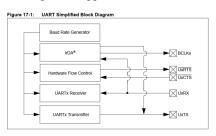
Embedded Systems 3.5 - UART (Clicker 2)

Enrico Simetti

ISME - Interuniversity Research Center on Integrated Systems for Marine Environment DIBRIS - Department of Computer Science, Bioengineering, Robotics and System Engineering University of Genova, Italy enrico.simetti@unige.it

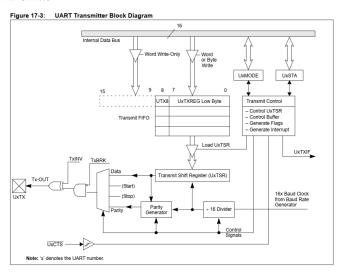
dsPIC33F UART I

- Full-duplex 8- or 9-bit data transmission
- Even, Odd or No Parity options (for 8-bit data)
- One or two Stop bits
- Fully integrated Baud Rate Generator with 16-bit prescaler
- ▶ Baud rates ranging from 38 bps to 10 Mbps at FCY = 40 MHz
- ▶ 4-deep First-In-First-Out (FIFO) transmit data buffer
- ▶ 4-deep FIFO receive data buffer
- Parity, Framing and Buffer Overrun error detection
- ► Support for 9-bit mode with Address Detect (9th bit = 1)
- ► Transmit and Receive Interrupts
- Loopback mode for diagnostic support



dsPIC33F UART II

UART Transmitter



dsPIC33F UART III

UART Receiver

Figure 17-10: UART Receiver Block Diagram Internal Data Bus Word or Word Read-Only Byte Read UxMODE UxSTA 15 URX8 UxRXREG Low Byte Receive Buffer Control - Generate Flags - Generate Interrupt - Shift Data Characters Load UxRSR to Buffer UxRXIF LPBACK From UxTX Control PERR Signals Receive Shift Register (UxRSR) Start bit Detect Parity Check Stop bit Detect + 16 Divider Shift Clock Generation Wake Logic 16x Baud Clock UEN1 UEN0 from Baud Rate Generator **BCLKx** BCLKx/UxRTS UEN UxRTS Selection UxCTS **UxCTS** Note: 'x' denotes the UART number.

UART related registers I

REGISTER 20-2: UxSTA: UARTx STATUS AND CONTROL REGISTER

R/W-0	R/W-0	R/W-0	U-0	R/W-0, HC	R/W-0	R-0	R-1			
UTXISEL1	UTXINV	UTXISEL0	_	UTXBRK	UTXBRK UTXEN ⁽¹⁾		TRMT			
bit 15	bit 15									
R/W-0	/-0 R/W-0 R/W-0		R-1	R-0	R-0	R/C-0	R-0			
URXISE	L<1:0>	ADDEN	RIDLE	PERR	FERR	OERR	URXDA			
bit 7							bit 0			

UxSTA: UART Status registers, contains the flags that notify the program of certain events.

- ▶ *UTXISEL*: selects when the IF is set to 1 during transmission
- ► *URXISEL*: selects when the IF is set to 1 during reception
- ► *UTXEN*: enables transmission
- ► *TRMT*: notifies if there is an on-going transmission
- ► *URXDA*: notifies if there are characters to be read
- **OERR**: notifies if an overflow error occurred

UART related registers II

After an overflow occurred, and UxSTAbits.OERR = 1, the peripheral will discard any incoming bytes, until the user resets UxSTAbits.OERR = 0;

We have the following choices when an overflow occurred:

- read all the bytes in the UART buffer, then clear OERR;
- clear OERR immediately (the bytes are lost);

UART related registers III

- bit 15 UTXISEL: Transmission Interrupt Mode Selection bit
 - 1 = Interrupt when a character is transferred to the Transmit Shift register and as result, the transmit buffer becomes empty
 - 0 = Interrupt when a character is transferred to the Transmit Shift register (this implies that there is at least one character open in the transmit buffer)
- bit 7-6 URXISEL<1:0>: Receive Interrupt Mode Selection bit
 - 11 = Interrupt flag bit is set when Receive Buffer is full (i.e., has 4 data characters)
 - 10 =Interrupt flag bit is set when Receive Buffer is 3/4 full (i.e., has 3 data characters)
 - 0x =Interrupt flag bit is set when a character is received

Changing these bits influences when UxTXIF and UxRXIF go to 1, i.e. about which kind of event the peripheral will alert us UTXISEL and URXISEL do not enable the interrupts!

Check IEC0 register to enable the interrupts.

UART related registers IV

Register 17-1: UxMODE: UARTx Mode Register

R/W-0	U-0	R/W-0	R/W-0	R/W-0 R/W-0		R/W-0	R/W-0	
UARTEN	_	USIDL	IREN ⁽¹⁾	RTSMD	_	UEN<1:0>		
bit 15							bit 8	

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSEL	<1:0>	STSEL
bit 7							bit 0

UxMODE: UARTx Mode register.

- ► *UARTEN*: enables the UART module
- ▶ *PDSEL*: selects the parity and data bits

UART related registers **V**

UxRXREG: contains the character received*UxTXREG*: write here the character to be sent to the transmit buffer*UxBRG*: the baud rate register

$$Baud Rate = \frac{FCY}{16 \cdot (UxBRG + 1)}$$

$$UxBRG = \frac{FCY}{16 \cdot Baud Rate} - 1$$

Note: Fcy denotes the instruction cycle clock frequency.

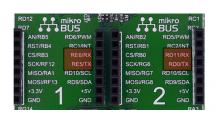
Example UART programming

Example: sending one character at 9600 with UART1, assuming 7.3728 MHz oscillator (Fcy = 1.8432 MHz)

```
U1BRG = 11; // (7372800 / 4) / (16 * 9600) - 1
U1MODEbits.UARTEN = 1; // enable UART
U1STAbits.UTXEN = 1; // enable U1TX (must be after UARTEN)
U1TXREG = 'C'; // send 'C'
```

Clicker 2 Board UART I

You must use the MikroBUS UART add-on board, inserted on one of the two on-board sockets:





Here we need to remap Both input (RX) and output (TX)

Clicker 2 Board UART II

Example: UART pins remap on MikroBUS 1

RP127/RG15	1	
AN29/PWM3H/PMD5/RP85/RE5	3	
AN30/PWM4L/PMD6/RPI86/RE6 AN31/PWM4H/PMD7/RP87/RE7	4	
	5	
AN16/PWM5L/RPI49/RC1 AN17/PWM5H/RPI50/RC2	6	
	•	
AN18/PWM6L/RPI51/RC3	8	
AN19/PWM6H/RPI52/RC4	9	
C1IN3-/SCK2/PMA5/RP118/RG6	10	
C1IN1-/SDI2/PMA4/RPI119/RG7	11	
C2IN3-/SDO2/PMA3/RP12 <u>0/RG8</u>	12	dsPIC33EP512MU810
MCLR	13	
C2IN1-/PMA2/RPI121/RG9	14	dsPIC33EP256MU810
Vss _	15	
VDD	16	
TMS/RPI16/RA0	17	
AN20/RPI88/RE8	18	
AN21/RPI89/RE9	19	
_	20	
	21	
AN3/C2IN1+/VPIO/RPI35/RB3	22	
AN2/C2IN2-/VMIO/RPI34/RB2	23	
PGEC3/AN1/RPI33/RB1	24	
PGED3/AN0/RPI32/RB0	25	

Input pin can be remapped as shown in the Interrupts section

Clicker 2 Board UART III

Output pin remap with PPS:

input: reg that corresonds to functionality and select pin outpu: select pin and then what output goes in that pin

TABLE 11-3: OUTPUT SELECTION FOR REMAPPABLE PINS (RPn)

Function	RPnR<5:0>	Output Name
DEFAULT PORT	000000	RPn tied to Default Pin
U1TX	000001	RPn tied to UART1 Transmit
U1RTS	000010	RPn tied to UART1 Ready-to-Send
U2TX	000011	RPn tied to UART2 Transmit
U2RTS	000100	RPn tied to UART2 Ready-to-Send
SDO1	000101	RPn tied to SPI1 Data Output
SCK1	000110	RPn tied to SPI1 Clock Output
SS1	000111	RPn tied to SPI1 Slave Select
SS2	001010	RPn tied to SPI2 Slave Select
CSDO	001011	RPn tied to DCl Data Output
CSCK	001100	RPn tied to DCI Clock Output
COFS	001101	RPn tied to DCI FSYNC Output
C1TX	001110	RPn tied to CAN1 Transmit
C2TX	001111	RPn tied to CAN2 Transmit
OC1	010000	RPn tied to Output Compare 1 Output
OC2	010001	RPn tied to Output Compare 2 Output
OC3	010010	RPn tied to Output Compare 3 Output
OC4	010011	RPn tied to Output Compare 4 Output
OC5	010100	RPn tied to Output Compare 5 Output
OC6	010101	RPn tied to Output Compare 6 Output
OC7	010110	RPn tied to Output Compare 7 Output
OC8	010111	RPn tied to Output Compare 8 Output
C10UT	011000	RPn tied to Comparator Output 1
C2OUT	011001	RPn tied to Comparator Output 2
C3OUT	011010	RPn tied to Comparator Output 3
U3TX	011011	RPn tied to UART3 Transmit
U3RTS	011100	RPn tied to UART3 Ready-to-Send

Note 1: This function is available in dsPIC33EPXXX(MC/MU)806/810/814 devices only.

Example UART remapping on MikroBUS 2

!!!!!!!!remap input and output of peripherals!!!!!!!!!

PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EPXXXMU810/814 AND PIC24EPXXXGU810/814 DEVICES ONLY

Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
0680	-	_	RP65R<5:0>						_	-	RP64R<5:0>						
0682	-	_	RP67R<5:0>						_	_	RP66R<5:0>						
0684	_	_		RP69R<5:0>						_	RP68R<5:0>						
0686	-	_		RP71R<5:0>						-	RP70R<5:0>						
0688	_	_		RP80R<5:0>						_	RP79R<5:0>						
068A	_	_		RP84R<5:0>						_	RP82R<5:0>						
068C	_	_	RP87R<5:0>						_	_	RP85R<5:0>						0000
068E	-	_	RP97R<5:0>						_	-	RP96R<5:0>						0000
0690	-	_		RP99R<5:0>						_	RP98R<5:0>						0000
0692	_	_		RP101R<5:0>						_	RP100R<5:0>						0000
0696	-	_			RP108	R<5:0>			_	_	RP104R<5:0>						0000
0698	-	_		RP112R<5:0>						-	RP109R<5:0>						0000
069A	_	_		RP118R<5:0>						_	RP113R<5:0>						0000
069C	_	_	RP125R<5:0>						_	_	RP120R<5:0>						0000
069E	-	_		RP127R<5:0>						_			RP126	R<5:0>			0000
	0680 0682 0684 0686 0688 068A 068C 069C 0692 0696 0698 069A 069C	0680 — 0682 — 0684 — 0686 — 0688 — 0688 — 0688 — 0688 — 0690 — 0690 — 0692 — 0696 — 0698 — 0698 —	0680	0080 0082 0082 0088 0086 0086 0086 0086 0086 0086 0096 0099 0099 0099 0099 0099 0099 0099 0099 0090 0090	0080 0082 0082 0088 0088 0086 0080 0090 0090 0090 0090 0090 0090 0090 0090 0090 0090 0090 0090 0090 0090 0090 0090	PROSE PROS		D080	PROSIN-S-D		NPGRR-5 0	PROSENCE PROSENCE	PROSE-6-0-	NPGRR-5 D	Page Page	PROSESS PRO	NPGRK-5D

Pins here are RD0/RP64 and RD11/RPI75

```
RPORObits.RP64R = 0x01; // Map UART 1 TX to pin RD0 which is
RP64
RPINR18bits.U1RXR = 0x4B; // Map UART 1 RX to pin RD11 which
is RPI75 (0x4B = 75) i put the pin that i need to use
```