Measurements Burridge-Knopoff oscillators

Bitto Manuel

June 5, 2024

1 Single block measurements

1.1 Breadboard implementation

The inductorless electronic analog of the Burridge-Knopoff model [1] is represented in Fig. 1. This circuit was implemented in a breadboard using 1N5817 Schottky diodes and different kinds of op-amps, namely UA741, OP07, TL081 and OP27; these op-amps were supplied with $V_{CC} = \pm 12$ V. The nominal values for the resistances and capacitors are $R = R_c = 10$ kΩ, $R_A = R_B = 10$ kΩ, $r = 1.8$ kΩ and $C = 100$ nF. The input voltages are $V_0 = 1$ V and the variable voltage V_d, while the output voltages are V and W (the subscript i is omitted).

The oscillating behavior of this circuit is shown in Fig. 2. The lower clamping in the Lissajous figure is intended and is due to the presence of the Schottky diodes. The frequency behavior at high voltages, namely $V_d \gtrsim 1$ V, is the same for each kind of op-amp. On the other hand, the amplitudes possess an offset which depends on the selected op-amp; nonetheless, they all exhibit a mostly linear behavior.

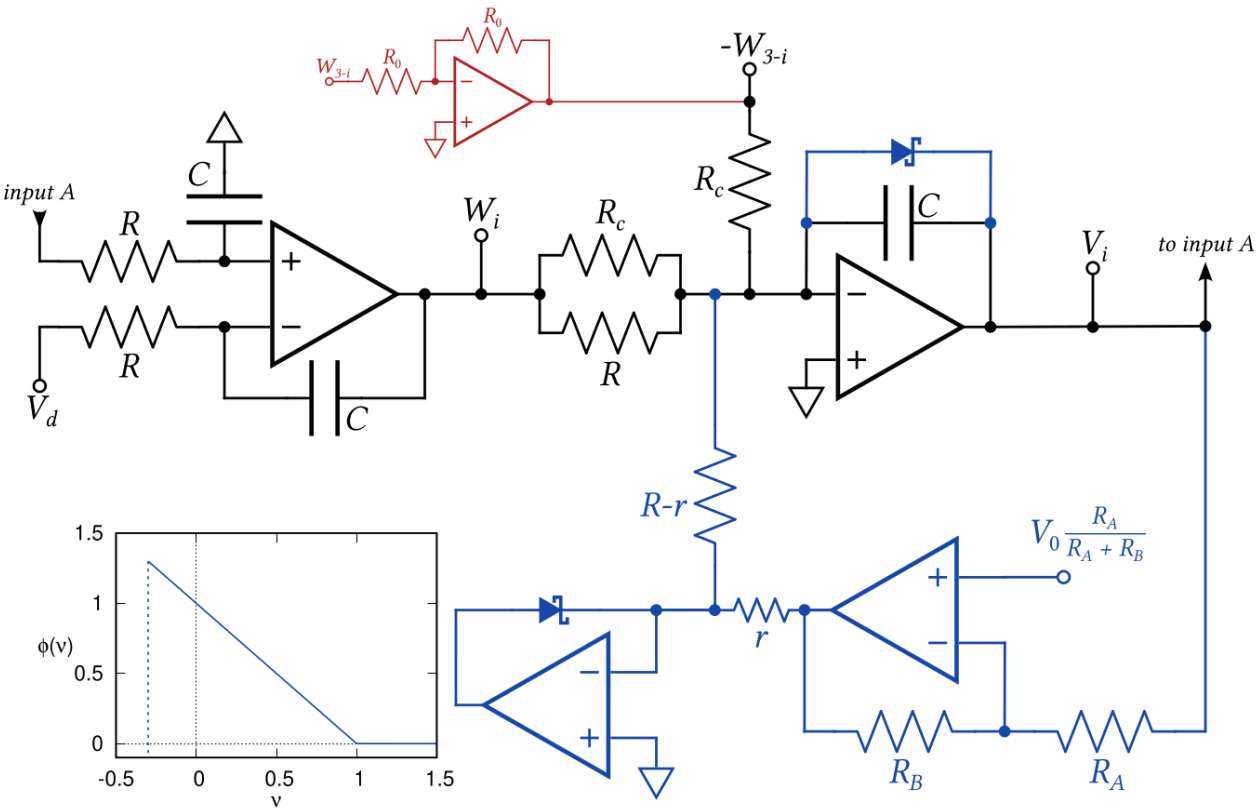

Figure 1: Inductorless representation of the BK model. The blue part of the network refers to the nonlinear element, whose characteristic is drawn in the bottom left plot. Figure adapted from Ref. [1].

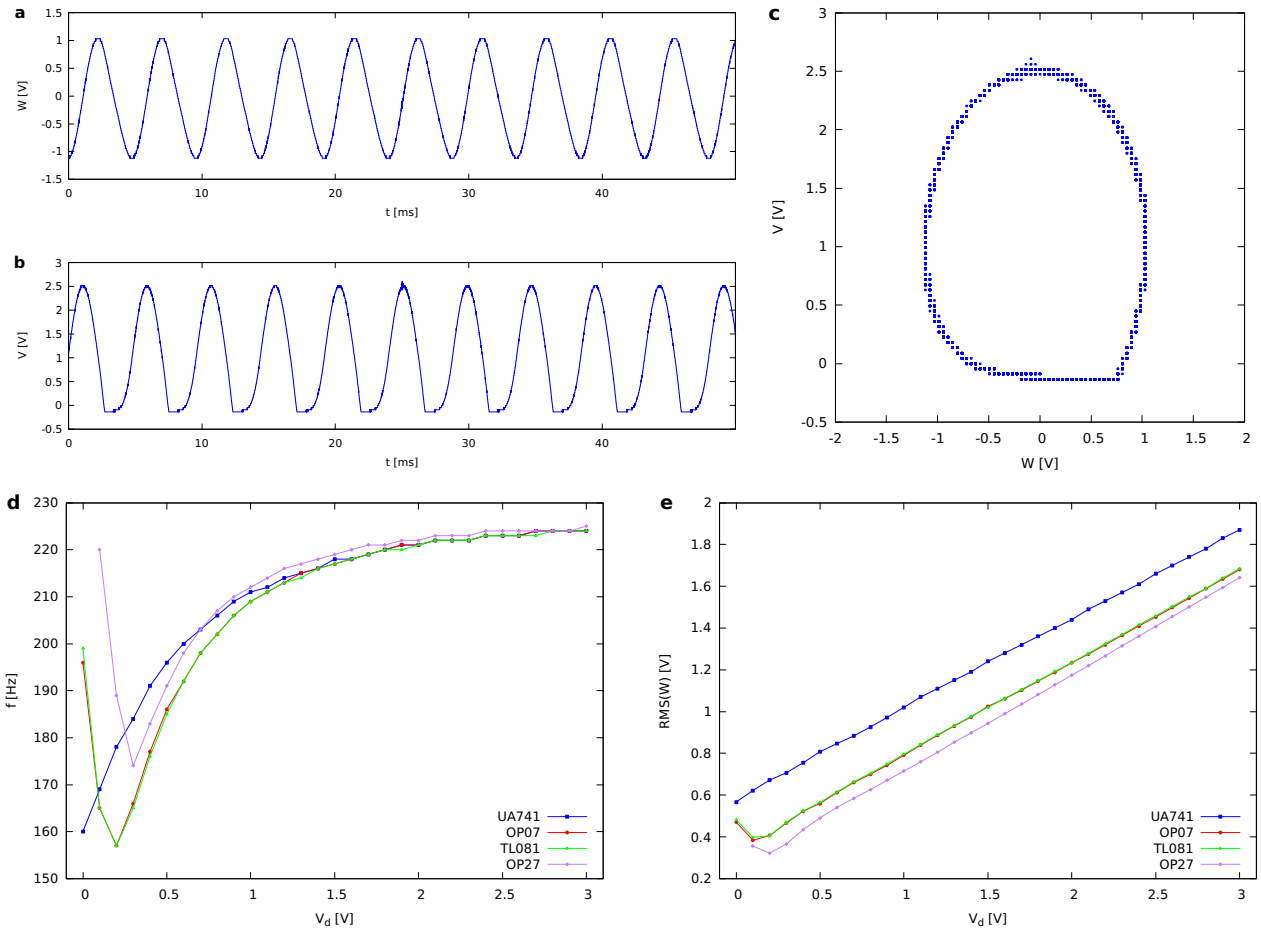

Figure 2: Oscillating behavior for the circuit implemented on the breadboard. (a) Plot of W and (b) of V as a function of time, for $V_d = 1$ V. (c) Phase portrait (Lissajous figure) of V versus W. (d) Frequency and (e) root mean square amplitude of the output signal W as a function of the parameter V_d and for different kinds of op-amps.

1.2 Prototypes

In order to describe the coupling between many oscillators it is not possible use the breadboard implementation of the circuit shown in Fig. 1, due to scalability issues. For the purpose of improving the system scalability, two smaller prototypical chips have been built. The circuit implemented in each chip is shown in Fig. 3. The differences between this circuit and the one used in the previous subsection lie in the nonlinear elements; in this case MBRA210L Schottky diodes have been used, as well as quad operational amplifiers OP470, which offer comparable performance to OP27 op-amps.

The oscillating behavior of this circuit is shown in Fig. 4 for both chips. These systems are much less stable with respect to the circuit implemented on the breadboard; in fact, measurements were possible only in a small range for V_d, namely $V_d \leq 1.1$ V for one chip and $V_d \leq 0.6$ V for the other one. It is also important to point out that the diode clamping is not present; in fact, it is only noticeable at voltages $V_d \lesssim 0.4$ V.

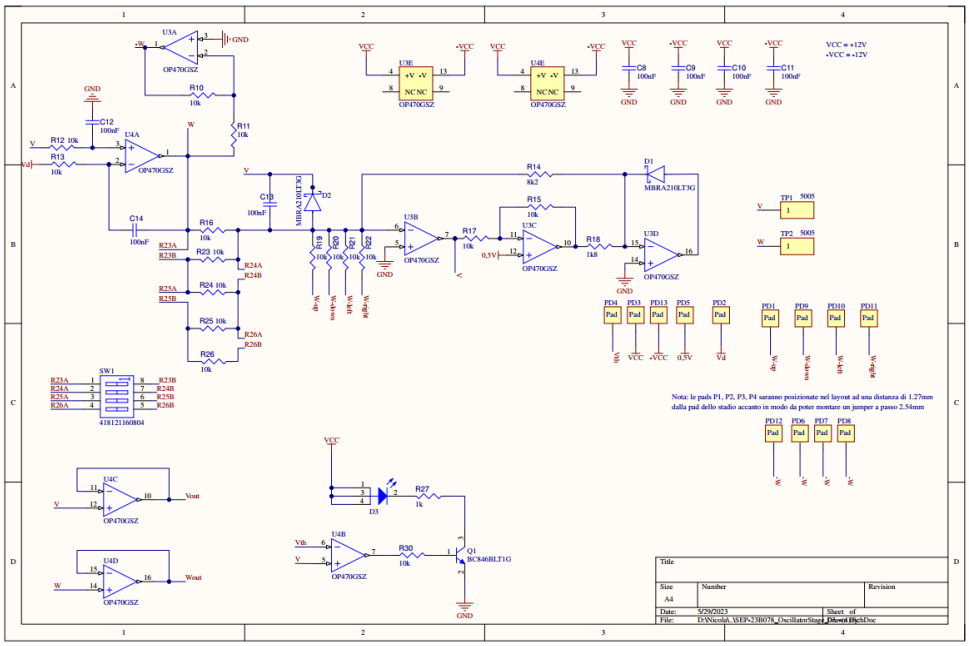

Figure 3: Circuit diagram of one prototypical chip.

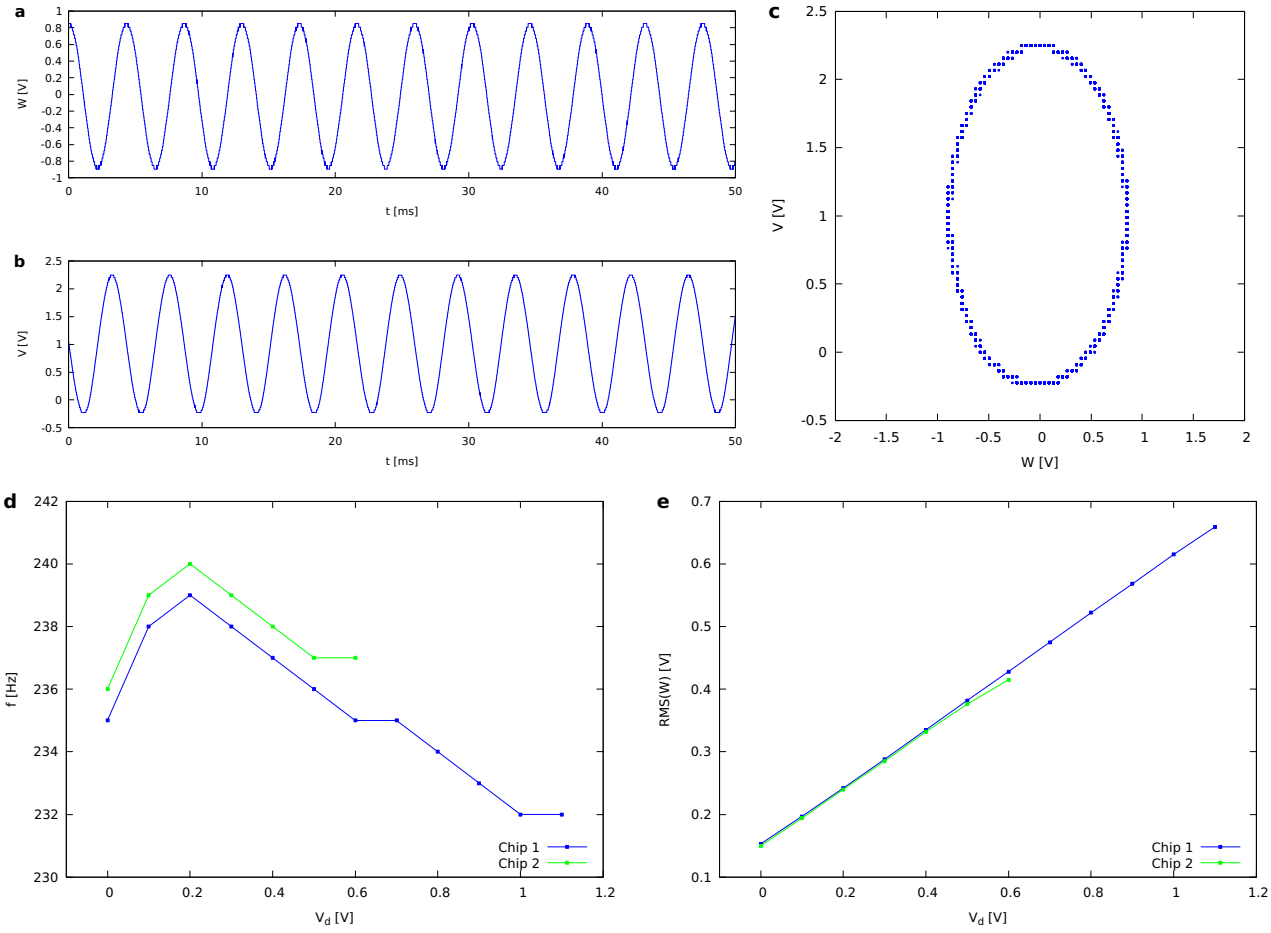

Figure 4: Oscillating behavior for the circuit implemented on the prototypical chips. (a) Plot of W and (b) of V as a function of time, for $V_d = 1$ V. (c) Phase portrait (Lissajous figure) of V versus W. (d) Frequency and (e) root mean square amplitude of the output signal W as a function of the parameter V_d and for the two different chips.

1.3 Board

In order to finally analyze the behavior of many coupled oscillators, a board containing 25 chips (or blocks) has been built. The circuit diagram is equivalent to the one shown in Fig. 3 for the prototypes, the only difference being the use of DFLS1100 Schottky diodes instead of MBRA210L ones.

The oscillating behavior is shown in Fig. 5. Once again, these systems are not as stable as the circuit on the breadboard; measurements were in fact taken for $V_d \leq 2.2$ V for the first two blocks. It is important to notice that in the voltage range 0.6 V $\leq V_d \leq 2.1$ V a clamping of the output voltage V can be observed; this is not intended and is probably due to intrinsic limitations in the current.

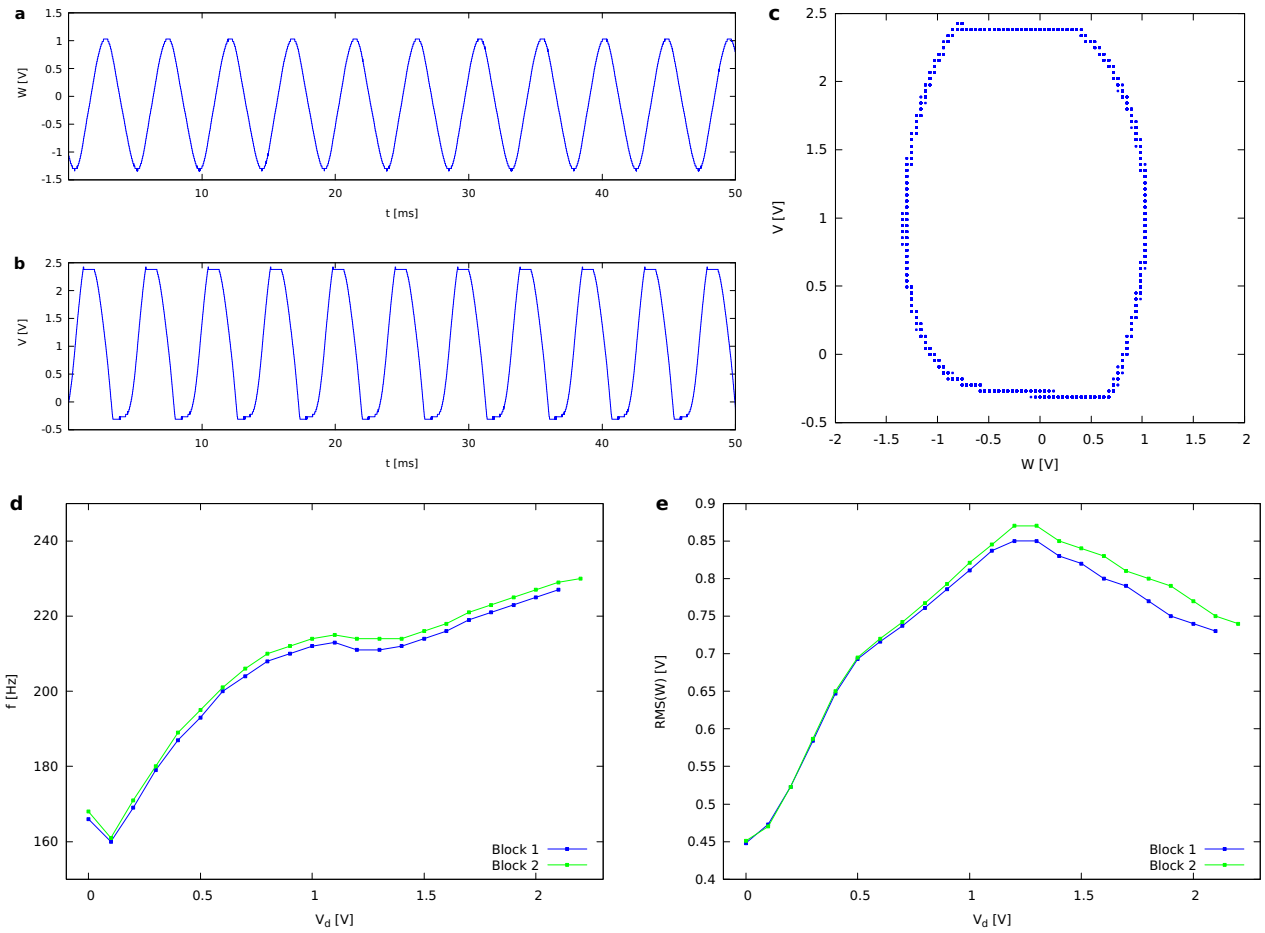

Figure 5: Oscillating behavior for the circuit implemented on the board. (a) Plot of W and (b) of V as a function of time, for $V_d = 1$ V. (c) Phase portrait (Lissajous figure) of V versus W. (d) Frequency and (e) root mean square amplitude of the output signal W as a function of the parameter V_d and for two different blocks.

1.4 New board

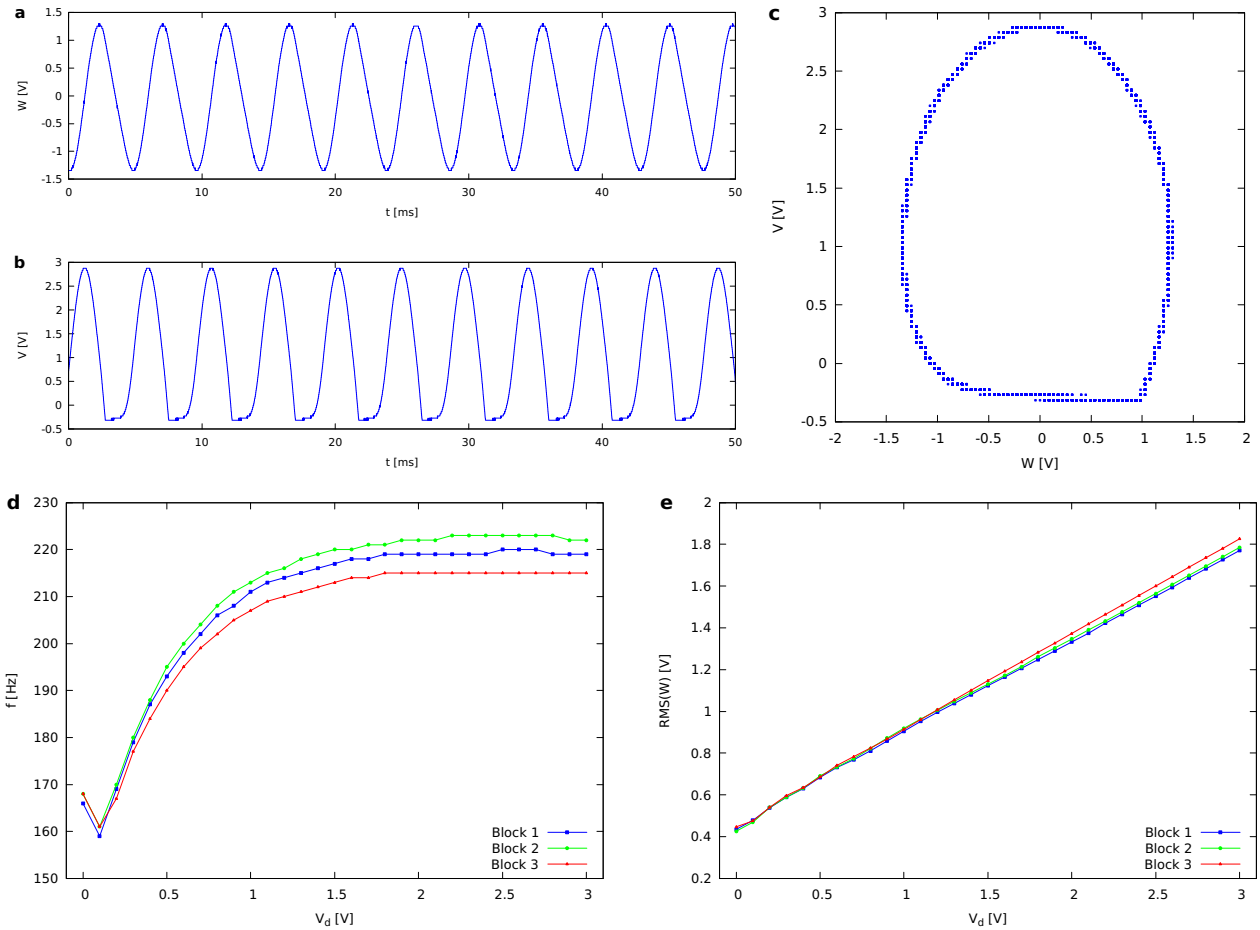

Figure 6: Oscillating behavior for the circuit implemented on the new board. (a) Plot of W and (b) of V as a function of time, for $V_d = 1$ V. (c) Phase portrait (Lissajous figure) of V versus W. (d) Frequency and (e) root mean square amplitude of the output signal W as a function of the parameter V_d and for three different blocks.

1.5 Conclusions

The comparison between frequency and amplitude on the three implementations is shown in Fig. 7. The frequency of the board is very similar to the breadboard one for voltages $V_d < 1$ V; at higher voltages there are small deviations in the board, probably due to the increased relevance of the current clamping. This might also be the reason why the amplitude behavior of the board is not linear.

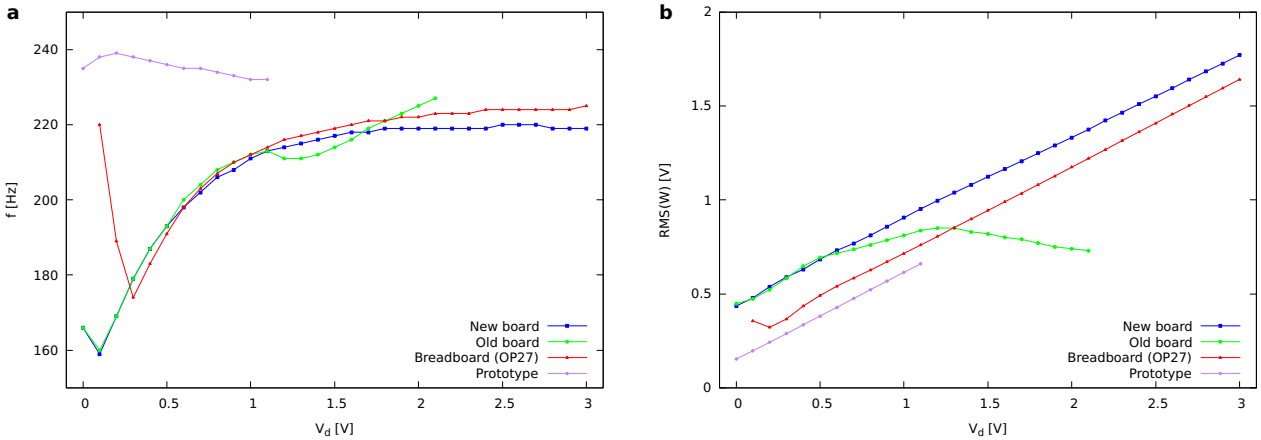

Figure 7: (a) Frequency and (b) root mean square amplitude of the output signal W as a function of the parameter V_d for the three implementations of the BK model, i.e. the first block of the board, the breadboard implementation with the OP27 op-amps and the first prototypical chip.

2 Multi block measurements

2.1 Two blocks

The coupling between two oscillators is performed by connecting the inverted voltage $-W_2$ of the second oscillator to the first one and viceversa, as shown in Fig. 1. A chaotic behavior can be observed, as can be seen in Fig. 8.

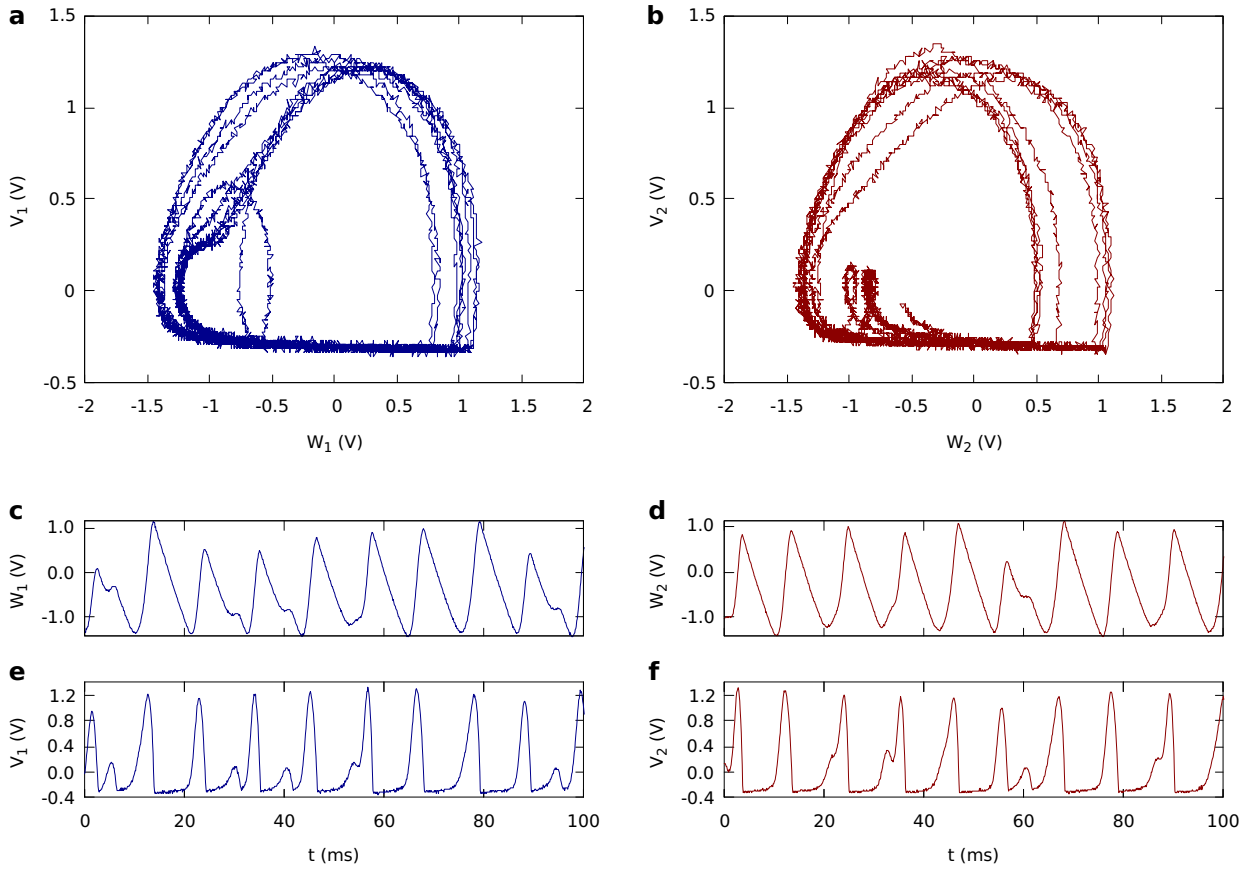

Figure 8: Chaotic behavior of two coupled blocks for $V_d = 0.05$ V and for a total time of 100 ms. Phase portraits of V_i vs W_i for the first (a) and second (b) block. Time series plots for W_1 (c), V_1 (e), W_2 (d) and V_2 (f).

In order to quantify the degree of chaos of this system, it is possible to carry out an analysis

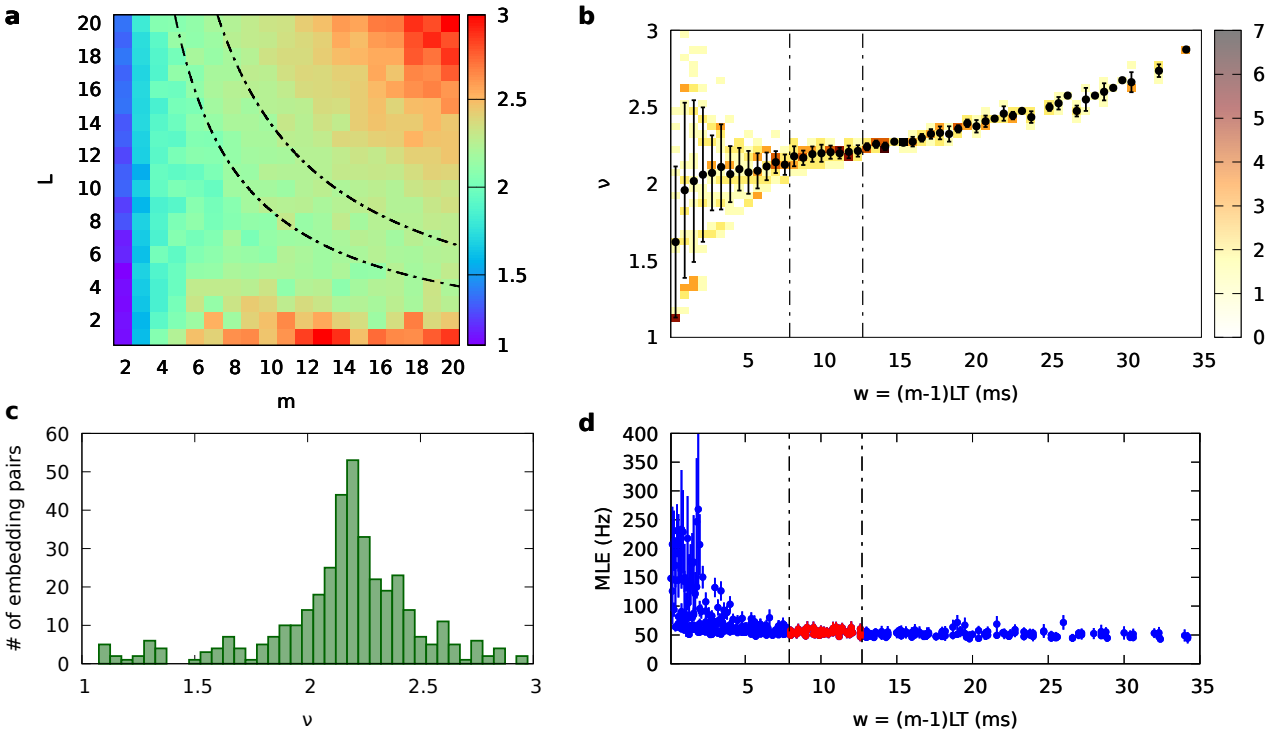

Figure 9: ciao

2.2 Three blocks

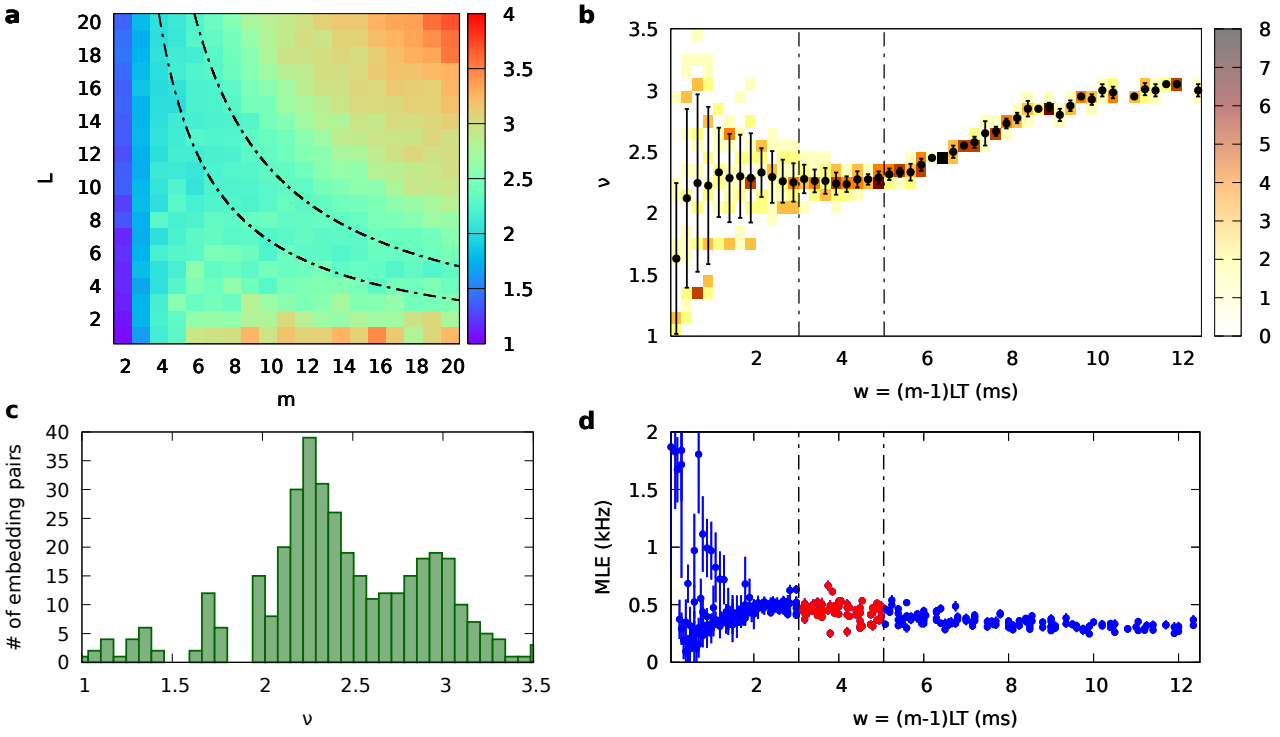

Figure 10: ciao

2.3 Four blocks

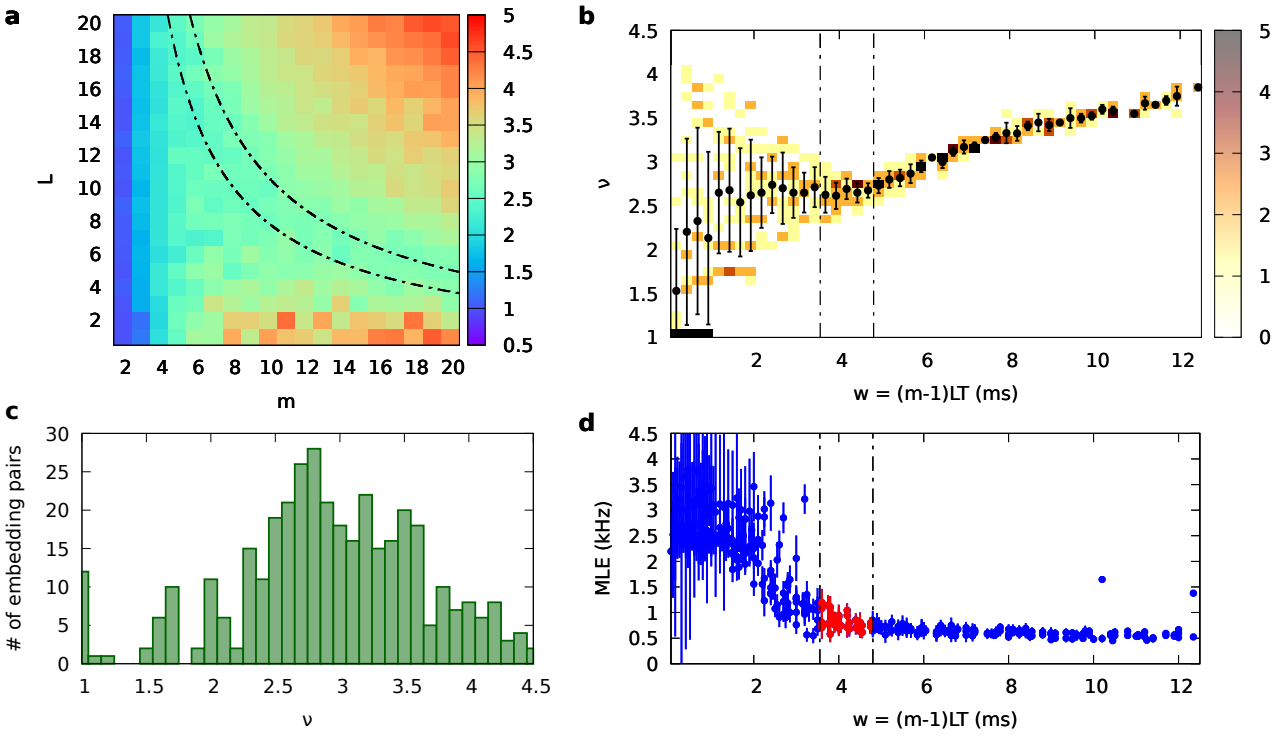

Figure 11: ciao

2.4 Five blocks

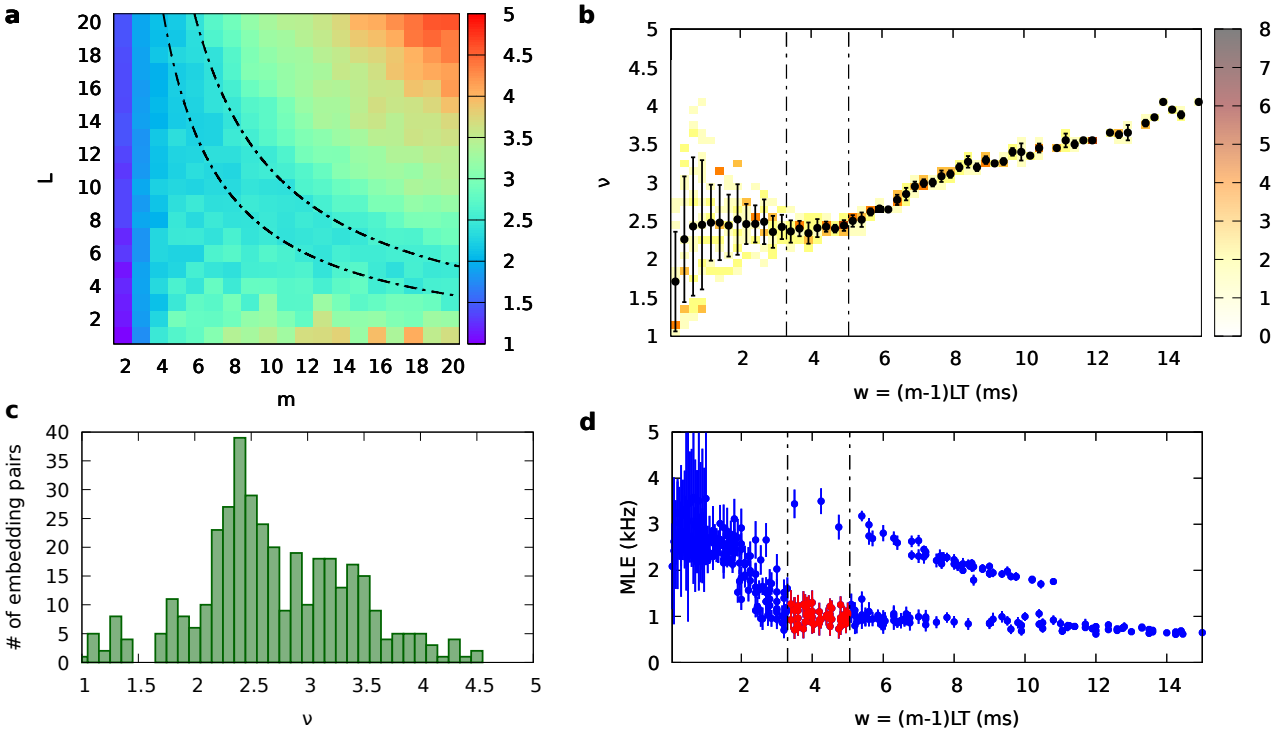

Figure 12: ciao

2.5 Six blocks

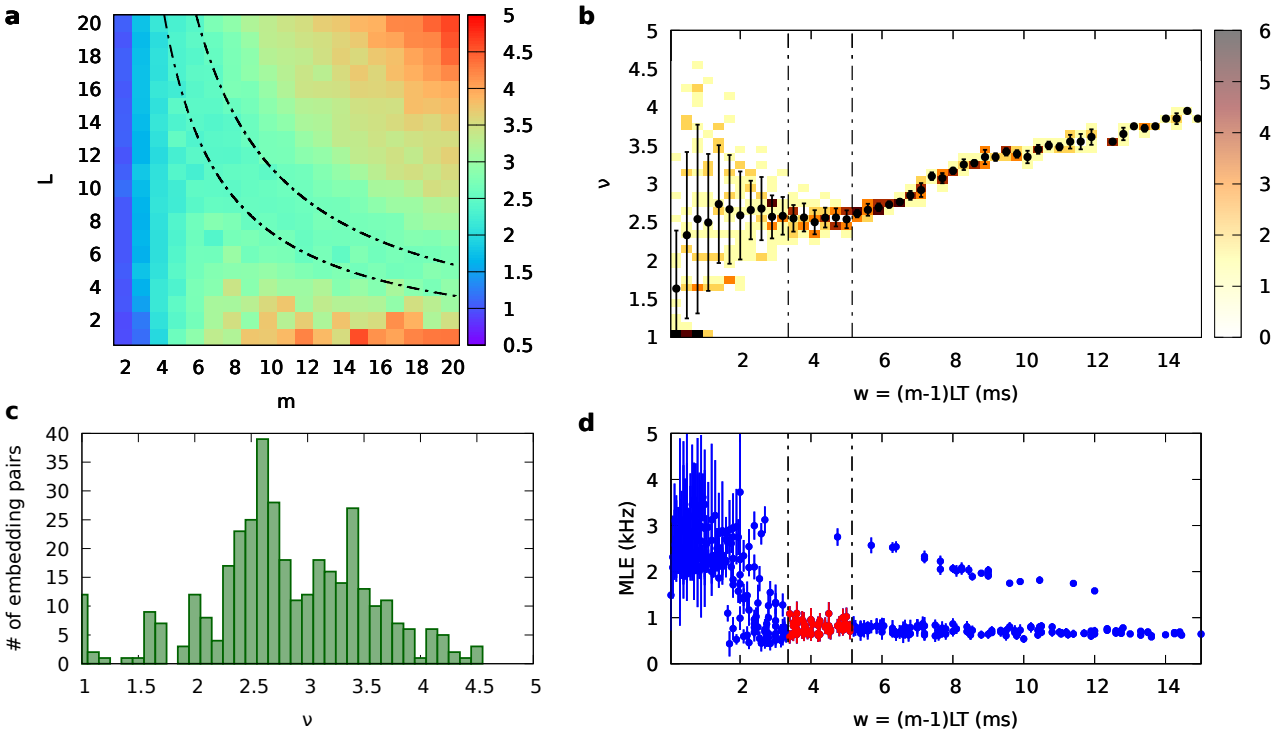

Figure 13: ciao

2.6 Seven blocks

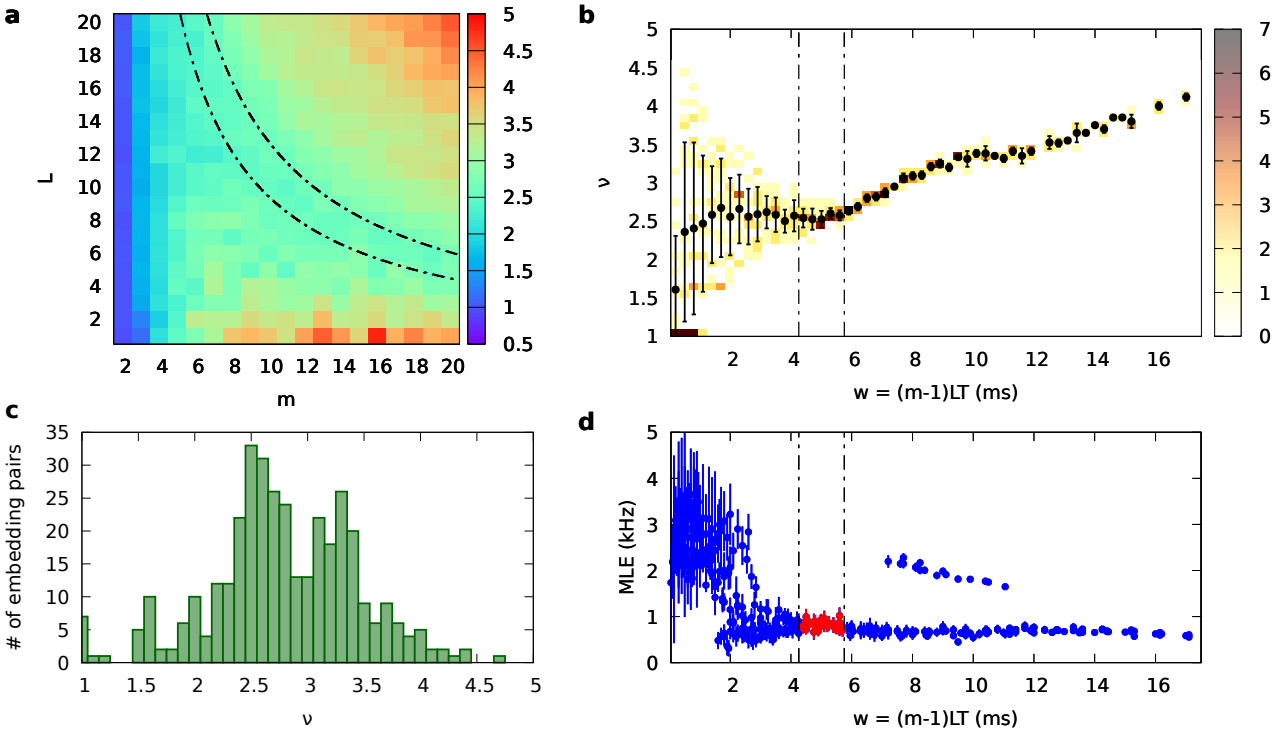

Figure 14: ciao

2.7 Eight blocks

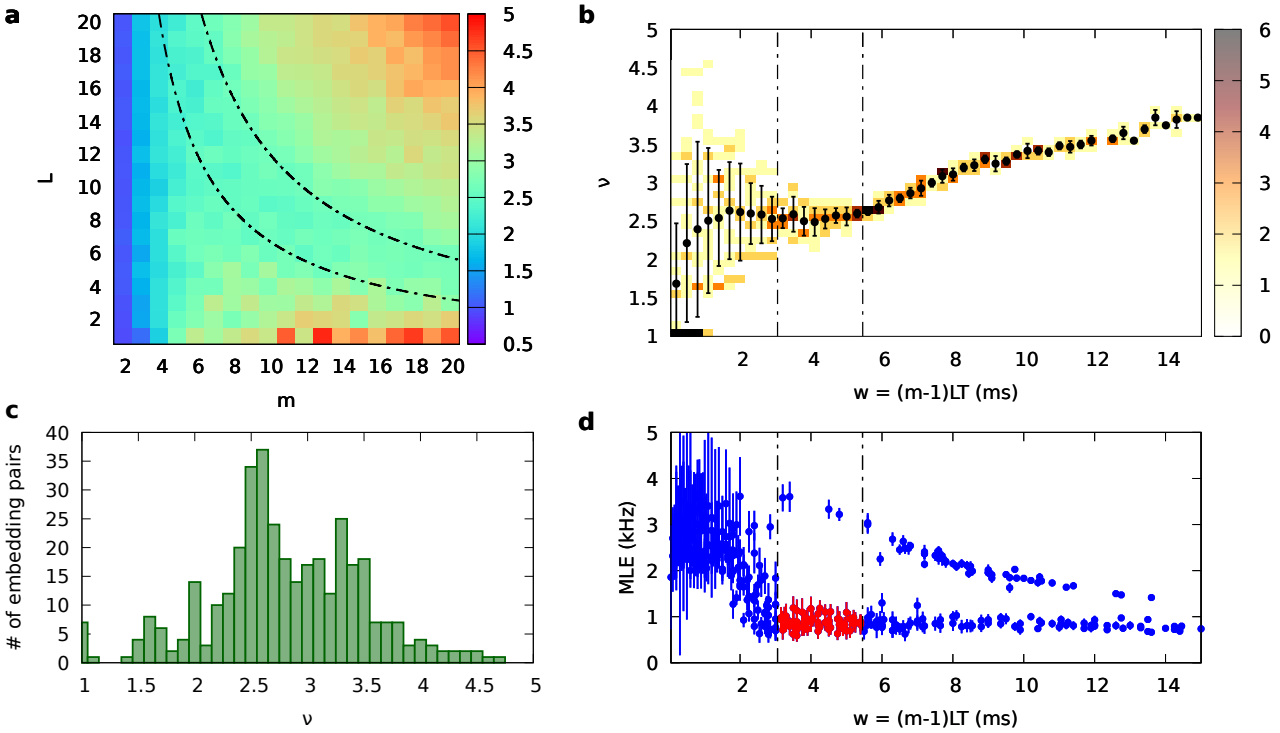

Figure 15: ciao

2.8 Nine blocks

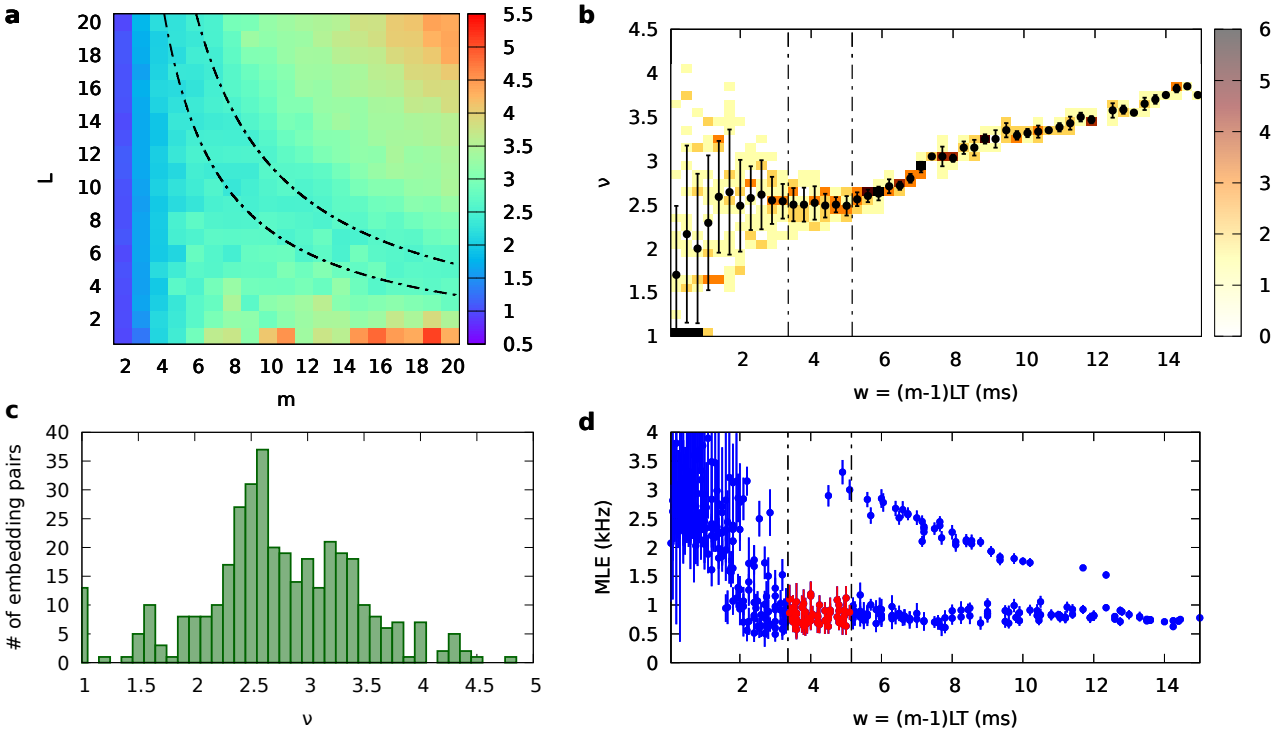

Figure 16: Edge

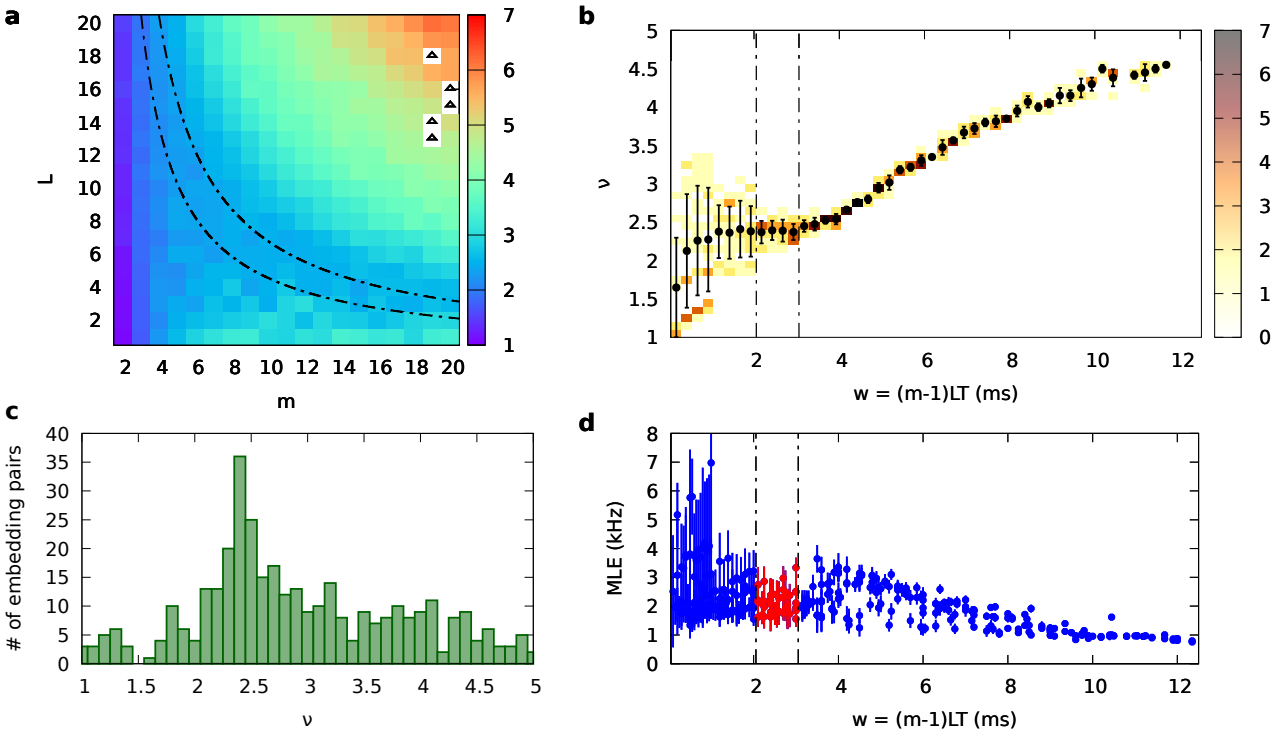

Figure 17: Middle

2.9 Ten blocks

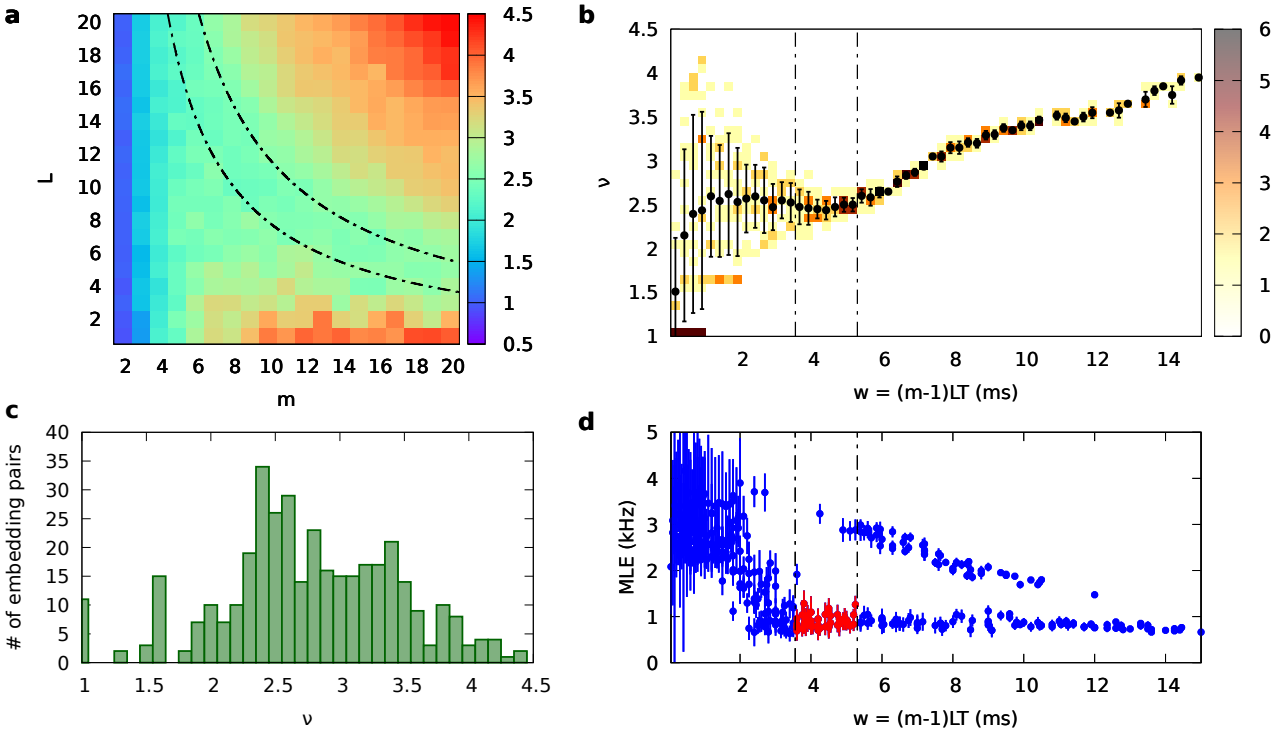

Figure 18: ciao

2.10 Conclusions

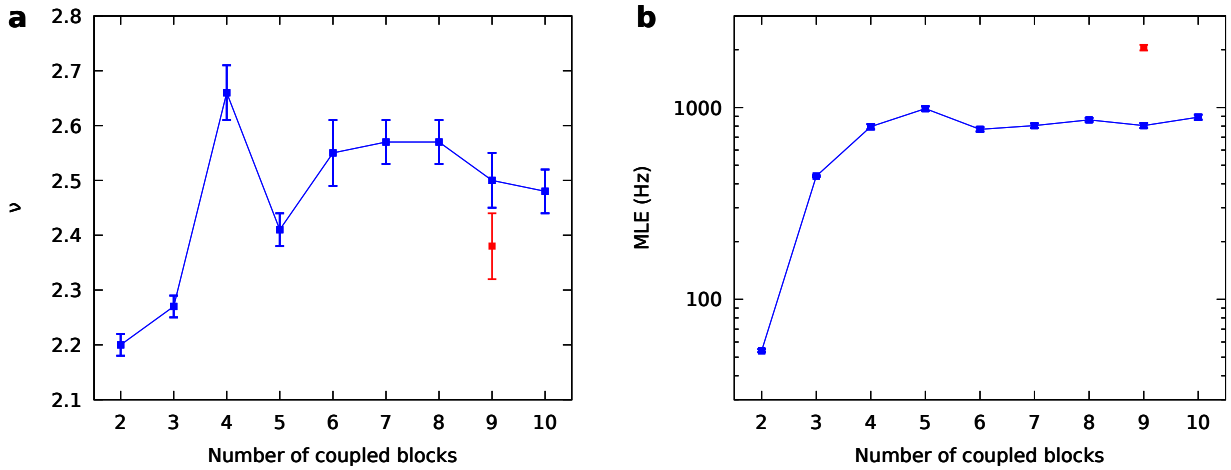

Figure 19: ciao

References

[1] A. Perinelli, R. Iuppa, and L. Ricci. "A scalable electronic analog of the Burridge–Knopoff model of earthquake faults". In: *Chaos 33, 093103* (2023). DOI: https://doi.org/10.1063/5.0161339.