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Problem 1

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-- Company:

-- Engineer:

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-- Create Date: 19:30:01 12/02/2013

-- Design Name:

-- Module Name: Conv\_to\_integer - Behavioral

-- Project Name:

-- Target Devices:

-- Tool versions:

-- Description:

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-- Dependencies:

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-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

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library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx primitives in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity Conv\_to\_integer is

Port ( A : in STD\_LOGIC\_VECTOR (7 downto 0);

B : in STD\_LOGIC\_VECTOR (7 downto 0);

Suma : out integer range 0 to 255);

end Conv\_to\_integer;

architecture Behavioral of Conv\_to\_integer is

function conv\_to\_integer (arg: std\_logic\_vector; size: integer) return integer is

variable aux : integer;

begin

aux := 0;

for i in 0 to size-1 loop

if (arg(i)='1') then

aux := aux + 2\*\*i;

else

aux := aux;

end if;

end loop;

return aux;

end conv\_to\_integer;

begin

suma <= conv\_to\_integer(A, 8) + Conv\_to\_integer(B, 8);

end Behavioral;

Problema dos

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-- Company:

-- Engineer:

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-- Create Date: 20:17:18 12/02/2013

-- Design Name:

-- Module Name: Final\_timer - Behavioral

-- Project Name:

-- Target Devices:

-- Tool versions:

-- Description:

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-- Dependencies:

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-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

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library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx primitives in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity Final\_timer is

Port ( Rst : in STD\_LOGIC;

Clk100Mhz : in STD\_LOGIC;

Segundos : in STD\_LOGIC\_VECTOR (7 downto 0);

Load : in STD\_LOGIC;

Seg : out STD\_LOGIC\_VECTOR (7 downto 0);

SelAn : out STD\_LOGIC\_VECTOR (3 downto 0);

Fin : out STD\_LOGIC);

end Final\_timer;

architecture Behavioral of Final\_timer is

component Clk1Hz

port (

Rst : in STD\_LOGIC;

Clk : in STD\_LOGIC;

ClkOut : out STD\_LOGIC);

end component;

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.STD\_LOGIC\_ARITH.ALL;

use IEEE.STD\_LOGIC\_UNSIGNED.ALL;

entity Cont0a99 is

port (

Load : in STD\_LOGIC;

Enable : in STD\_LOGIC;

Rst : in STD\_LOGIC;

Clk : in STD\_LOGIC;

ValorDec : in STD\_LOGIC\_VECTOR(3 downto 0);

ValorUni : in STD\_LOGIC\_VECTOR(3 downto 0);

Cuenta : out STD\_LOGIC\_VECTOR(7 downto 0));

end Cont0a99;

architecture Behavioral of Cont0a99 is

--EMBEDDED

signal CountUni : STD\_LOGIC\_VECTOR (3 downto 0);

signal CountDec : STD\_LOGIC\_VECTOR (3 downto 0);

begin

-- Count Unidades

process (Rst,Clk,Load)

begin

if ((Rst = '1') or (Load = '1')) then CountUni <= (others => '0');

elsif (rising\_edge(Clk)) then

if (Enable = '1') then

-- CountUni is reset when unidades = 9

if (CountUni = "1001") then CountUni <= (others => '0');

else CountUni <= CountUni - 1;

end if;

else CountUni <= CountUni;

end if;

end if;

end process;

-- Count Decenas

process (Rst,Clk,Load)

begin

if ((Rst = '1') or (Load = '1')) then CountDec <= (others => '0');

elsif (rising\_edge(Clk)) then

if (Enable = '1') then

if (CountDec = "1001") then CountDec <= (others => '0');

elsif (CountUni = "1001") then CountDec <= CountDec - 1;

end if;

else CountDec <= CountDec;

end if;

end if;

end process;

--Agrupar en un solo bus

Cuenta <= CountDec & CountUni;

end Behavioral;

component Mux4to1

port (

UnidadesCont : in STD\_LOGIC\_VECTOR(3 downto 0);

DecenasCont : in STD\_LOGIC\_VECTOR(3 downto 0);

Contador : out STD\_LOGIC\_VECTOR(3 downto 0));

end component;

-- Anode Selector.

-- According to a 2-bit count, select one of the 4

-- display anodes

component SelAnodo

port (

Sel : in STD\_LOGIC\_VECTOR(1 downto 0);

Anodo : out STD\_LOGIC\_VECTOR(3 downto 0));

end component;

-- BCD (or Binary could be used) to 7 Segment decoder

component DecBCD7Seg

port (

BCD : in STD\_LOGIC\_VECTOR(3 downto 0);

Seg : out STD\_LOGIC\_VECTOR(7 downto 0));

end component;

-- Embedded signal declaration

-- 1-bit Embedded Signals

signal Clk1Hz\_int : STD\_LOGIC;

signal ClkRefresh\_int : STD\_LOGIC;

signal contador\_int : STD\_LOGIC\_VECTOR(3 downto 0);

signal Sel\_int : STD\_LOGIC\_VECTOR(1 downto 0);

-- 8-bit Embedded Signals

signal Cuenta\_int : STD\_LOGIC\_VECTOR(7 downto 0);

begin

-- Do the wiring using VHDL

U1 : Clk1Hz

port map (

Rst => Rst,

Clk => Clk100MHz,

ClkOut => Clk1Hz\_int);

U2 : Cont0a99

port map (

Load => Load,

Rst => Rst,

Clk => Clk100MHz,

ValorDec => SegundosUni (3 downto 0),

ValorUni => SegundosDec (3 downto 0),

Cuenta => Cuenta\_int);

U3 : RefreshDisplay

port map (

Rst => Rst,

Clk => Clk100MHz,

ClkOut => ClkRefresh\_int);

U4 : Mux4to1

port map (

UnidadesCont => Cuenta\_int(3 downto 0),

DecenasCont => Cuenta\_int(7 downto 4),

Contador => Contador\_int);

U5 : SelAnodo

port map (

Sel => Sel\_int,

Anodo => SelAn);

U6 : DecBCD7Seg

port map (

BCD => Contador\_int,

Seg => Seg);

end Behavioral;

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-- Company:

-- Engineer:

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-- Create Date: 11:27:52 10/06/2010

-- Design Name:

-- Module Name: Clk1Hz - Behavioral

-- Project Name:

-- Target Devices:

-- Tool versions:

-- Description:

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-- Dependencies:

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-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

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library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.STD\_LOGIC\_ARITH.ALL;

use IEEE.STD\_LOGIC\_UNSIGNED.ALL;

entity Clk1Hz is

port (

Rst : in STD\_LOGIC;

Clk : in STD\_LOGIC;

ClkOut : out STD\_LOGIC);

end Clk1Hz;

architecture Behavioral of Clk1Hz is

--Declaraciones de constantes

constant Fosc : integer := 100000000; --Frecuencia del oscilador de tabletas NEXYS 3

constant Fdiv : integer := 1; --Frecuencia deseada del divisor

constant CtaMax : integer := Fosc / Fdiv; --Cuenta maxima a la que hay que llegar

--Declaracion de signals

signal Cont : integer range 0 to CtaMax;

begin

--Proceso que Divide la Frecuencia de entrada para obtener una Frecuencia de 1 Hz

process (Rst, Clk)

begin

if Rst = '1' then

Cont <= 0;

elsif (rising\_edge(Clk)) then

if Cont = CtaMax then

Cont <= 0;

ClkOut <= '1';

else

Cont <= Cont + 1;

ClkOut<= '0';

end if;

end if;

end process;

end Behavioral;

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.STD\_LOGIC\_ARITH.ALL;

use IEEE.STD\_LOGIC\_UNSIGNED.ALL;

entity Cont0a99 is

port (

Load : in STD\_LOGIC;

Enable : in STD\_LOGIC;

Rst : in STD\_LOGIC;

Clk : in STD\_LOGIC;

ValorUnidades : in STD\_LOGIC\_VECTOR(3 downto 0);

ValorDecenas : in STD\_LOGIC\_VECTOR(3 downto 0);

Cuenta : out STD\_LOGIC\_VECTOR(7 downto 0));

end Cont0a99;

architecture Behavioral of Cont0a99 is

--EMBEDDED

signal CountUni : STD\_LOGIC\_VECTOR (3 downto 0);

signal CountDec : STD\_LOGIC\_VECTOR (3 downto 0);

begin

-- Count Unidades

process (Rst,Clk,Load)

begin

if ((Rst = '1') or (Load = '1')) then CountUni <= (others => '0');

elsif (rising\_edge(Clk)) then

if (Enable = '1') then

-- CountUni is reset when unidades = 9

if (CountUni = "1001") then CountUni <= (others => '0');

else CountUni <= CountUni - 1;

end if;

else CountUni <= CountUni;

end if;

end if;

end process;

-- Count Decenas

process (Rst,Clk,Load)

begin

if ((Rst = '1') or (Load = '1')) then CountDec <= (others => '0');

elsif (rising\_edge(Clk)) then

if (Enable = '1') then

if (CountDec = "1001") then CountDec <= (others => '0');

elsif (CountUni = "1001") then CountDec <= CountDec - 1;

end if;

else CountDec <= CountDec;

end if;

end if;

end process;

--Agrupar en un solo bus

Cuenta <= CountDec & CountUni;

end Behavioral;

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-- Company:

-- Engineer:

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-- Create Date: 11:47:07 10/06/2010

-- Design Name:

-- Module Name: RefreshDisplay - Behavioral

-- Project Name:

-- Target Devices:

-- Tool versions:

-- Description:

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-- Dependencies:

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-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

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library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.STD\_LOGIC\_ARITH.ALL;

use IEEE.STD\_LOGIC\_UNSIGNED.ALL;

entity RefreshDisplay is

port (

Rst : in STD\_LOGIC;

Clk : in STD\_LOGIC;

ClkOut : out STD\_LOGIC);

end RefreshDisplay;

architecture Behavioral of RefreshDisplay is

--Declaraciones de constantes

constant Fosc : integer := 100000000; --Frecuencia del oscilador de tabletas NEXYS 3

constant Fdiv : integer := 800; --Frecuencia deseada del divisor

constant CtaMax : integer := Fosc / Fdiv; --Cuenta maxima a la que hay que llegar

--Declaracion de signals

signal Cont : integer range 0 to CtaMax;

begin

--Proceso que Divide la Frecuencia de entrada para obtener una Frecuencia de Refresh

process (Rst, Clk)

begin

if Rst = '1' then

Cont <= 0;

elsif (rising\_edge(Clk)) then

if Cont = CtaMax then

Cont <= 0;

ClkOut <= '1';

else

Cont <= Cont + 1;

ClkOut<= '0';

end if;

end if;

end process;

end Behavioral;

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-- Company:

-- Engineer:

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-- Create Date: 13:18:24 10/06/2010

-- Design Name:

-- Module Name: Mux4to1 - Behavioral

-- Project Name:

-- Target Devices:

-- Tool versions:

-- Description:

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-- Dependencies:

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-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

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library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.STD\_LOGIC\_ARITH.ALL;

use IEEE.STD\_LOGIC\_UNSIGNED.ALL;

entity Mux4to1 is

port (

DecHor : in STD\_LOGIC\_VECTOR (3 downto 0);

UniHor : in STD\_LOGIC\_VECTOR (3 downto 0);

DecMin : in STD\_LOGIC\_VECTOR (3 downto 0);

UniMin : in STD\_LOGIC\_VECTOR (3 downto 0);

Sel : in STD\_LOGIC\_VECTOR (1 downto 0);

Tiempo : out STD\_LOGIC\_VECTOR (3 downto 0));

end Mux4to1;

architecture Behavioral of Mux4to1 is

begin

--Seleccion de unidad de tiempo HH:MM

with Sel select

Tiempo <= UniMin when "00",

DecMin when "01",

UniHor when "10",

DecHor when others;

end Behavioral;

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-- Company:

-- Engineer:

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-- Create Date: 13:34:41 10/06/2010

-- Design Name:

-- Module Name: SelAnodo - Behavioral

-- Project Name:

-- Target Devices:

-- Tool versions:

-- Description:

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-- Dependencies:

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-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

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library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.STD\_LOGIC\_ARITH.ALL;

use IEEE.STD\_LOGIC\_UNSIGNED.ALL;

entity SelAnodo is

port (

Sel : in STD\_LOGIC\_VECTOR (1 downto 0);

Anodo : out STD\_LOGIC\_VECTOR (3 downto 0));

end SelAnodo;

architecture Behavioral of SelAnodo is

begin

--Seleccion de display

with Sel select

Anodo <= "1110" when "00",

"1101" when "01",

"1011" when "10",

"0111" when others;

end Behavioral;

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-- Company:

-- Engineer:

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-- Create Date: 13:37:01 10/06/2010

-- Design Name:

-- Module Name: DecBCD7Seg - Behavioral

-- Project Name:

-- Target Devices:

-- Tool versions:

-- Description:

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-- Dependencies:

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-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

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library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.STD\_LOGIC\_ARITH.ALL;

use IEEE.STD\_LOGIC\_UNSIGNED.ALL;

entity DecBCD7Seg is

port (

BCD : in STD\_LOGIC\_VECTOR (3 downto 0);

Seg : out STD\_LOGIC\_VECTOR (7 downto 0));

end DecBCD7Seg;

architecture Behavioral of DecBCD7Seg is

begin

--Implementacion de un decodificador Binario a 7 segmentos que tambien sirve como

--Decodificador BCD a 7 segmentos

--Los segmentos encienden con un 0 logico, se apagan con un 1 logico

with BCD select

-- .gfedcba

Seg <= "11000000" when X"0",

"11111001" when X"1",

"10100100" when X"2",

"10110000" when X"3",

"10011001" when X"4",

"10010010" when X"5",

"10000010" when X"6",

"11111000" when X"7",

"10000000" when X"8",

"10010000" when X"9",

"10000110" when X"A",

"10000110" when X"B",

"10000110" when X"C",

"10000110" when X"D",

"10000110" when X"E",

"10000110" when X"F",

"10000110" when others;

end Behavioral;