Roll No. _____ Name_____ Group_____

Computer Science & Engineering Department
Thapar Institute of Engineering & Technology, Patiala
Microprocessor Based Systems Design (UCS617)
Theory Quiz-1 (Set-A) [February 29, 2024]

Total Time: 10+5=15 min [05:15 PM - 05:30 PM] **Total Marks: 10+5= 15**

Instructions for students:

- Any cutting or overwriting will be considered as a wrong answer.
- Missing roll number or name will be considered as an absent.
- No Negative marking is there and no extra material is allowed.

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1. On finding the RST 5 instruction, the execution would be transferred to the following memory location:
a. 0038
b. **0028**
c. 0008
d. 0020

2. What will be the combination of $\overline{S_2}$, $\overline{S_1}$, and $\overline{S_0}$to select halt?
a. 1, 0, 1
b. 0, 0, 0
c. 0, 1, 0
d. **0, 1, 1**

3. After the execution of the following 8085 assemble language program, what will be the status of PSW?

```
MVI A, 56 H
ADI AB H
RST 5
```

a. 1001 0101
b. **0001 0001**
c. 0001 0101
d. 1001 0001

4. A software delay subroutine is given below:

```
DELAY: MVI B, FF H
MVI C, FF H
LOOP:  DCR C
JNZ LOOP
DCR B
JNZ LOOP
```

How many times DCR C instruction will be executed?
a. **$(65279)_{10}$**
b. $(65379)_{10}$
c. $(65479)_{10}$
d. $(65579)_{10}$

5. Interpret Bit pattern: 0100 1010 for SIM instruction:
a. All interrupts are masked and no data is sent.
b. **RST 6.5 is masked, and 0 is sent on the SOD pin.**
c. RST 5.5 and RST 7.5 is masked, and 0 is sent on the SOD pin.
d. Reset RST7.5, RST6.5, and RST5.5.

6. How many numbers of T-states for RZ instruction of an 8085 microprocessor?
a. 10/4
b. 10/6
c. 12/6
d. 12/4

7. In a microprocessor, the service routine for a certain interrupt starts from a fixed location of memory which cannot be externally set but the interrupt can be delayed and rejected. Such an interrupt is known as:
a. Non-maskable and non-vectored
b. Maskable and non-vectored
c. Non-maskable and vectored
d. **Maskable and vectored**

8. The physical address of the logical address A4FB:3871 is
a. **A8821**
b. A7821
c. A8121
d. A8221

9. What will be the combination of bits on Queue status signals $\overline{QS_1}$ and $\overline{QS_0}$ to represent that the queue is empty?
a. 0 0
b. 1 1
c. **1 0**
d. 0 1

10. **Stack Pointer** is used as an offset from the current SS during the execution of instructions that involve the stack segment in the external memory and **Base Pointer** contains an offset address in the current SS, which is used by instructions utilizing the based addressing mode.

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Lab Quiz-1 (Set A) [February29, 2024]

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1. Suppose that we have to subtract 83 from 38 such that 38 and 83 are stored in memory at 8050H and 8051H respectively. Dr. Kuldeep has written the program for achieving this task which has the following code snippet. Interpret it.

```
LXI H, 8051H
MVI A, 99
SUB M
INR A
```

a. Determine the one's complement of 83
b. Determine the two's complement of 83
c. **Determine the 10's complement of 83**
d. None of these

[1]

2. An 8085-assembly language program is given below. Assume the carry flag is initially unset. The content of the accumulator after the execution of the program is

```
MVI A, 93 H
RLC
MOV B, A
ADD B
RLC
RST 5
```

a. 9C H
b. 27 H
c. C9 H
d. 72 H

[1]

3. Determine the missing instruction in the following code such that the output generated in the accumulator would be D3 H.

```
MVI A, 23H
_____
HLT
```

a. ADI D0H
b. ANI D0H
c. ORI D0H
d. XRI F0H

[1]

4. Write the missing instructions to find the total number of positive numbers in a block of data stored at memory locations starting from A400H to A409H and store the result at A40AH.

```
        MVI C, 0A H
        MVI B, 00 H
        LXI H, A400 H
BACK:   MOV A, M
ANI 80 H
JNZ SKIP
INR B
SKIP:   INX H
        DCR C
JNZ BACK
        MOV B, M
        RST 5
```

[2]